SHARP SERVICE MANUAL

CODE : 00ZMZ1E14//-E

MODEL MZ-1E14

CONTENTS

SHARP CORPORATION

1. SPECIFICATION

1-1. General specification

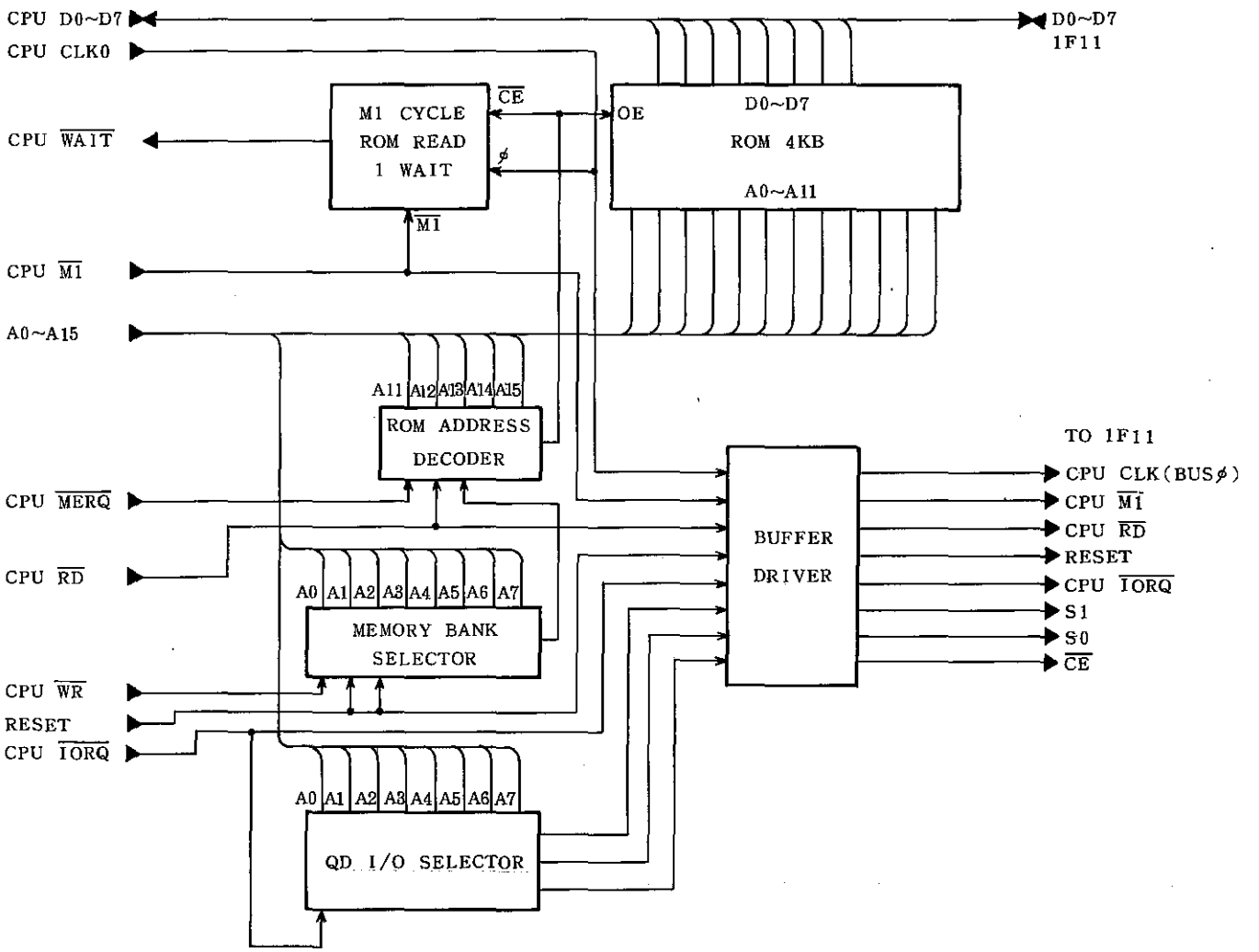
Pin configuration	See the wiring diagram for detail of bus line connector and the SIO connector.
Signal level	TTL level Input/output electrical characteristics shall conform to the IC used.
Input/output specification	ICs used: SN74LS00 SN74LS02 SN74LS04 SN74LS10 SN74LS30 SN74LS74 SN74LS138 SN74LS541 2732(ROM)
Operating temperature	5°C ~ 35°C
Storage temperature	−15°C ~ 60°C
Supply voltage	5V±5% (external power supply not needed when used in conjunction with the 1F11, MZ-700).
Physical dimensions	

1-2. Buffered signals

The following signals are buffered by the SN74LA541.
IORQ, RESET, RD, CE, S1, S0, ϕ, M1

2. BLOCK DIAGRAM

2-1. Block diagram



2-2. Description

1) ROM

The MZ disk monitor routine program is contained in the ROM. It locates on the MZ-700 VRAM, key side bank, dominating the 2 KB addresses of $E800 through $EFFF. Even though the 2732 ROM has a 4 KB capacity, only 2 KB are used actually.

The MZ-700 monitor ROM reads the contents of $E800 to check if it is $00. If so, the control advances to $E800 for execution.

2) M1 CYCLE ROM READ 1 WAIT

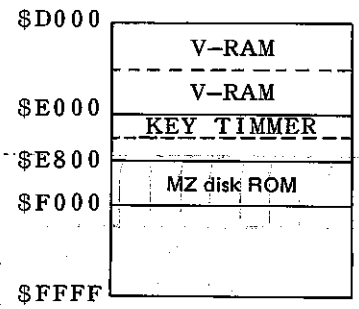
This block is used to insert a single wait during the M1 cycle (op code fetch) of the Z-80 CPU in executing the contents of the above ROM, as it uses the memory of relatively slow access while a faster memory is required for the memory read in the M1 cycle.

3) ROM ADDRESS DECODER

This block enables data output of the ROM when the VRAM side bank has been assigned at 4) and that the CPU has executed the read operation to the address $E800 through $EFFF.

4) MEMORY BANK SELECTOR

Performs to select the memory bank. Only when the MZ-700 has chosen the VRAM side bank, it makes bank output enabled.



5) MZ DISK I/O SELECTOR

The SIO of the 1F11 is enabled only when the CPU accesses the I/O address of the MZ disk.

The table below shows the relation among address, S1, S0, and $\overline{CE}$.

I/O port	$\overline{C/E}$	S1	S0	SIO register
$F4	0	0	0	Channel A DATA
$F5	0	0	1	Channel B DATA
$F6	0	1	0	Channel A CWR
$F7	0	1	1	Channel B CWR

6) BUFFER DRIVER

Not only enhances signal driving capacity to the signal sent to the 1F11, but reduced influences to the CPU as much as possible.

7) 1F11 interfacing signals

a. CPU CLOCK (BUS ϕ) ..... MZ-700 CPU clock (3.85 MHz).
b. CPU$\overline{M1}$ ..... $\overline{M1}$ signal from the MZ-700 CPU.
c. CPU$\overline{RD}$ ..... $\overline{RD}$ signal from the MZ-700.
d. CPU$\overline{IORQ}$ ..... $\overline{IORQ}$ signal from the MZ-700.
e. $\overline{RESET}$ ..... MZ-700 system reset signal.
f. $\overline{CE}$ ..... 1F11 SIO chip enable signal.
g. S1 ..... 1F11 SIO control/data select signal.
h. S0 ..... 1F11 SIO channel A/B select signal.

3. TROUBLESHOOTING

1) Troubleshooting procedure

In the first place it becomes necessary to find out on which side the trouble is; 1E14 or 1F11. Get the properly functioning 1E14 and 1F11 connected with the unit one at a time to find out which connection causes the trouble.

2) Described next are possible causes which may occur when either the 1E14 or 1E11 is in connection.

3-1. Problem causes by the 1E14

(1) ROM starts

The message "MAKE READY OD**MONITOR 9Z-503M**" does appear on the display when power is turned on with the disk loaded in the drive unit.

(2) No operation can take place (including program wild run).

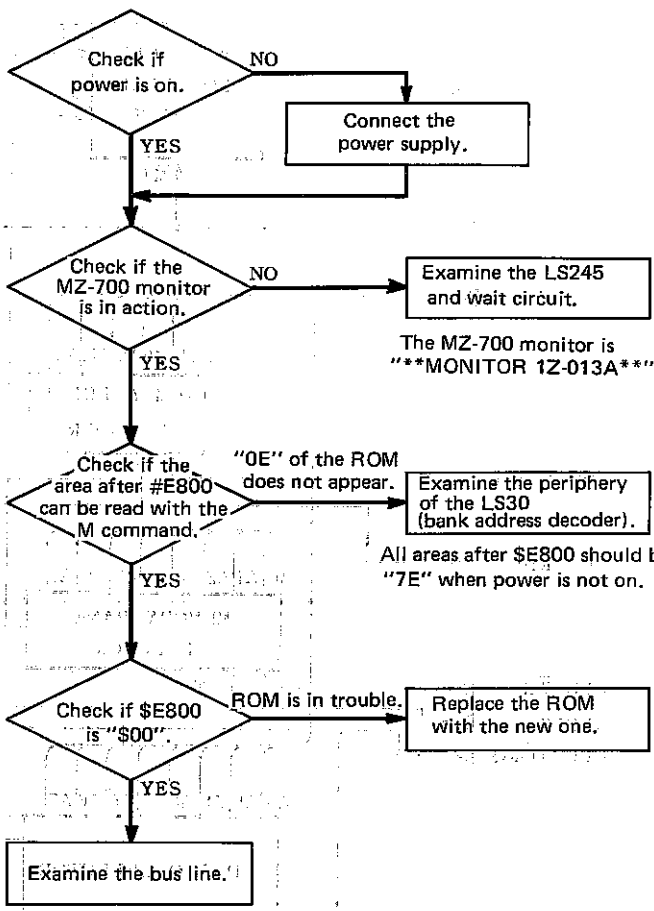
3-2. Problem caused by the 1F11

(1) The motor does not start to run.
(2) Write does take place.
- Write protect error occurs at all times.
- The message "NOT READY ERROR" displayed.
- The data written on the disk can not be read.

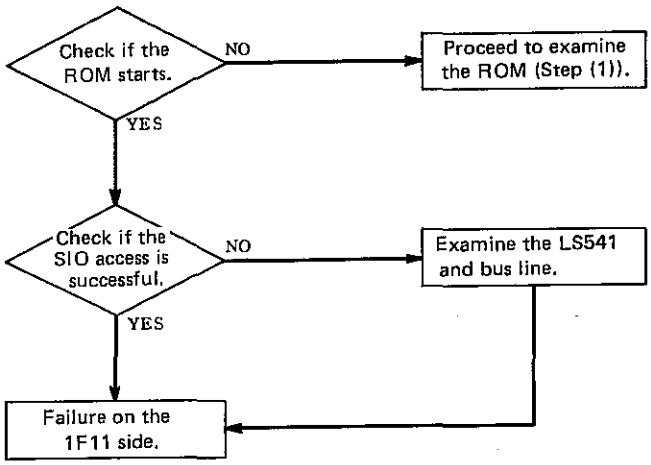
(3) Read is not enabled.

Troubleshooting procedure —1E14—

(1) ROM does not start.



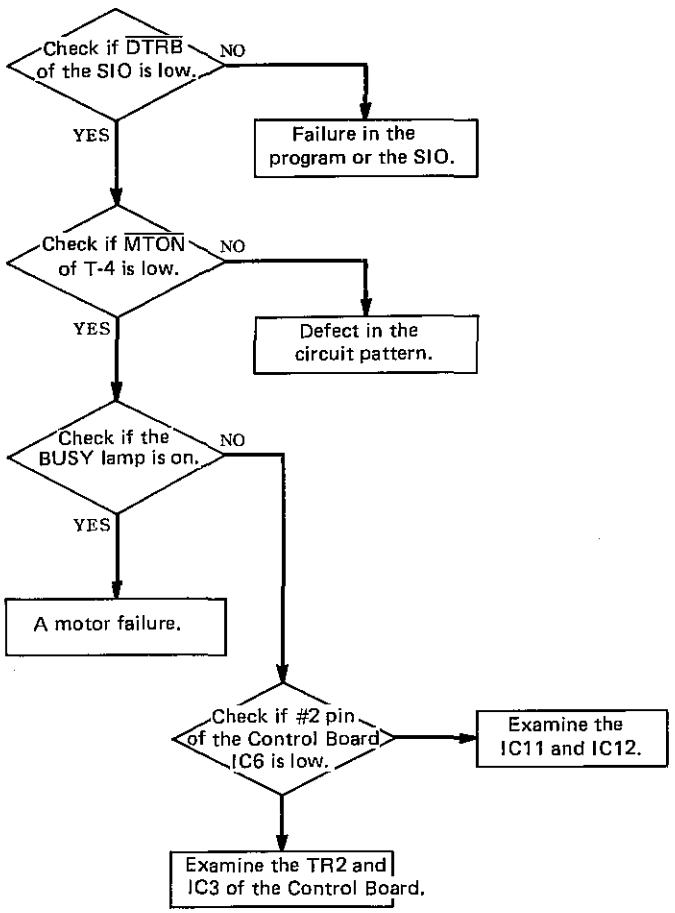
(2) No operation can take place



–1F11–

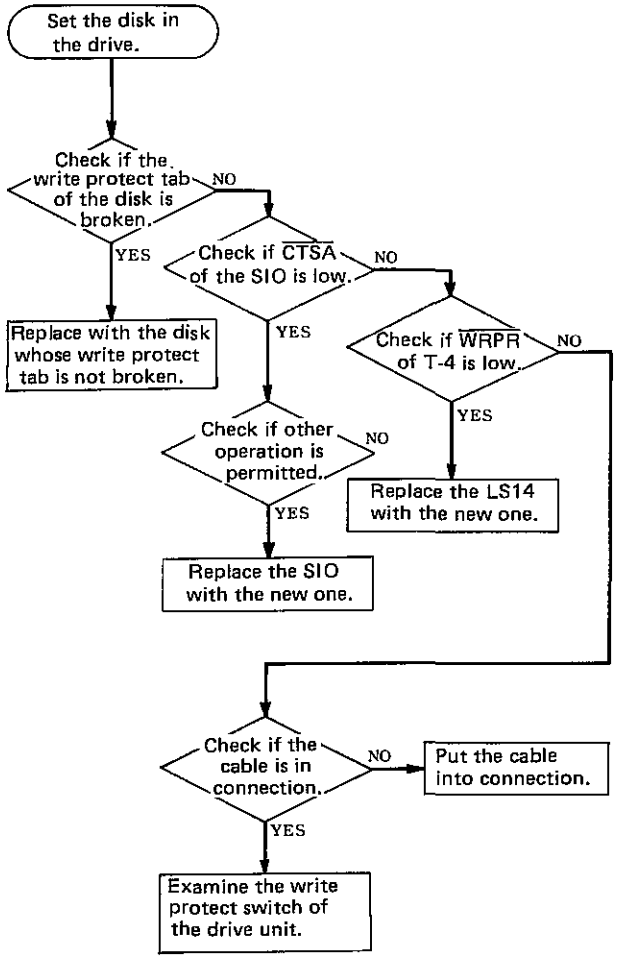
(a) The motor does not start to run.

Conduct test while the LOAD command is in execution.

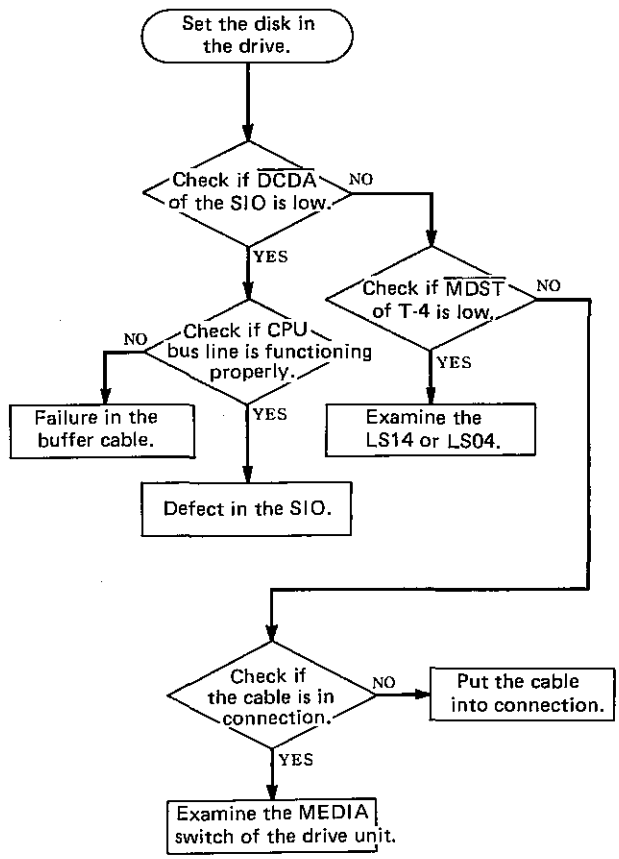


(b) Write is not enabled.

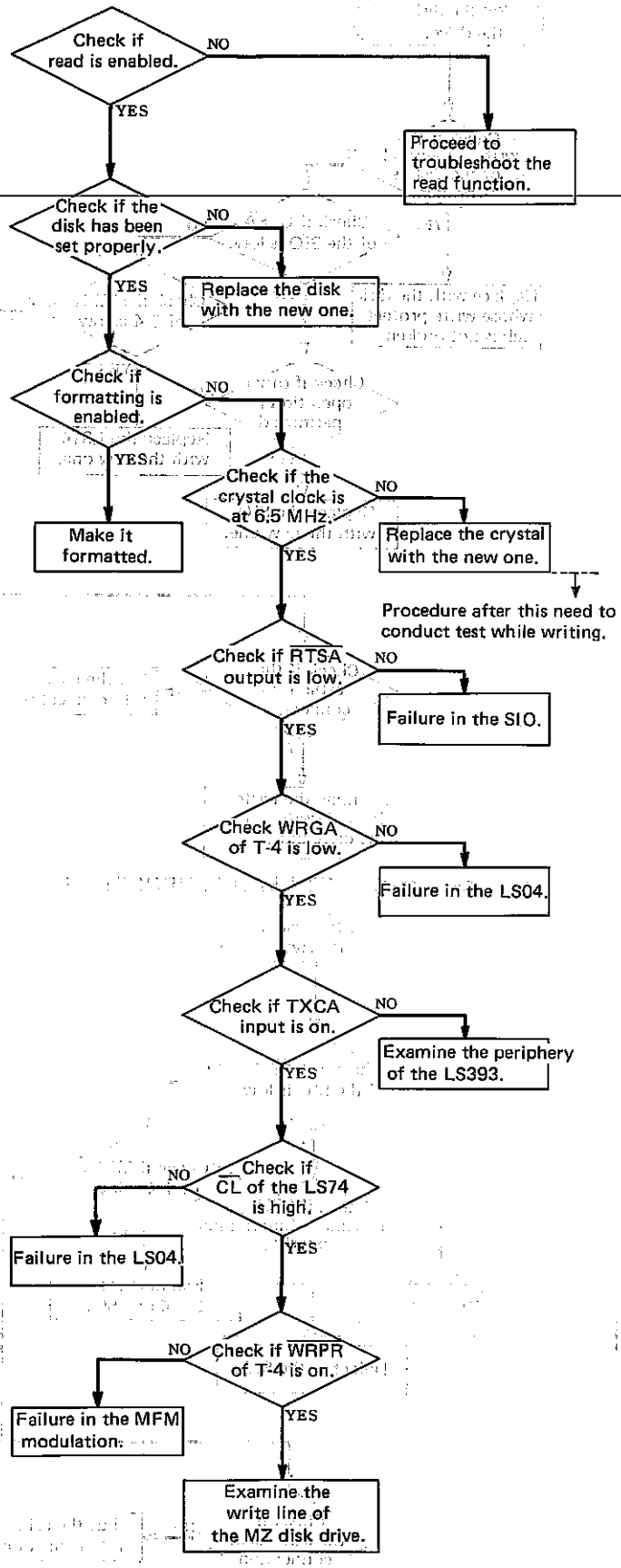
(1) Write protect error occurs at all times.



(2) The message "NOT READY ERROR" displayed.

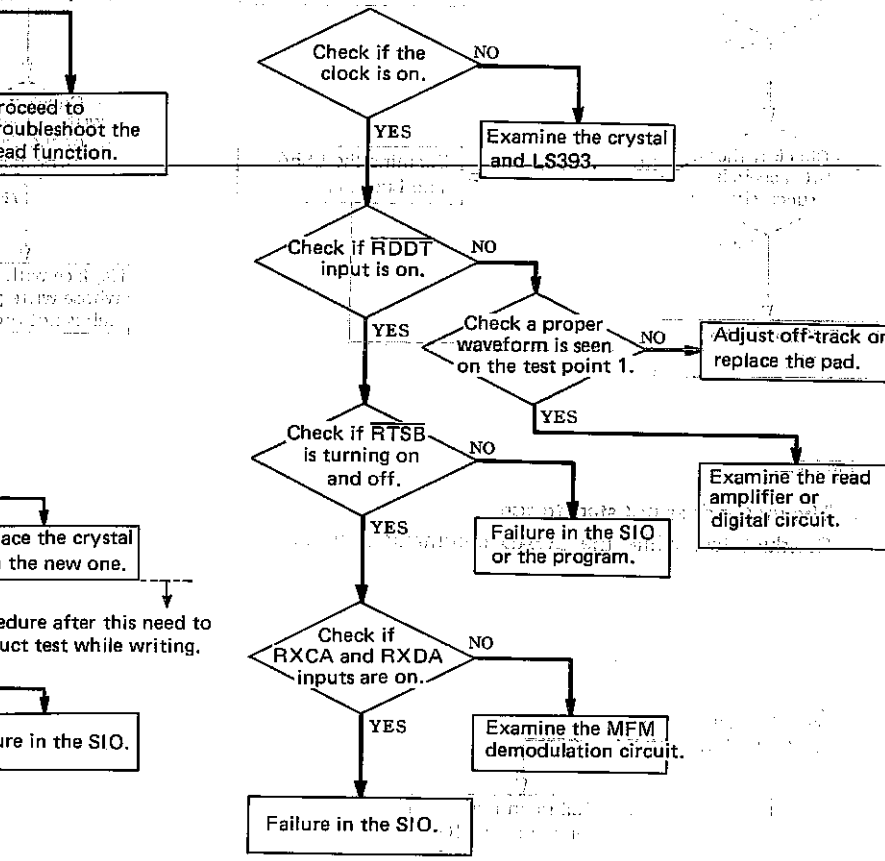


(3) Write is not enabled.



(c) **Read is not enabled.**

Set the disk in the MZ disk and conduct test while the LOAD command is in execution.



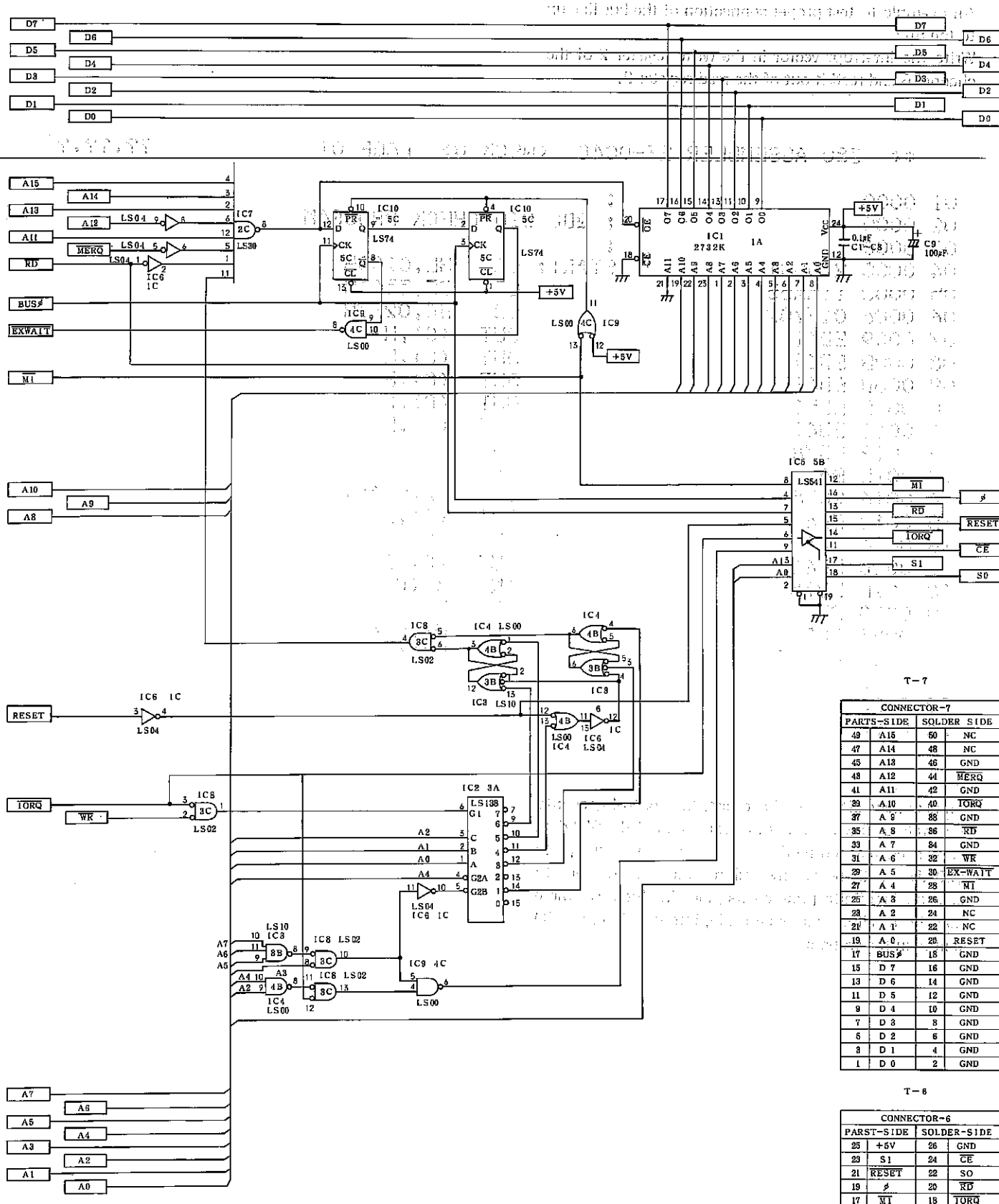
* Procedure to examine the SIO bus line (with the MZ-700, 1E14, 1F11 in connection).
An example to test proper connection of the bus line up to the SIO.
Write the interrupt vector in the write register 2 of the channel B and read it out of the read register 2.

```
**  Z80 ASSEMBLER 2Z-004C  <QSCK-0>  PAGE 01                ??.??.?

01 0000                    ;
02 0000                    ; QDC SIO CHECK PROGRAM
03 0000                    ;
04 0000 210001             START: LD   HL,0100H
05 0003 11AA55                    LD   DE,55AAH
06 0006 01F702                    LD   BC,02F7H
07 0009 ED61                      OUT  (C),H
08 000B ED69                      OUT  (C),L
09 000D ED41                      OUT  (C),B
10 000F ED51                      OUT  (C),D
11 0011 ED41                      OUT  (C),B
12 0013 ED78                      IN   A,(C)
13 0015 BA                        CP   D
14 0016 20E8                      JR   NZ,START
15 0018 ED41                      OUT  (C),B
16 001A ED59                      OUT  (C),E
17 001C ED41                      OUT  (C),B
18 001E ED78                      IN   A,(C)
19 0020 BB                        CP   E
20 0021 20DD                      JR   NZ,START
21 0023 C304E8                    JP   E804H
22 0026
23 0026
24 0026                           END
```

Immediately after the above test, the control goes into the state of ready for monitor command, if the SIO data have been read correctly, that is, the control jumps to $00AD. If there is any failure, the control goes to execute indefinite program looping. In this case, there may be a failure like open cable, buffer failure, or SIO failure in the worst case.

4. CIRCUIT DIAGRAM



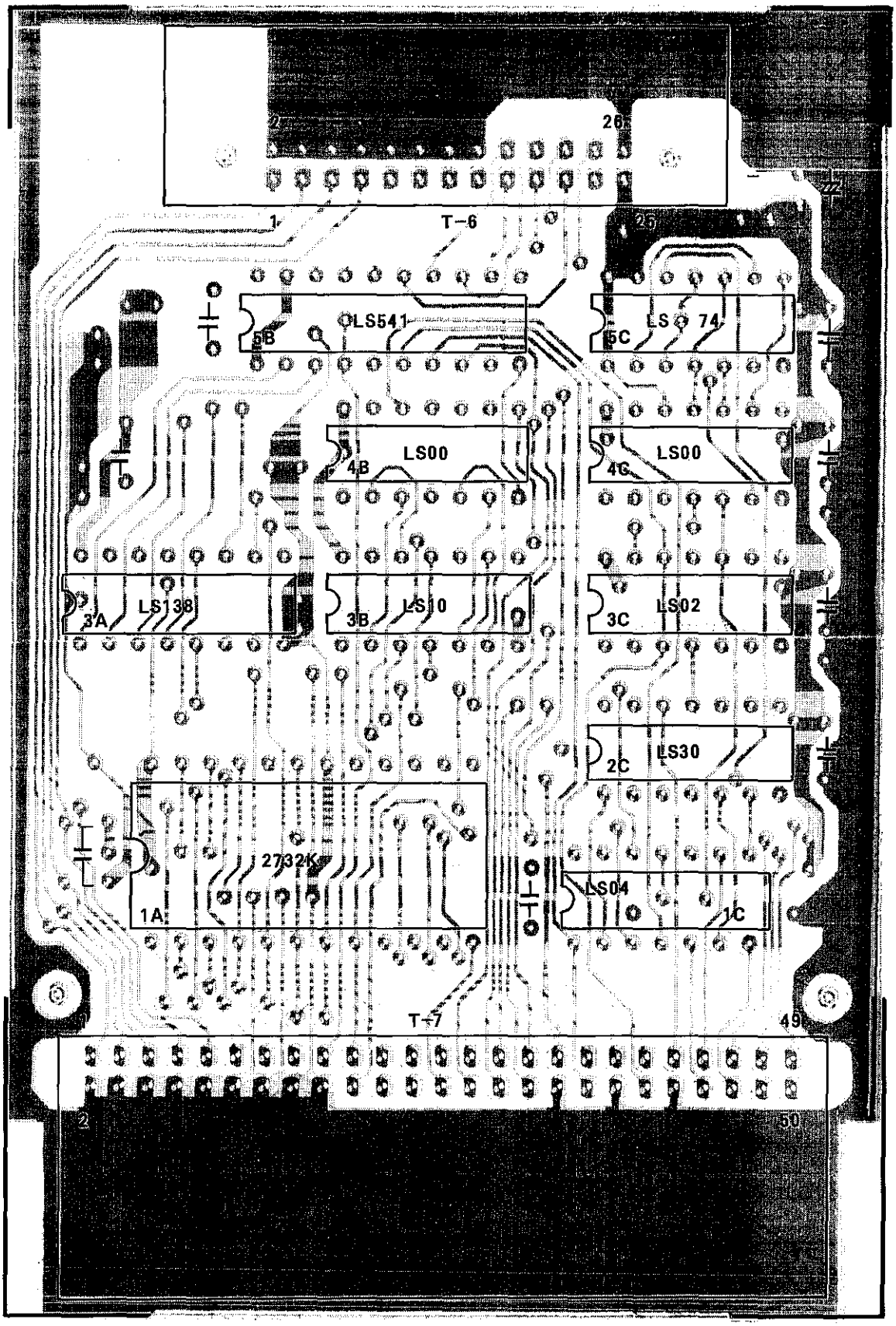
T-7

CONNECTOR-7			
PARTS-SIDE		SOLDER SIDE	
49	A15	50	NC
47	A14	48	NC
45	A13	46	GND
43	A12	44	MERQ
41	A11	42	GND
39	A10	40	IORQ
37	A 9	38	GND
35	A 8	36	RD
33	A 7	34	GND
31	A 6	32	WR
29	A 5	30	EX-WAIT
27	A 4	28	MI
25	A 3	26	GND
23	A 2	24	NC
21	A 1	22	NC
19	A 0	20	RESET
17	BUSϕ	18	GND
15	D 7	16	GND
13	D 6	14	GND
11	D 5	12	GND
9	D 4	10	GND
7	D 3	8	GND
5	D 2	6	GND
3	D 1	4	GND
1	D 0	2	GND

T-6

CONNECTOR-6			
PARST-SIDE		SOLDER-SIDE	
25	+5V	26	GND
23	S1	24	CE
21	RESET	22	SO
19	ϕ	20	RD
17	M1	18	IORQ
15	D7	16	GND
13	D6	14	GND
11	D5	12	GND
9	D4	10	GND
7	D3	8	GND
5	D2	6	GND
3	D1	4	GND
1	D0	2	GND

5. PARTS & SIGNAL LAYOUT



6. PARTS GUIDE

1 EXTERIORS

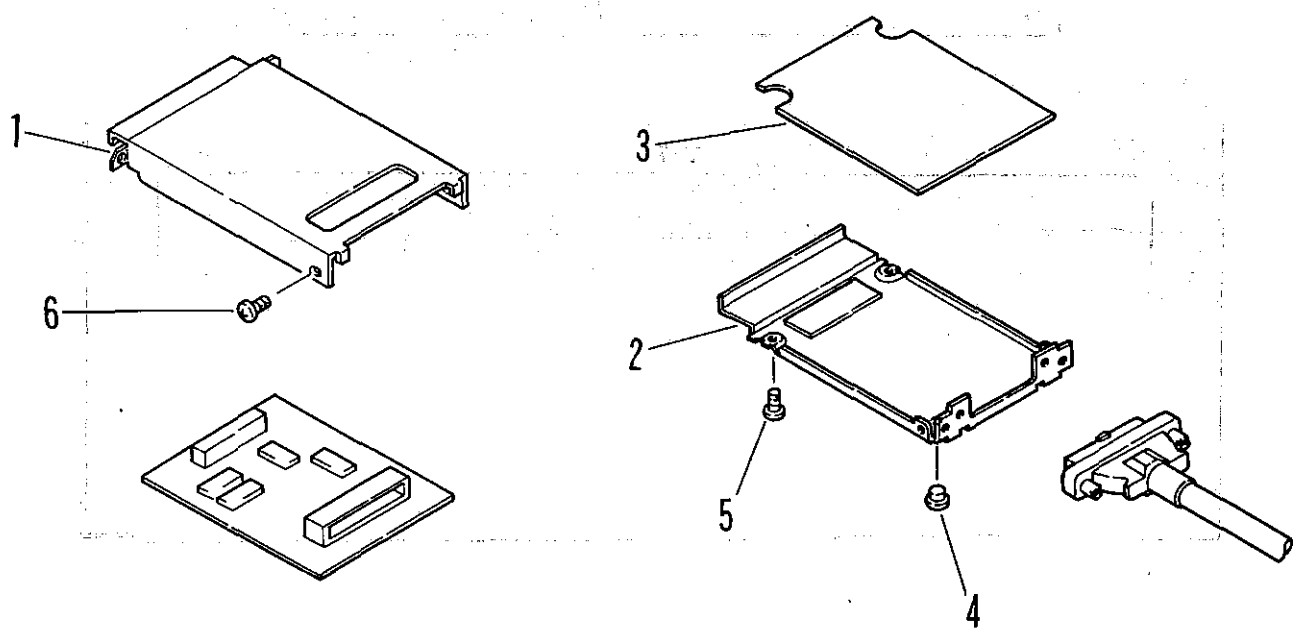
NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	0CF69-5001///	AM	N	C	I/F Cabinet upper
2	0CF69-5000///	AH	N	C	I/F Cabinet lower
3	0CF69-5021///	AB	N	C	Insulator
4	0CF69-5026///	AB	N	C	Leg For Cabinet
5	0CF69-0005///	AA	N	C	Screw (M3×6)
6	0CF69-0019///	AA	N	C	Screw (M3×6)

2 ELECTRONIC PARTS

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	VHiSN74LS00-1	AE		B	IC [IC4,IC9]
2	VHiSN74LS02-1	AE		B	IC [IC8]
3	VHiSN74LS04-1	AE		B	IC [IC6]
4	VHiSN74LS10-1	AE		B	IC [IC3]
5	VHiSN74LS30-1	AE		B	IC [IC7]
6	VHiSN74LS74AN	AG		B	IC [IC10]
7	VHiSN74LS138N	AG		B	IC [IC2]
8	VHiSN74LS541N	AP		B	IC [IC5]
9	VHi2732//AC88	BK	N	B	EP-Rom [IC1]
10	0CF69-5105///	AF	N	B	IC socket
11	0CF69-5103///	AM	N	C	Connector [T6]
12	0CF69-5104///	AT	N	C	Connector [T7]
13	0CF69-5095///	AC	N	C	Capacitor [C3]
14	0CF69-5092///	AC	N	C	Capacitor [C1~2,C4~9]
15	0CF69-5023///	AA	N	C	Screw

3 PACKING,INST.BOOK,OTHER

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	RMEMR1028AC73	BF	N	E	Master Disk
2	TiNSE1140ACZZ	BB	N	D	Instruction book (Disk basic) (Disk Basic)
3	TiNSE1215ACZZ	AL	N	D	Instruction Book(Installation)
4	TiNSE1216ACZZ	AP	N	D	Instruction book (QD Basic)
5	TSELF1002ACZZ	AA		D	Label
6	SPAKA1467ACZZ	AM	N	D	Packing Cushion
7	SPAKC1562ACZZ	AT	N	D	Packing Case
8	SSAKA0001SCZZ	AA		D	Poly Bag(Instruction Book)
9	SSAKA0302CCZZ	AA		D	Poly Bag(I/F unit)
10	SSAKB0002YDE0	AA		D	Poly Bag(Media)
11	QCNW-1105ACZZ	AK	N	C	Cable for CMT



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