SHARP SERVICE MANUAL

CODE : 00ZMZ1E05//-E

MINI FLOPPY DISK INTERFACE

MODEL-MZ1E05

FOR MZ-700 MFD I/F BOARD

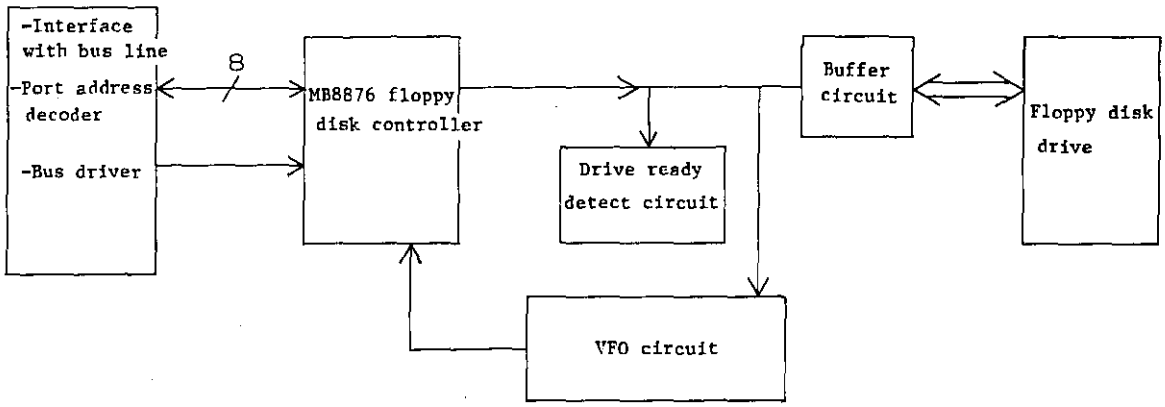
CONTENTS

SHARP CORPORATION

Introduction

This interface PWB is used to connect the MZ1F02 Floppy Disk Drive to the MZ-700 Series Personal Computer via the MZ-1U06 Expansion Box.

1. Block diagram



$SD8 thru $SDF are used for the port addresses.

(1) This section interfaces the data transferred between the CPU and the Floppy Controller (FDC).

(2) This section controls the Floppy Disk Drive (FDD) and for data transfer between the CPU and the FDD.

(3) This section detects the ready state of the FDD to inform it to the FDC.

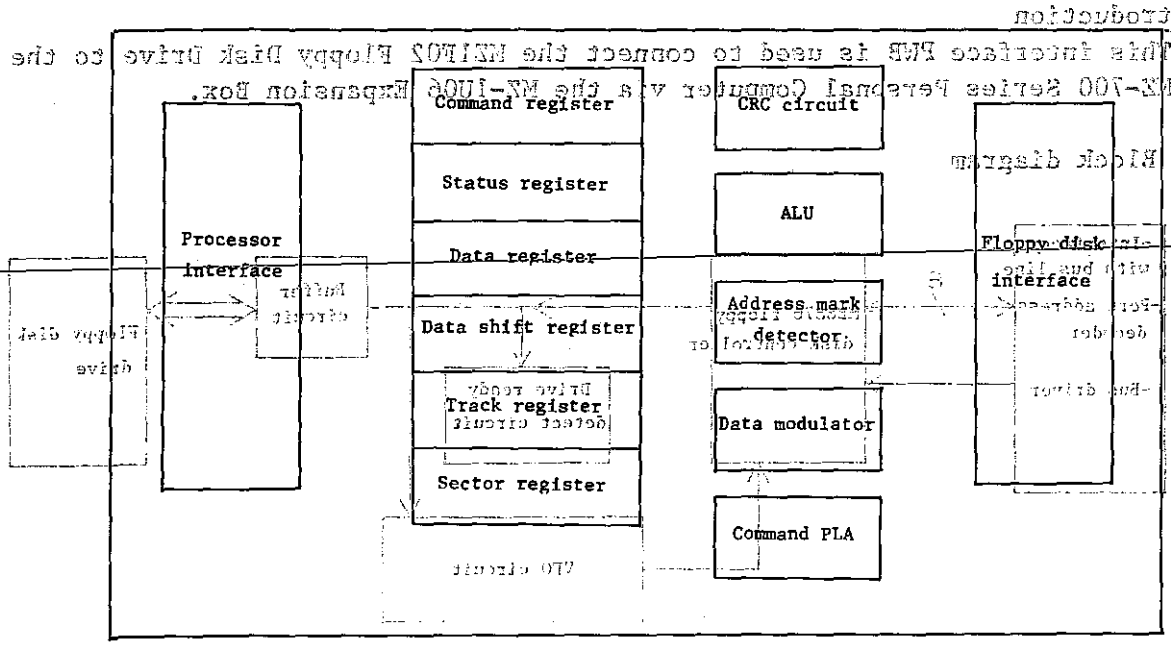
(4) This section is the variable frequency oscillator circuit through which the FDC receives the read data from the FDD.

(5) This section is the buffer (driver) circuit for data and control signals between the FDC and the FDD.

2. Description of the MB8876 Floppy Disk Controller

It is the LSI which intervenes between the floppy disk drive and the processor to transfer read and write data and to control mechanical section and to detect control signals.

2-1. Block diagram



2-2. Description of blocks

1) Command register

Used to send the operational command from the processor to the FDC.

2) Status register

Read only register used to indicate the internal state of the FDC, process status during command execution, and the state of the disk drive.

3) Data register

Data read from the disk is stored in this register during the disk read or data stored in the register is written on the disk during the disk write.

4) Data shift register

During disk write, the data sent parallel from the data register are modulated in the FM or MFM mode as the write data, then sent out serial from the WD terminal.

5) Track register

The contents of this register is reduced from FFH after master reset and becomes 00H when $\overline{TR00}$ reaches low level. Normally, the disk read/write head location is set in this register.

6) Sector register

For the read data and write data commands, the sector number in the ID field read from the disk is compared with the contents of this register. When they match, read/write is enabled to that sector.

7) CRC circuit
The Cyclic Redundancy Check circuit (CRC) is used to check a data error in reading or writing serial data from/to the disk.

8) ALU circuit
As the Arithmetic Logical Unit (ALU) compares serial data, increment it (+1), decrement it (-1), and through (±0), it is used to revise, compare, and verify the register contents.

9) Address mark detect circuit
It is used to detect the data that has a specific bit pattern in the serial bit cell where the data read from the disk are contained. Such as the index mark, ID address mark, data mark, and deleted mark are detected.

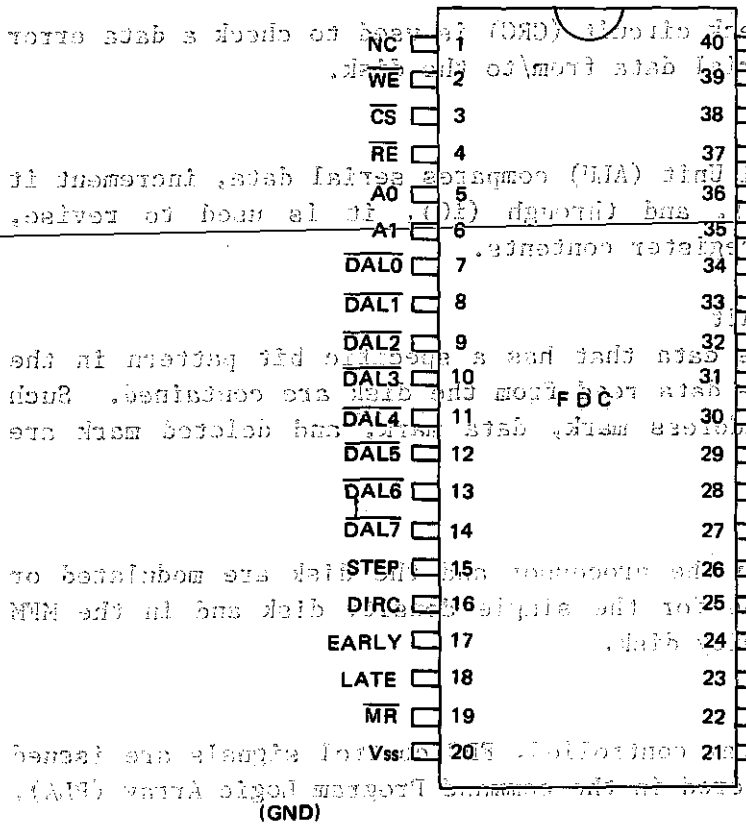
10) Data modulator
Data transferred between the processor and the disk are modulated or modulated in the FM mode for the single density disk and in the MFM mode for the double density disk.

11) Command PLA
As the FDC is microprogram controlled, FDC control signals are issued from the microprogram stored in the command Program Logic Array (PLA).

12) Processor interface
It is the interface used to perform data transfer between the FDC internal register and the processor. The processor transfers data and command to the FDC internal register via this interface. Signal lines of this interface consists of data lines, register select lines, read line, write line and chip select line.

13) Floppy disk interface
As the floppy disk interface, the FDC has the disk read/write head drive signal line, disk data read line, disk data write line, and FD status sense line.

2-3. Pin configuration



2-4. Signal description

Pin No.	Signal name	Symbol	I/O	Function
20	POWER SUPPLIES	VSS	In	Ground
21		VCC	In	+5V
19	MASTER RESET	$\overline{MR}$	In	Becomes active with MR=0, and it resets all STR 7 bits and stores 01H in the SCR and 03H in the CR. The restore command becomes active at a low to high transition of MR.
Computer interface				
2	WRITE ENABLE	$\overline{WE}$	In	Internal register data write strobe input line. Write is done with $\overline{CS}$=0 and $\overline{WE}$=0.
3	CHIP SELECT	$\overline{CS}$	In	Chip select. Chip is selected with $\overline{CS}$=0 and allows data transfer with the computer.

Pin No.	Signal name	Symbol	I/O	Function
4	READ ENABLE	$\overline{RE}$	In	Internal register data read strobe input line. Read is done with $\overline{CS}$=0 and $\overline{RE}$=0.
5 6	REGISTER SELECT LINE	A0 A1	In	Internal register select input. The registers selective as CR, STR, TR, and DR.
7 〜 14	DATA ACCESS LINE	$\overline{DAL0}$ $\overline{DAL7}$	In/ Out	Bidirectional 8-bit data input/output pins. High impedance when $\overline{CS}$=1. Signal polarity is inverted (negative logic).
24	CLOCK	CLK	In	2-MHz basic clock input. 1 MHz in the case of a mini-floppy disk.
38	DATA REQUEST	DRQ	Out	Open drain type output. During read, DR indicates byte data full. During write, DR indicates byte data empty and so data is requested. DRQ is set when write or read is executed. Must be connected with a 10 Kohms pullup resistor.
39	INTERRUPT REQUEST	IRQ	Out	Open drain type output. IRQ=1 occurs at a command termination, interruption, or at an occurrence of type IV command interrupt. Reset at write of a next command or read of STR. A 10 Kohms pullup resistor is connected.
Floppy disk interface				
15	STEP	STEP	Out	Creates step pulse to move the head. One pulse moves the head one step.
16	DIRECTION	DIRC	Out	Indicates head moving direction. The head moves outward with DIRC=0 and inward with DIRC=1.
17	EARLY	EARLY	Out	Write precompensation output. When EARLY=1, it indicates that the serial data output from WD must be shifted to the faster one.
18	LATE	LATE	Out	Write precompensation output. When LATE=1, it indicates that the serial data output from WD must be shifted to the slower one.

Pin No.	Signal name	Symbol	I/O	Function
22	TEST	$\overline{TEST}$	In	Test pin used during manufacture of the LSI.
23	HEAD LOAD TIMING	HLT	In	Head settle time input after the issuance of a head load command. In the aging condition with HLT=1.
25	READ GATE	RG	Out	With RG=1, it indicates the external data separator the FDC detected the field that contains "0" only (in the case of the FM mode) or the field that contains "0" or "1" only (in the case of the MFM mode). It is used for obtaining synchronization.
26	READ CLOCK	RCLK	In	Signal used to window the data which is created externally according to the flow of data and inputted to the FDC side. It rises in conjunction with $\overline{RAW\ READ}$. Falling edge is important regardless of its level (high or low).
27	RAW READ	$\overline{RAW\ READ}$	In	Raw data input directly from the disk drive. Used during data receive and the data is represented by a negative pulse.
28	HEAD LOAD	HLD	Out	Output used to determine whether the head should be pressed against the disk. With HLD=1, the head is pressed. With HLD=0, the head is released from the disk surface.
29	TRACK GREATER	TG43	Out	With TG43=1, it indicates that the head is over Track 44 thru 76. With TG43=0, it indicates that the head is over track 00 thru 43. This output is valid only for the read/write command.
30	WRITE GATE	WG	Out	Output which indicates that data has been written on the disk. WG=1 shows that data has been written.

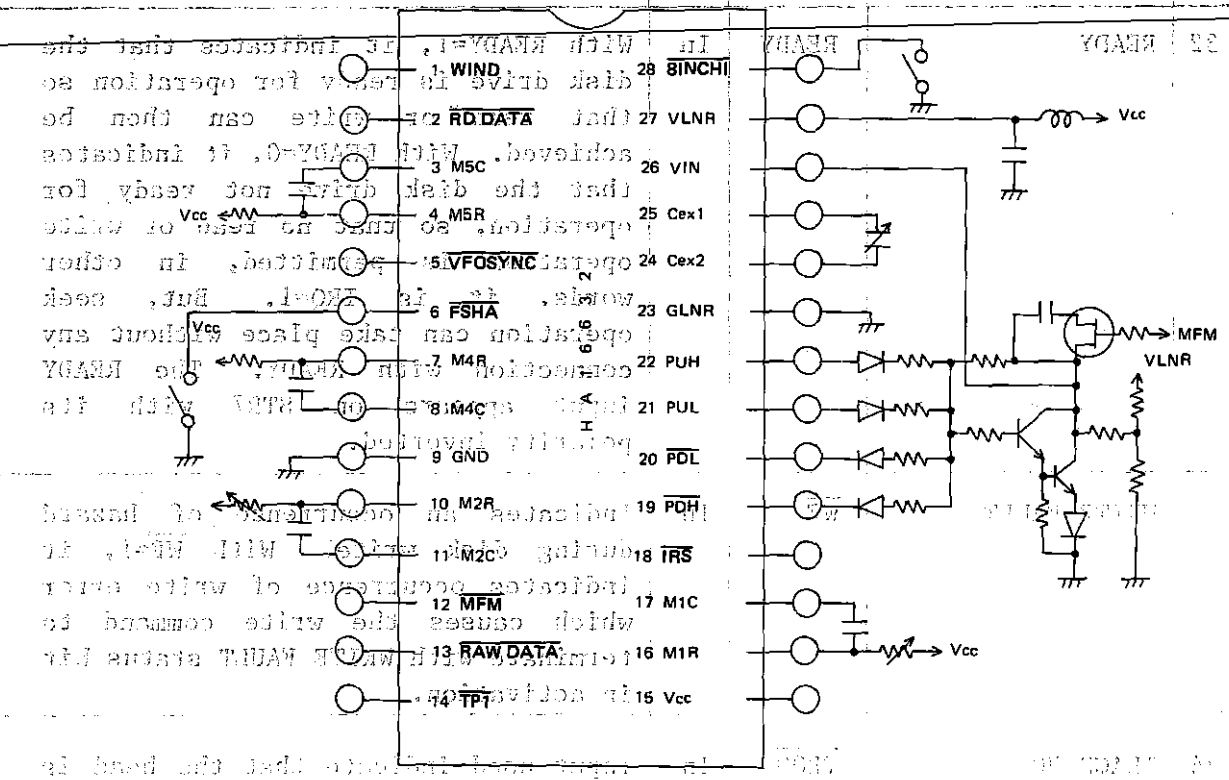
Pin No.	Signal name	Symbol	I/O	Function
31	WRITE DATA	WD	Out	Disk write data output line. It will be in a pulse width of 250 ns in the case of the MFM mode and 500 ns in the case of the MF mode. Regardless of FM and MFM, an address mark is also attached similar as data.
32	READY	READY	In	With READY=1, it indicates that the disk drive is ready for operation so that read or write can then be achieved. With READY=0, it indicates that the disk drive not ready for operation, so that no read or write operation is permitted, in other words, it is IRQ=1. But, seek operation can take place without any connection with READY. The READY input appears on STR7 with its polarity inverted.
33	WRITE FAULT	$\overline{WF}$	In	Indicates an occurrence of hazard during disk write. With $\overline{WF}$=1, it indicates occurrence of write error which causes the write command to terminate with WRITE FAULT status bit in activation.
34	TRACK 00	$\overline{TR00}$	In	Input used indicate that the head is over the track 00. With $\overline{TR00}$=0, it indicates that the track 00 is sensed.
35	INDEX PULSE	$\overline{IP}$	In	Input which indicates detection of a disk index hole. With $\overline{IP}$=0, it indicates detection of the index hole.
36	WRITE PROTECT	$\overline{WRPT}$	In	Input used to indicate that the disk is write protected. After initiation of the write command, $\overline{WPRT}$ is sampled at all times. The command is terminated with $\overline{WPRT}$=0 and the WRITE PROTECT status bit is therefore activated.
37	DOUBLE DENSITY	$\overline{DDEN}$	In	Input to indicate whether the disk is single or double density. $\overline{DDEN}$=0 indicates the double density disk and $\overline{DDEN}$=1 indicates the single density.
40 1	NON CONNECTION	NC		

3. Description of the VFO circuit

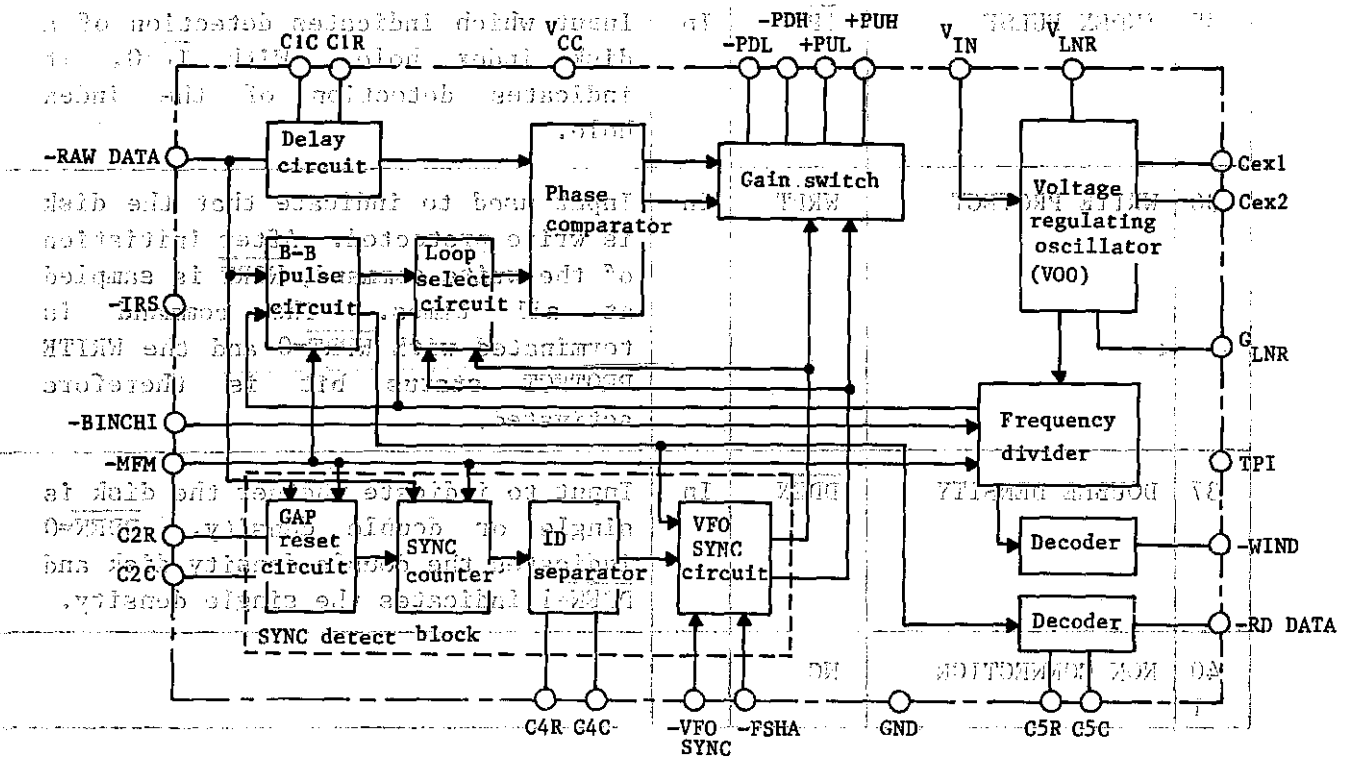
This circuit is used to create the WINDOW signal in synchronization with the read signal that contains motor noise of the floppy disk drive.

In the interface board, an exclusively dedicated IC is used for the VFO circuit.

3-1. VFO circuit diagram



3-2. Block diagram



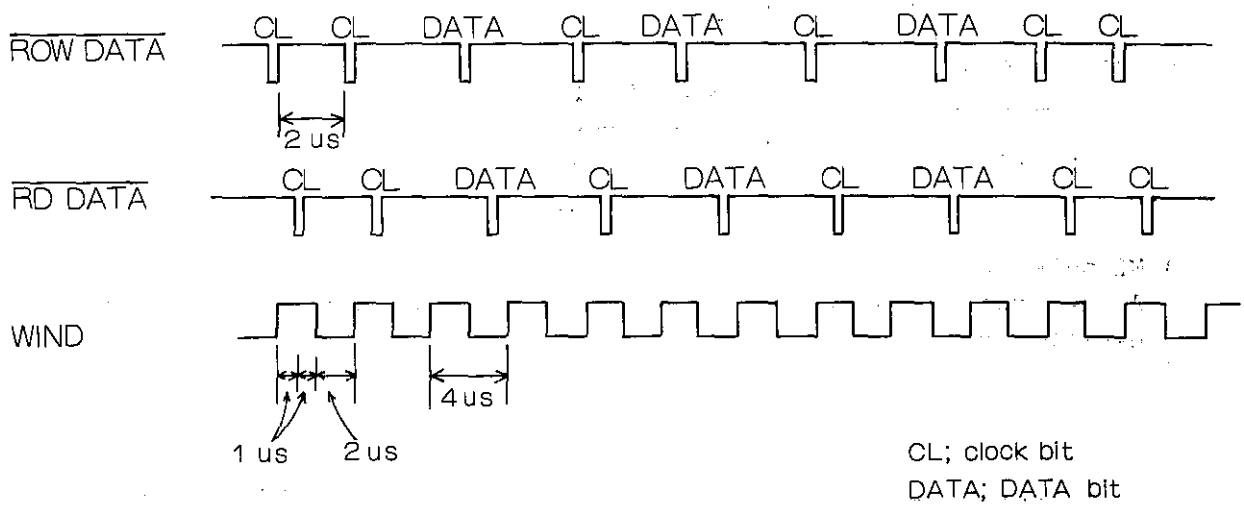
3-3. Description of the HA16632 VFO IC

Item	Pin name	Function	Note
Power supply	VCC	Power supplies except to the VCO block.	
	GND	Ground for blocks except to the VCO block.	
	VLNR	Power supply to the VCO block.	
	GLNR	Ground for the VCO block.	
Input signal	$\overline{\text{RAW DATA}}$	Raw read data from the floppy disk. Consists of (1) clock signal and (2) data signal.	Clock and data signals
	$\overline{\text{VFO SYND}}$	Input to indicate detection of a SYNC byte. With the low state of $\overline{\text{FSHA}}$, gain is switched for loop trap. $\overline{\text{VFO SYNC}}$=low: sync byte detected. $\overline{\text{VFO SYNC}}$=high: sync byte not detected.	
	$\overline{\text{MFM}}$	Input to select data recording method. $\overline{\text{MFM}}$=low: MFM mode MFM=high: FM mode	
	$\overline{\text{8 INCH}}$/(-VCO)	1. Input to select the floppy disk type; 8" floppy disk or 5" floppy disk. (When IRS=high) $\overline{\text{8 INCH}}$=low: 8" FDD 8 INCH=high: 5" FDD 2. VCO oscillator output monitor signal When -IRS=low	
	$\overline{\text{FSHA}}$	Input to select the floppy disk controller type. $\overline{\text{FSHA}}$=low: MB8876 or 8877 FSHA=high: UPD765AC	
	$\overline{\text{IRS}}$	IC test pin $\overline{\text{IRS}}$=high: IC used on board IRS=low: IC in test	
	VIN	VCO oscillation frequency control voltage input	

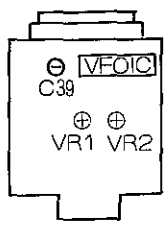
Item	Pin name	Function	Note
Output signal	WIND/(+MIQ)	1. WIND output for identifying the clock signal from the data signal contained in RAW DATA. +WIND=high: Clock signal +WIND=low: Data signal (When $\overline{IRS}$=high)	
		2. One-shot monomultivibrator output M1 monitor pin (When $\overline{IRS}$=low)	
	$\overline{RD\ DATA}$/(+M2Q)	1. Shaped read data output (When $\overline{IRS}$=high)	
		2. One-shot monomultivibrator output M2 monitor pin (When $\overline{IRS}$=low)	
	$\overline{PDL}$	Charge pump down output in low gain (data loop)	
	$\overline{PDH}$	Charge pump up output in high gain (data loop)	
	PUL	Charge pump down output in low gain (sync loop)	
	PUH	Charge pump up output in high gain (sync loop)	
	TPI	IC test pin $\overline{IRS}$=high: Loop select circuit output monitor $\overline{IRS}$=low: VFO SYNC circuit output monitor	
Resistor/ capacitor connection pin	C1R	One-shot monomultivibrator M1 resistor and capacitor connection	
	C1C	One-shot monomultivibrator M1 capacitor connection	
	C2R	One-shot monomultivibrator M2 resistor and capacitor connection	
	C2C	One-shot monomultivibrator M2 capacitor connection	
	C4R	One-shot monomultivibrator M4 resistor and capacitor connection	
	C4C	One-shot monomultivibrator M4 capacitor connection	

Item	Pin name	Function	Note
Resistor/ capacitor connection pin	C5R	One-shot monomultivibrator M5 resistor and capacitor connection	
	C5C	One-shot monomultivibrator M5 capacitor connection	
	CEX1	VCO capacitor connection	
	CEX2	VCO capacitor connection	

3-4. Timings (with data "01010" in the MFM mode)



3-5. VFO circuit adjustments

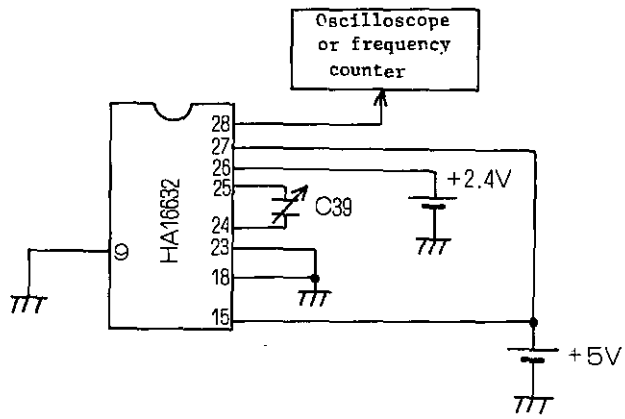


Adjust the VFO using C39, VR1 and VR2.

C39: Trimmer capacitor
VR1/VR2: Variable resistor

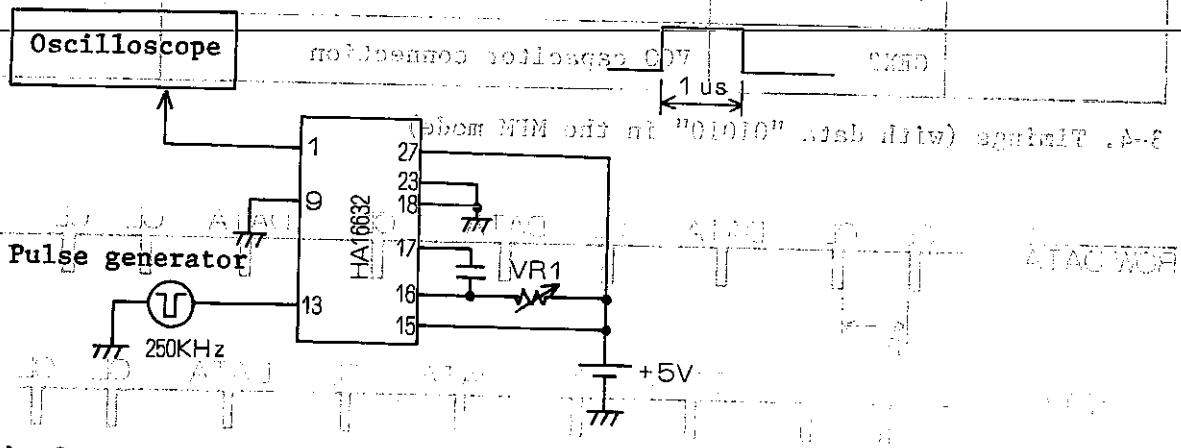
a) VCO oscillation frequency

Adjust C39 so that the oscillation frequency of 4 MHz ±50 kHz is obtained.



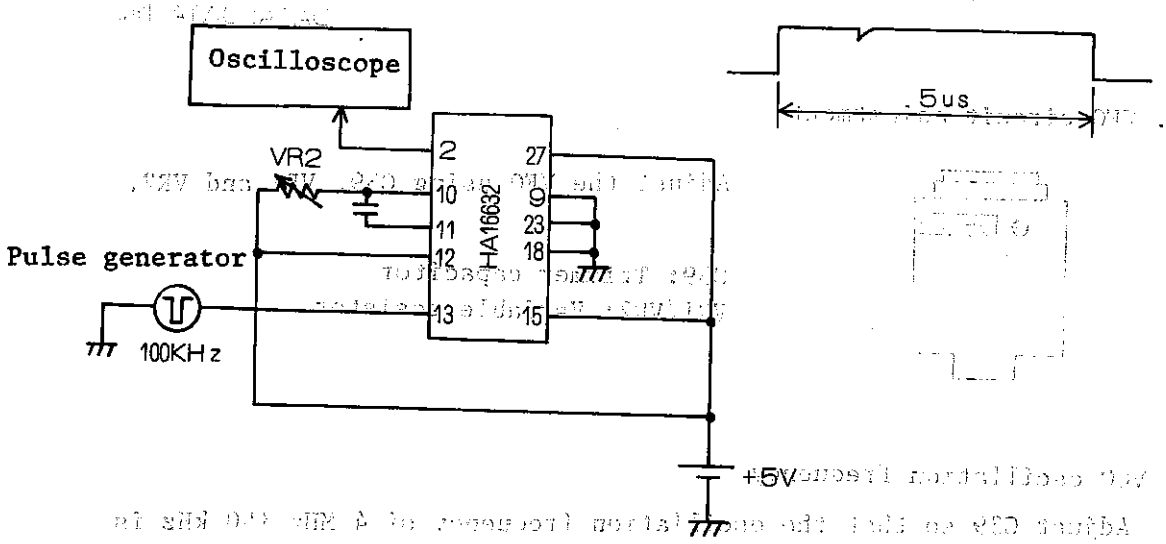
b) M1 pulse width

Adjust the VR1 so that the following waveform should be seen on the oscilloscope.

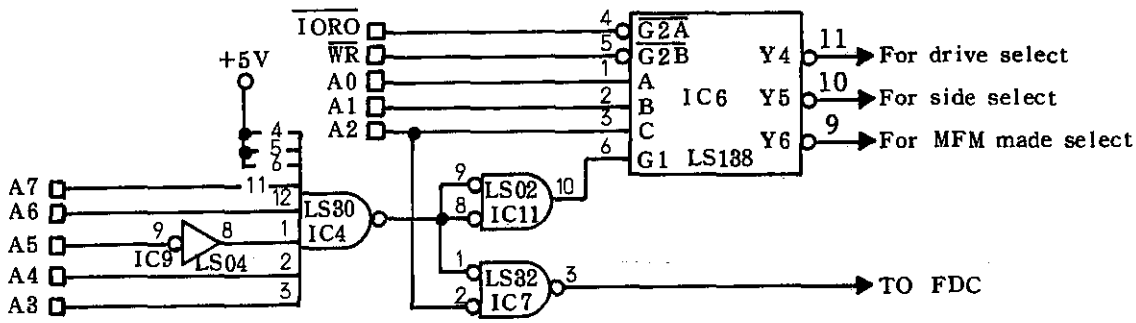


c) M2 pulse width

Adjust the VR2 so that the following waveform should be seen on the oscilloscope.



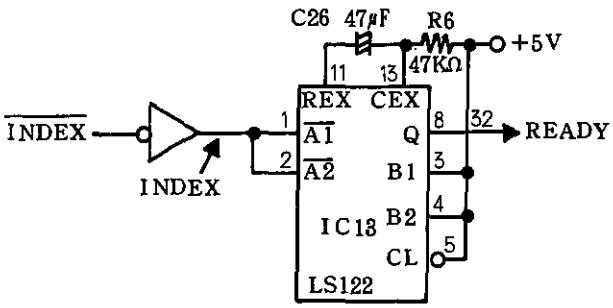
4. Port address select circuit



Port address table

A7	A6	A5	A4	A3	A2	A1	A0	Selection
1	1	0	1	1	0	X	X	FDC
(D)				(8~B)				
1	1	0	1	1	1	0	0	Drive
(D)				(C)				
1	1	0	1	1	1	0	1	Side
(D)				(D)				
1	1	0	1	1	1	1	0	MFM mode
(D)				(E)				

5. Ready circuit



Because the ready signal is not issued from the FDD, $\overline{\text{READY}}$ is derived from $\overline{\text{INDEX}}$ through the monomultivibrator IC. After motor on, $\overline{\text{INDEX}}$ appears. As soon as the motor reaches the operating revolutions, it becomes a pulse of about 200 ms which cause the ready signal to be active.

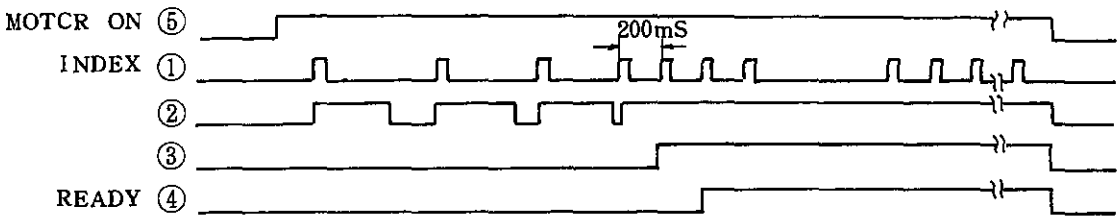
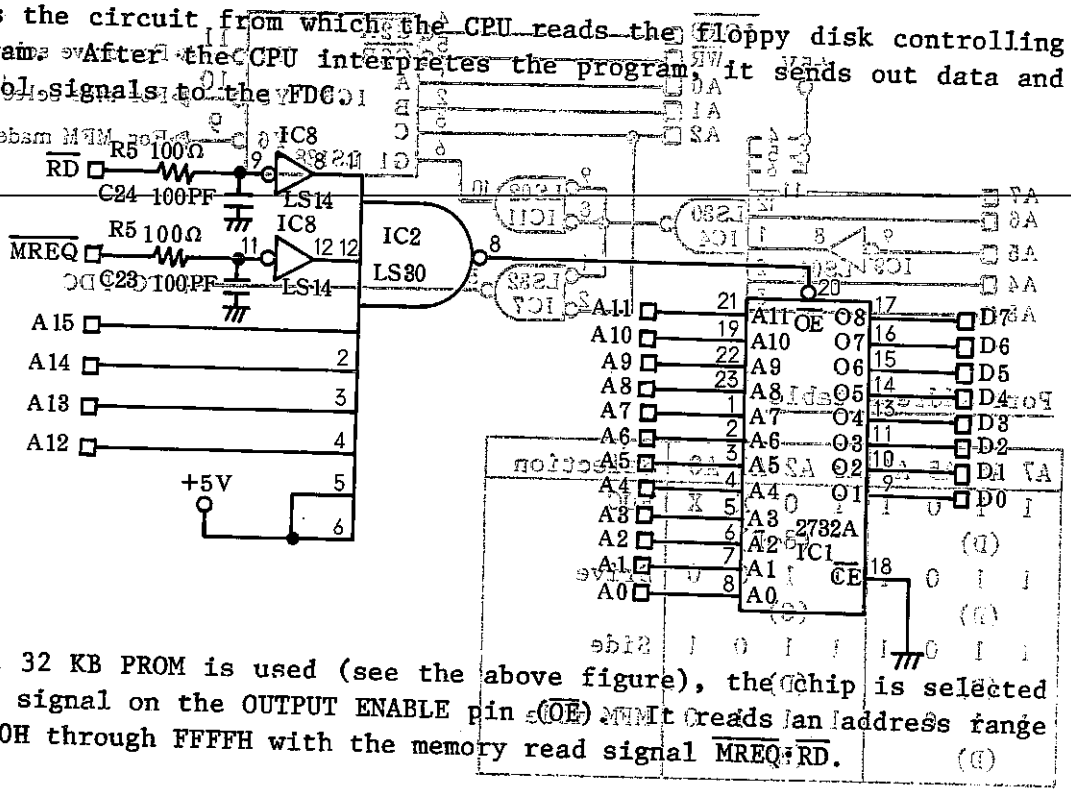


Fig.2 READY signal timing

6. PROM select circuit

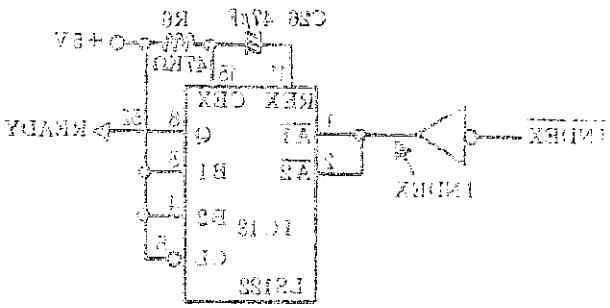
It is the circuit from which the CPU reads the floppy disk controlling program. After the CPU interpretes the program, it sends out data and control signals to the FDC.



As the 32 KB PROM is used (see the above figure), the chip is selected by the signal on the OUTPUT ENABLE pin ($\overline{OE}$). It reads an address range of F000H through FFFFH with the memory read signal $\overline{MREQ}$·$\overline{RD}$.

7. Ready circuit

Because the ready signal is not issued from the FDD, $\overline{READY}$ is derived from $\overline{INDEX}$ through the monomultivibrator IC. After motor on, $\overline{INDEX}$ appears. As soon as the motor reaches the operating revolutions, it becomes a pulse of about 200 ms which causes the ready signal to be active.



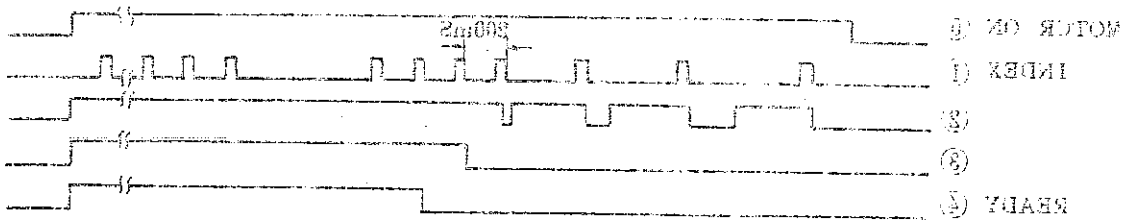
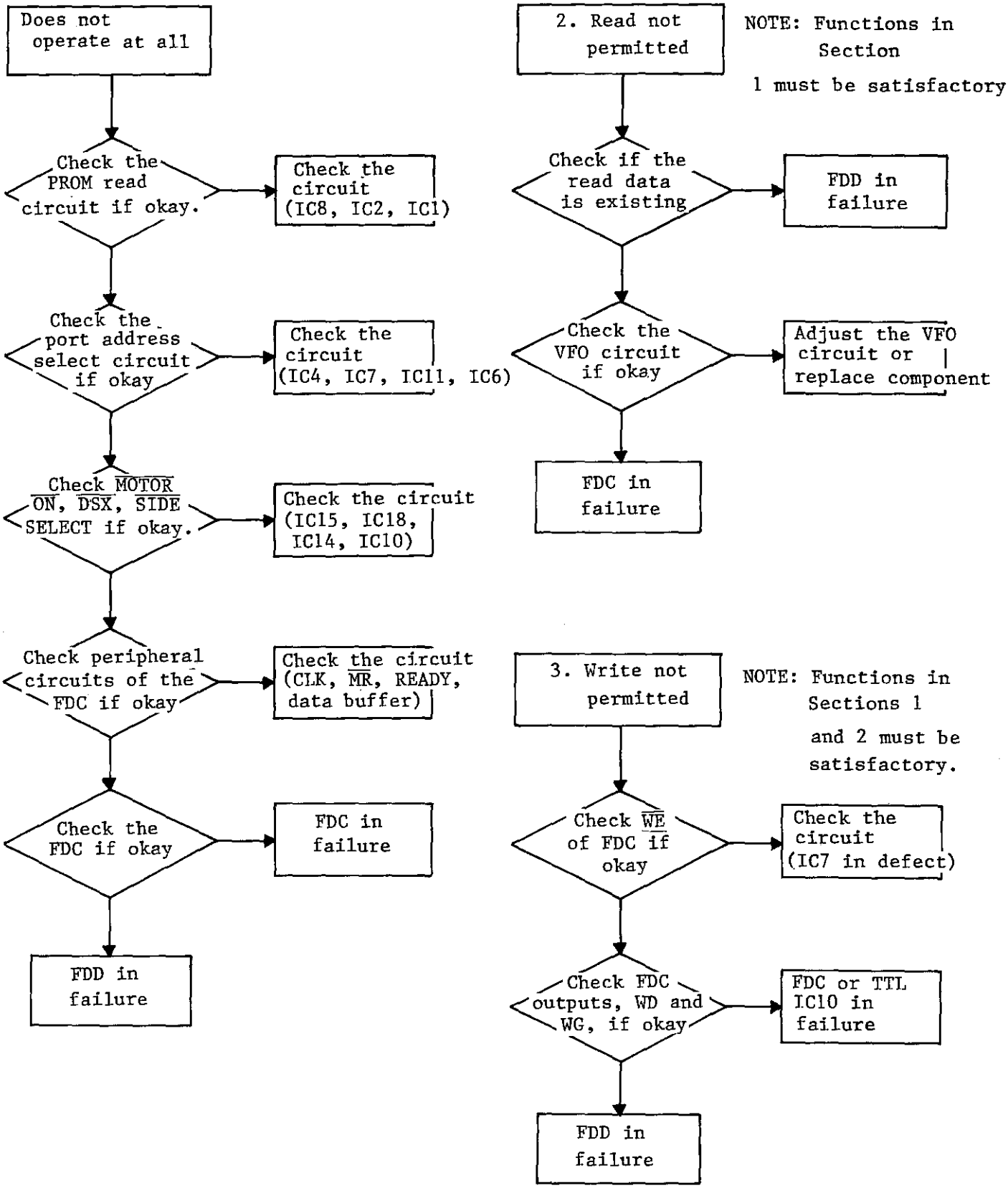
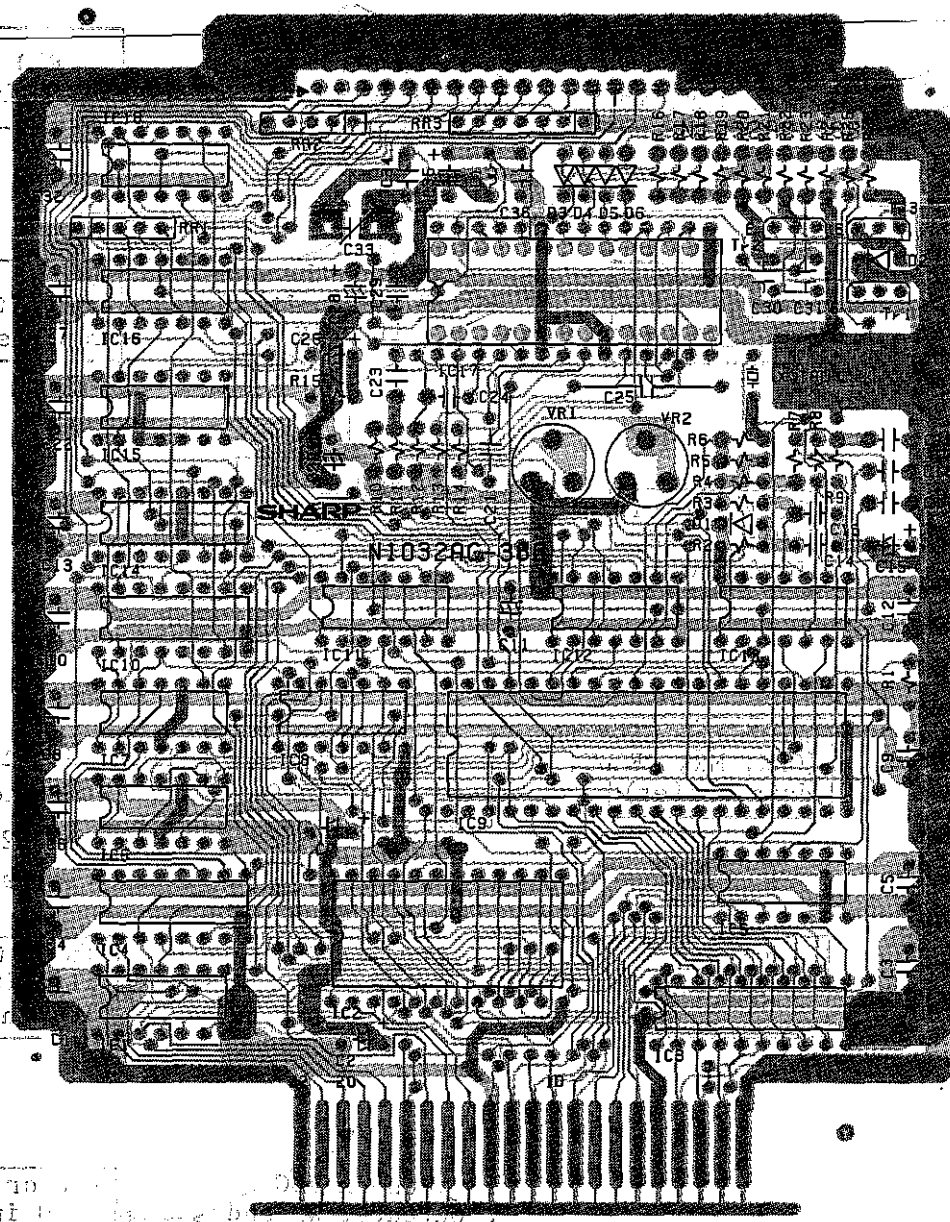


Fig.2 READY signal timing

7. Trouble shooting



8. Parts position



1 Electronic parts

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	QCNCW1031ACZZ	AX	N	C	Connector
2	QSOCZ6424ACZZ	AE		C	IC socket (24pin)
3	QSOCZ6428ACZZ	AE		C	IC socket (28pin)
4	RC-KZ1026CCZZ	AF		C	Capacitor
5	RCiLL1001ACZZ	AC		C	Coil
6	RCRS-0004MCZZ	AN		C	(4MHz)
7	RMPTC4102QCKB	AC		B	Block resistor (1.0KΩ×4 1/8W ±10%)
8	RMPTC4472QCKB	AC		B	Block resistor (4.7KΩ×4 1/8W ±10%)
9	RMPTC6472QCKB	AC		B	Block resistor (4.7KΩ×6 1/8W ±10%)
10	RVR-M1414QCZZ	AD		B	Variable resistor SR19R 10KΩ
11	VCCCPU1HH120J	AA		C	Capacitor (50WV 12pF)
12	VCCCPU1HH680J	AB		C	Capacitor (50WV 68PF)
13	VCCCPU1HH750J	AA	N	C	Capacitor (50WV 75PF)
14	VCEAAA1CW106Q	AB		C	Capacitor (16WV 10μF)
15	VCEAAU1AW107Q	AB		C	Capacitor (10WV 100μF)
16	VCSATU0JE476M	AB		C	Capacitor (16WV 47μF)
17	VCKYPU1HB101K	AA		C	Capacitor (16WV 101pF)
18	VCKYPU1HF223Z	AA		C	Capacitor (50WV 0.022μF)
19	VCQSTT2TS511J	AD		C	Capacitor (150WV 510pF)
20	VCQYKU1HM102K	AA		C	Capacitor (50WV 1000pF)
21	VCQYKU1HM682K	AB		C	Capacitor (50WV 6800pF)
22	VCQYKU1HM683K	AB		C	Capacitor (50WV 0.068μF)
23	VCSATU1CE226K	AE		C	Capacitor (16WV 22μF)
24	VCSATU1VE106M	AE		C	Capacitor (35WV 10μF)
25	VCTYPA1NX104M	AB		C	Capacitor (12WV 0.10μF)
26	VHDLS1588L1-1	AB		B	Diode (1S1588L1)
27	VHiHA16632AP1	BH		B	IC
28	VHiMB8876A/-1		N	B	IC
29	VHiM74LS02/-1	AE		B	IC (M74LS02P)
30	VHiM74LS04/-1	AE		B	IC (M74LS04P)
31	VHiM74LS138-1	AK		B	IC (M74LS138P)
32	VHiM74LS14/-1	AM		B	IC (M74LS14P)
33	VHiM74LS175-1	AG		B	IC (M74LS175P)
34	VHiM74LS245-1	AM		B	IC (M74LS245P)
35	VHiM74LS30/-1	AE		B	IC
36	VHiM74LS32/-1	AF		B	IC (M74LS32P)
37	VHiM74LS74/-1	AG		B	IC (M74LS74P)
38	VHiSN74LS122N	AH		B	IC (SN74LS122N)
39	VHiSN74145N-1	AN		B	IC (SN74145N)
40	VHiSN7416N/-1	AF		B	IC
41	VRD-ST2EY101J	AA		C	Resistor (1/4W 100Ω ±5%)
42	VRD-ST2EY103J	AA		C	Resistor (1/4W 10KΩ ±5%)
43	VRD-ST2EY122J	AA		C	Resistor (1/4W 1.2KΩ ±5%)
44	VRD-RV2EY153J	AA		C	Resistor (1/4W 15KΩ ±5%)
45	VRD-ST2EY221J	AA		C	Resistor (1/4W 220Ω ±5%)
46	VRD-ST2EY472J	AA		C	Resistor (1/4W 4.7KΩ ±5%)
47	VRD-ST2EY473J	AA		C	Resistor (1/4W 47KΩ ±5%)
48	VRD-ST2EY560J	AA		C	Resistor (1/4W 56Ω ±5%)
49	VRD-ST2EY561J	AA		C	Resistor (1/4W 560Ω ±5%)
50	VRN-RT2EK101F	AB		C	Resistor (1/4W 100Ω ±2%)
51	VRN-RT2EK102F	AB		C	Resistor (MR25 1KΩG)
52	VRN-RT2EK103F	AB		C	Resistor (1/4W 10KΩ ±2%)
53	VRN-RT2EK221F	AA		C	Resistor (1/4W 220Ω ±1%)
54	VRN-RT2EK223F	AB		C	Resistor (1/4W 22KΩ ±1%)
55	VRN-RT2EK331F	AB		C	Resistor (1/4W 330Ω ±2%)
56	VRN-RT2EK471F	AB		C	Resistor (1/4W 470Ω ±2%)
57	VRN-RT2EK513F	AB		C	Resistor (1/4W 51KΩ ±1%)
58	VS2SC641KC/-1	AE		B	Transistor
59	VS2SK168-//-1	AD		B	FET
60	LANGT1049ACZZ	AE		C	Angle for PWB

2 Packing and accesory

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	QCNW-1038ACZZ	BN		C	Cable
2	SPAKA1346ACZZ	AH		D	Packing cushion for unit
3	SPAKA1380ACZZ	AB		D	PAD
4	SPAKC1347ACZZ	AK		D	Packing case
5	TiNSE1097ACZZ	AD		D	Instruction manual
6	TLABN1235ACZZ	AA		D	Label
7	TSELF1002ACZZ	AA		D	Seal

SHARP

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