MZ-5500/5600

TECHNICAL REFERENCE

Vol.2 (HARDWARE)

SHARP CORPORATION

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SECTION ONE
System Specifications

1. Introduction

The MZ-5500 series is the first 16-bit MZ series personal computer in which the Intel's 8086 is used for the CPU.

It has been designed with intense care for man-machine interface: the mouse, the bit map display system, and the multiwindow display function are introduced to the MZ-5500 series.

It has the system RAM area of 128KB (MZ-5511) or 256KB (MZ-5521) as standard and it can also be expanded to 512KB at a maximum.
The 96KB video RAM area is provided standard and it also can be expanded to 192KB, permitting clear color graphic displaying.
Up to two units of 320KB (formatted) mini-floppy disk drives can be internally installed, and the OS (Operating System) is contained in the 5.25" disk media. The OS supports CP/M-86 and MS-DOS as option.
Not only the MZ-5600 series succeeds all functions and features from the MZ-5500 series, but, it also permits the following external memory expansion and higher processing speed.

1) 8MHz/5MHz selective for operation of the 8086-II CPU.
2) Implementation of the 640KB (formatted), 5.25" floppy disk drive.
3) Use of the 10.7MB (formatted), 5.25" hard disk (MZ-5645).

Not only the MZ-5645 has one unit of the internal hard disk drive, it also enhances expansion to 21.4MB when the MZ-1F18 external hard disk drive is added (applicable for the 200V version only).
The MZ-5600 enables absorption of the software created on the MZ-5500 series.
Since the 8086-II is adopted, improvement has been achieved for higher processing speed and graphic speed, and consideration is given for the real time processing of the software developed on the MZ-5500 in the 5MHz mode.
Such as CP/M-86, MS-DOS, MZ-3500 series BASIC, and GW-BASIC are available as option.
Because the MZ-5600 series is a up-graded model for the MZ-5500 and has been developed on the basis of MZ-5500 peripherals and software, consideration has been given for compatibility in basic terms.
See Table-1 for individual model configurations of the MZ-5500 series and MZ-5600 series.

1-1 MZ-5500 SERIES HARDWARE DESCRIPTION

System configuration

The following figure shows the complete system configuration for the MZ-5500 Series system, including some peripheral devices which are to be marketed in the near future.

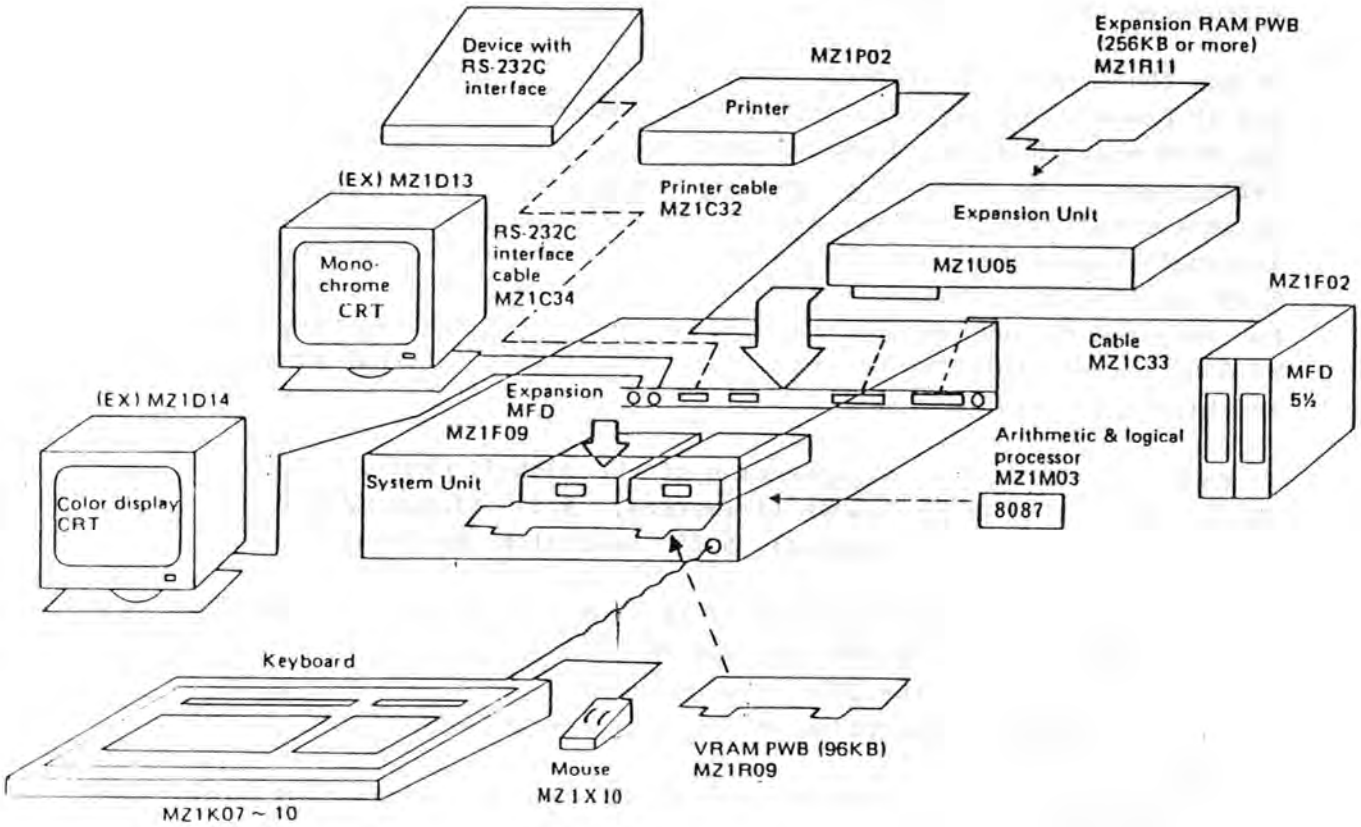


Fig. 1

Specifications

System highlights

1) High data processing capability achieved with a 16-bit microprocessor.
2) Large addressable memory space of 512KB: Standard 256KB plus an additional 256KB.
3) High-resolution color graphic display with large-capacity video screen memory and bit-map display.
4) One or two mini-floppy disk drives, each of 320KB are provided as a standard feature.
5) Powerful standard I/O system interface.
6) Integrated sound generator.
7) CP/M86 as the standard operating system.

Model description

Model	Description
MZ-5511	Contains one MFD plus 256KB of RAM.
MZ-5521	Contains two MFD's plus 256KB of RAM.

1-2 MZ-5600 SERIES HARDWARE DESCRIPTION

System configuration

The following figure shows the complete system configuration for the MZ-5600 Series system, including some peripheral devices which are to be marketed in the near future.

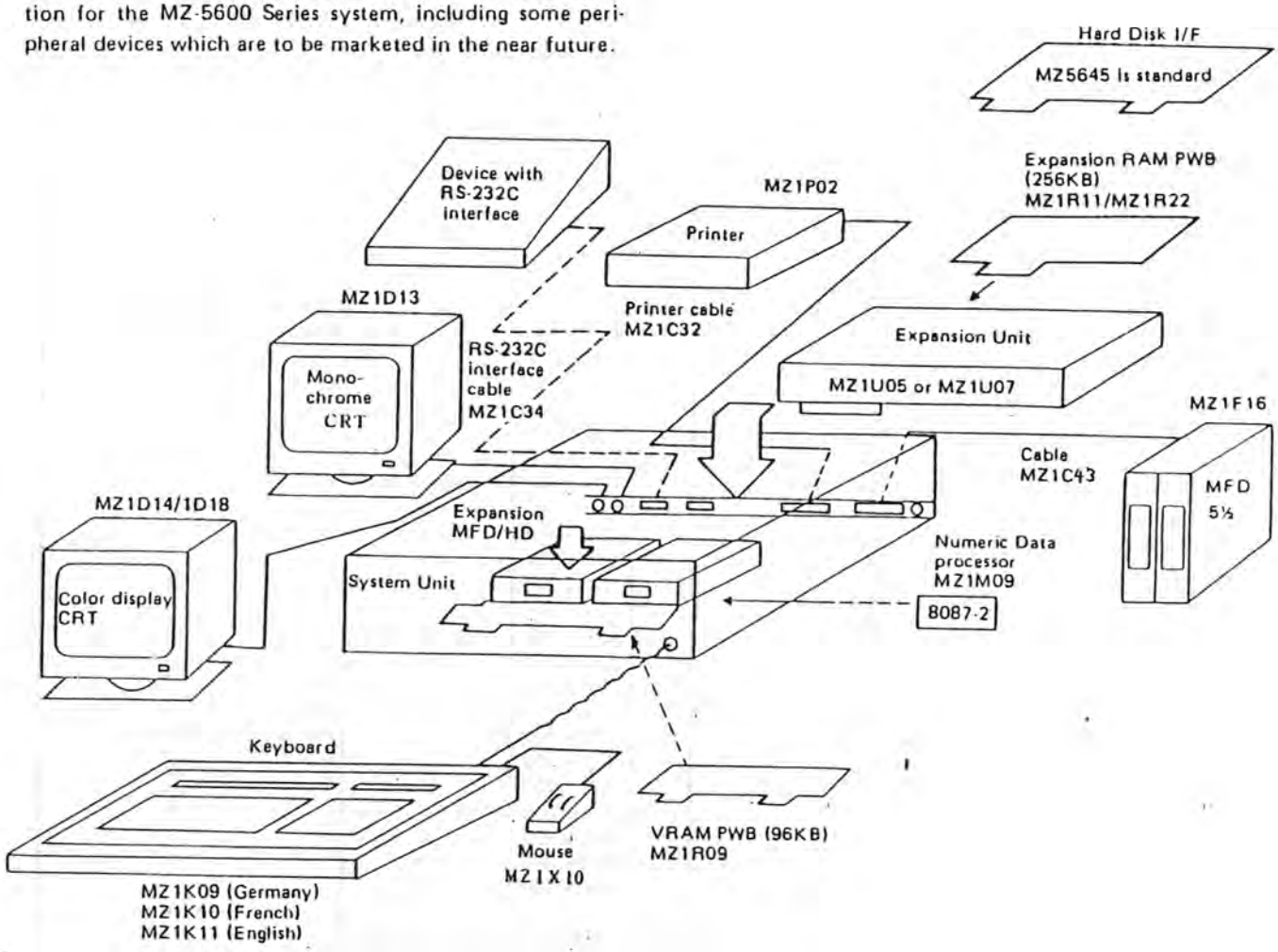


Fig. 2

Specifications

System highlights

1) High data processing capability achieved with a 16-bit microprocessor.
2) Large addressable memory space of 512KB: Standard 256KB plus an additional 256KB.
3) High-resolution color graphic display with large-capacity video screen memory and bit-map display.
4) One or two mini-floppy disk drives, each of 640KB are provided as a standard feature. And the MZ5645 is 10.7MB Hard disk is standard.
5) Powerful standard I/O system interface.
6) Integrated sound generator.
7) CP/M86 as the standard operating system.

Model description

Model	Description
MZ-5631	Contains one MFD plus 256KB of RAM
MZ-5641	Contains two MFD's plus 256KB of RAM
MZ-5645	Contains one MFD and one HD plus 256KB RAM

Specification of Disk

Item	HD	MFD
No. of side/drive	1	2
Tracks/side	673	40
Bytes/sector	512	256
Sectors/track	16	16
Total Bytes/Drive	5513216	327680
Bytes/block	4096	2048

1-3 MZ-5500 specification

Item		Std./Opt.					Description
CPU		Std. Opt. Std.	8086 8087 80C49	Arithmetic and logic processor. For keyboard control.			
MEMORY	ROM	Std.	IPL	16KB			
	RAM	Std Std Opt. Opt.	SYSTEM VRAM SYSTEM VRAM	256KB 96KB 256KB 96KB			Installed in the Expansion Unit. Available by a RAM PWB.
DISPLAY	I/F		Monochrome Color	Composite signal R.G.B.V.H SYNC			
	Display scheme			Bit map display			
	Screen configuration by system soft ware (CPM III)	Std.	Resolution Pages		Resolution	Number of pages	
				B/W	640 x 400 640 x 200 320 x 200	3 6 8	
				C	640 x 400 640 x 200 320 x 200	6 8 8	
		Opt.		B/W	640 x 400 640 x 200 320 x 200	4 4 4	When optional VRAM is installed.
				C	640 x 400 640 x 200 320 x 200	2 4 8	
	Color			8 colors (can be specified for each dot)			
	Gradation			8 gradations available with the dedicated monitor.			Available on a monochrome monitor (1D13) with a 640 x 400 matrix.
	Screen/character configuration		Display capacity Character cell	40 or 80 characters on each row. The number of rows per screen is programmable. 8 x 8, 8 x 16			Controlled by software.
	Screen control		Superimposed Multi-window Scroll Reduction/ expansion Palette feature Background color Color priority Reverse video Boundary color	3 pages 4 windows Character scroll Smooth scroll Software control 8 colors available Can be specified for each window. Planes with order of priority. Reversible for each window.			Horizontal or vertical direction. Vertical direction only. 8 colors Available on all color models other than the 640 x 400 dot model.

Item		Std./Opt.			Description
Integrated I/O interface	Sound	Std.		Three codes available through a built-in speaker.	
	Centronics I/F	Std.		One channel	For printer attachment
	Clock	Std.	Real-time clock	Backed up by battery.	Built-in 13 byte RAM
	MFD I/F	Std.		Capable of controlling up to 4 drives.	Two built-in drives plus two external drives
	RS-232C	Std.	A Channel	Start-stop asynchronous/sync.	Programmable between 110 and 9600 bauds.
		Std.	B Channel	Start-stop asynchronous.	
	Key I/F	Std.			Not used
	Cassette I/F	Std.			
OP I/O I/F	256KB RAM PWB	Opt.		Expansion RAM PWB.	
	HD I/F PWB	Opt.		Hard disk drive I/F PWB.	
	Expansion Unit	Opt.			
	SFD I/F PWB	Opt.		SFD I/F PWB.	MZ-1E11
Additional device	Mouse	Opt.		Attached to keyboard.	Available with the MZ-1X10
	MFD	Opt.	Single drive increment.	Additional drive to be installed in the System Unit.	Available with the MZ-1F09 For MZ5511 only
	MFD unit	Opt.	Contains two drives.	External drives	Available with the MZ-1F02.
	Hard disk unit	Opt.		10.7M Bytes	Available with the MZ-1F10
	SFD unit	Opt.	Contains two drives.	External drives	Available with the MZ-1F05
CRT	12" monochrome	Opt.		640 x 400 dot matrix	MZ-1D13
	12" color display	Opt.		640 x 400 dot matrix	MZ-1D14
	15" color display	Opt.		640 x 400 dot matrix	MX-1D18
Printer	80 columns	Opt.			MZ-1P02 MZ-1P07
	80 columns in color	Opt.			MZ-1P04

1-4 MZ-5600 specification

Item		Std./Opt.					Description
CPU		Std. Opt. Std.	8086-2 (8 MHz) 8087-2 (8 MHz) 80C49	Main Numeric data processor. For keyboard control.			
MEMORY	ROM	Std.	IPL	16KB (8KB x 2)			
	RAM	Std. Std. Opt. Opt.	SYSTEM VRAM SYSTEM VRAM	256KB 96KB 256KB 96KB			Installed in the Expansion Unit. Available by a RAM PWB.
DISPLAY	I/F		Monochrome Color	Composite signal R.G.B.V.H SYNC			
	Display scheme			Bit map display			
	Screen configuration by system soft ware (CPM III)	Std.	Resolution Pages		Resolution	Number of pages	
				B/W	640 x 400 640 x 200 320 x 200	3 6 8	
				C	640 x 400 640 x 200 320 x 200	6 8 8	
		Opt.		B/W	640 x 400 640 x 200 320 x 200	4 4 4	When optional VRAM is installed.
				C	640 x 400 640 x 200 320 x 200	2 4 8	
	Color			8 colors (can be specified for each dot)			
	Gradation			8 gradations available with the dedicated monitor.			Available on a monochrome monitor (1D13) with a 640 x 400 matrix.
	Screen character configuration		Display capacity Character cell	40 or 80 characters on each row. The number of rows per screen is programmable. 8 x 8, 8 x 16			Controlled by software.
	Screen control		Superimposed Multi-window Scroll Reduction/ expansion Palette feature Background color Color priority Reverse video Boundary color	3 pages 4 windows Character scroll Smooth scroll Software control 8 colors available Can be specified for each window. Planes with order of priority. Reversible for each window.			Horizontal or vertical direction. Vertical direction only. 8 colors Available on all color models other than the 640 x 400 dot model.

Item		Std./Opt.			Description
Integrated I/O interface	Sound	Std.		Three codes available through a built-in speaker.	
	Centronics I/F	Std.		One channel	For printer attachment.
	Clock	Std.	Real-time clock	Backed up by battery.	Built-in 13 byte RAM.
	MFD I/F	Std.		Capable of controlling up to 4 drives.	Two built-in drives plus two external drives.
	RS-232C	Std.	A Channel	Start-stop asynchronous/sync.	Programmable between 110 and 9600 bauds.
		Std.	B Channel	Start-stop asynchronous.	
	Key I/F	Std.			
OP I/O I/F	256KB RAM PWB	Opt.		Expansion RAM PWB.	
	HD I/F PWB	Opt.		Hard disk drive I/F PWB.	For MZ5631, MZ5641
	Expansion Unit	Opt.			MZ5645 is standard
	SFD I/F PWB	Opt.		SFD I/F PWB.	MZ-1E11
Additional device	Mouse	Opt.		Attached to keyboard.	Available with the MZ-1X10
	MFD	Opt.	Single drive increment.	Additional drive to be installed in the System Unit.	Available with the MZ-1F15 For MZ5631 only
	MFD unit	Opt.	Contains two drives.	External drives	Available with the MZ-1F16
	Hard disk unit	Opt.		10.7M Bytes	MZ1F10 External for MZ5631/5641 MZ1F18 External For MZ5645 only (200V system only) MZ1F14 Internal
	SFD unit	Opt.	Contains two drives.	External drives	Available with the MZ-1F05
CRT	12" monochrome	Opt.		640 x 400 dot matrix	MZ-1D13
	12" color display	Opt.		640 x 400 dot matrix	MZ-1D14
	15" color display	Opt.		640 x 400 dot matrix	MX-1D18
Printer	80 columns	Opt.			MZ-1P02

1-5 Optional devices specifications (for MZ-5500/5600)

• Green monitor MZ-1D13

Type	High resolution 12" monochrome video monitor for the MZ-5500/5600 Series.	
Specifications	CRT	12 inches, 90 deg. deflection
	Display capacity	640 dots horizontally by 400 rasters vertically
	Input signal	Composite signal of 1 Vp-p
	Supply voltage	Rated voltage
	Power consumption	*29 Watts
	Outer dimensions	313(W) x 289(H) x 327(D)mm
	Weight	6.2kg

• Color monitor MZ-1D14

Type	High resolution color video monitor for the MZ-5500/MZ-5600 Series	
Specifications	CRT	12 inches, 90 deg. deflection
	Display capacity	640 dots horizontally by 400 rasters vertically
	Video input signal	Independent RGB input of TTL level with positive polarity
	Sync. input	Independent H.V. sync. inputs of TTL level with negative polarity
	Supply voltage	Rated voltage
	Power consumption	*63 Watts
	Outer dimensions	326(W) x 288(H) x 375(D)mm
	Weight	11kg

• Expansion Unit MZ-1U07/1U05

Description	Used to install optional expansion PWBs or interface PWBs required to control optional peripheral devices which cannot be controlled with the interface contained in the MZ-5500/5600 Series System Unit. (MZ1U05 is 4 slots and MZ1U07 is 5 slots.)

• Expansion RAM PWB MZ-1R22/1R11

Description	Designed to be installed in the expansion Unit to add 256KB of additional RAM space. (MZ1R22 is used only SEEG)

• Expansion VRAM PWB MZ-1R09

Description	Provides an additional VRAM space of 96KB to increase the total VRAM area to 192KB for extended graphic capabilities.

* Mouse MZ-1X10

Description	A kind of pointing device. By moving it on the desk with your hand, you can move the cursor on the display. Used by connecting the cable directly to the connector on the rear of the MZ-5500/5600 series keyboard. For details, see 94.

* GPIO MZ-1E21

Description	The interface board which is designed to carry out information exchange in the parallel I/O mode between the MZ-5500/5600 series and peripherals. Needs the MZ-1U05/1U07 expansion unit to use.

• Printer

Model	Print system	Max. print speed	Character type	Character cell	Max. columns/row	Max. paper width/feed method	Copy capacity
MZ-1P02	Dot matrix impact printer	120cps	Alphanumeric, and symbolic, characters	Basic: 9 columns x 9 rows Character: 9 columns x 7 rows	Standard 80 characters	10 inches/ • Friction feed • Tractor feed (optional)	3 copies, conditional

Color Display MZ1D18

Product outline	640 x 400 dots, 15 inch flat square, non-glare semi-black type color display for use with the MZ-5500/5600.	
Specification	Tube used	15 inch, 90° deflection flat square type (non-glare treated)
	Input signal (Horizontal synchronization signal) (Vertical synchronization signal)	R, G, B, three independent TTL polarity TTL positive polarity TTL negative polarity
	(Deflection frequency)	24.86KHz, horizontal, and 55.48 Hz, vertical
	Display time	29.80μS, horizontal and 16.09 ms, vertical
	Resolution	640 dots, horizontal, and 400 dots, vertical
	Display colors	Seven colors of red, green, blue, yellow, magenta, cyan, white, and black
	Display capacity	4000 characters, maximum. 2000 characters with the MZ-5500/5600.
	Dot pitch	0.39 mm
	Power supply	Rated voltage
	Physical dimensions	404(W) x 409(D) x 331(H) mm
	Weight	15.0 Kg
	Power consumption	75 (W)
	Input connector	Rectangular 8-pin connector 1. Open 2. Video input (red) 3. Video input (green) 4. Video input (blue) 5. Ground 6. Ground 7. Horizontal synchronizing signal 8. Vertical synchronizing signal
	Adjust knob	Front: POWER switch Side: Vertical synchronization, vertical amplitude horizontal synchronization, horizontal phase, brightness
	System configuration	(Personal computer) MZ-5600 series ↓ (Color display) MZ-1D18 (Cable attached to the unit) ↓ (Tilt stand)
	Appearance color	Office gray
Accessories	Interfacing cable, instruction manual	

*MZ-1F05 standard floppy disk drive

Product outline	The 8" floppy disk drive for use with the MZ-3500 series, MZ-5500 series, and MZ-5600 series. It has to be interfaced via the exclusively designed MZ-1E11 interface board for the MZ-5500 and MZ-5600. Interfacing cable comes with the MZ-1E11.	
Specification (per drive	Memory capacity	1.2MB, formatted
	Tracks	77 tracks x 2
	Sectors	8 sectors/track
	Media	8" floppy disk
	Supply voltage	100V (50/60Hz)
	Power consumption	100W
	Physical dimensions	19.5cm wide, 37.5cm deep 22.0cm high
	Weight	15.2Kg
	Color	Office gray

*MZ-1F10 hard disk drive

Product outline	5.25", 10.7MB external hard disk drive for use with the MZ-5500 series, MZ-5631 and 5641. Includes the interface and interfacing cable.	
Specification	Recording capacity	10.7MB, formatted
	Track capacity	8.704KB, formatted
	Sectors capacity	512B, formatted
	Sectors per track	17
	Disk used	2 disks
	Heads	4
	Cylinders	317
	Revolutions	3600RPM
	Data transfer speed	500KB/s, max., between CPU and controller
	Recording density	9260BPI
	Recording method	MFM
	Supply voltage	100V, 50/60Hz
	Power consumption	65W
	Physical dimensions	11.8cm wide, 33.1cm deep 18.9cm high
	Color	Office gray

1-6 Optional devices specifications (for MZ-5500)

• Arithmetic and logical processor MZ-1M03

Description	Designed to increase arithmetic and logical operation speeds.

• Additional mini-floppy disk drive (MFD) MZ-1F02

Description	Additional mini-floppy disk drive unit for the MZ-3500 Series and MZ-5500 Series. May be used as the 3rd and 4th drives, and has a total storage capacity of 640KB. Join to the MFD I/F connector on the rear of the System Unit using the dedicated cable MZ-1C33.		
Specifications	Drive	Thin-profile, double-sided, double-density drive (FD55B) x 2.	
	PWB	I/F PWB: 45 x 129mm (double-sided paper epoxy board)	
		LED PWB: 23 x 8.5mm (single-sided paper epoxy board)	
	Power supply	Switching regulator	+5V (1.3A) and +12V (1.3A) Contained in a metallic housing measuring 98(W) x 16.5(H) x 87(D)mm
	Cabinet	Top and bottom cabinets: Press-molded metal Front panel: Molded resin Color: Office gray Dimensions: 117.7(W) x 177.7(H) x 331.3(D)mm Weight: 6kg	

*MZ-1F09 internal expansion MFD drive

Product outline	Flat type, two-sided, double-density, mini-floppy disk drive (with cable) option. One unit of this drive can be expanded internally in the MZ-5511.
Specification	Identical to the internal mini-floppy disk drive unit of the MZ-5500.

1-7 Optional devices specifications (for MZ-5600)

• Arithmetic and logical processor MZ-1M09

Table 8

Description	Designed to increase arithmetic and logical operation speeds. (8087-2)

• Additional mini-floppy disk drive (MFD) MZ-1F16

Table 9

Description	Additional mini-floppy disk drive unit for the MZ-5600 Series. May be used as the 3rd and 4th drives, and has a total storage capacity of 1280 KB. Join to the MFD I/F connector on the rear of the System Unit using the dedicated cable MZ-1C43.		
Specifications	Drive	Thin-profile, double-sided, double-density drive (FD55F) x 2.	
	PWB	I/F PWB: 45 x 129mm (double-sided paper epoxy board)	
		LED PWB: 23 x 8.5mm (single-sided paper epoxy board)	
	Power supply	Switching regulator	+5V (1.3A) and +12V (1.3A) Contained in a metallic housing measuring 98(W) x 16.5(H) x 87(D)mm
	Cabinet	Top and bottom cabinets: Press-molded metal Front panel: Molded resin Color: Office gray Dimensions: 117.7(W) x 177.7(H) x 331.3(D)mm Weight: 6kg	

*MZ-1F15 internal expansion MFD drive

Product outline	Flat type, two-sided, double-density, double-track, mini-floppy disk drive (with cable) option which can be expanded internally in the MZ-5631.
Specification	Identical to the internal mini-floppy disk drive unit of the MZ-5600.

°MZ-1F18 expansion hard disk unit

Product outline	Expansion hard disk unit option for use with the MZ-5645. Must be directly connected to the hard disk interface provided in the MZ-5645 slot.	
Specification	Recording capacity	10.7MB, formatted
	Track capacity	8.704KB, formatted
	Sectors capacity	512B, formatted
	Sectors per track	17
	Disk used	2 disks
	Heads	4
	Cylinders	317
	Revolutions	3600RPM
	Data transfer speed	500KB/s, max., between CPU and controller
	Recording density	9260BPI
	Recording method	MFM
	Supply voltage	200V, 60Hz
	Power consumption	65W
	Physical dimensions	11.8cm wide, 33.1cm deep 18.9cm high
	Color	Office gray

°MZ-1F14 internal expansion hard disk

Product outline	Hard disk unit (with interface unit and interfacing cable) for internal expansion in the MZ-5631.
Specification	Identical to the MZ-1F18.

SECTION TWO
Hardware Specifications

1. CPU peripheral

For the CPU of the MZ-5500 is used the 16-bit CPU (8086) which has bec me the main trend and is driven by 5MHz clock. On the other hand, the 8086-II is adopted for the MZ-5600 which permits 8MHz/5MHz selection for driving clock. In the 5MHz mode, compatibility is obtained for the real time processing for applications developed on the MZ-5500.

The 8086/8086-II has features shown in Table 1-1, and has two modes of minimum and maximum allowing choice of pin configuration according to the size of the system used. It consists of the execution unit (EU) and the bus interface unit (BIU); the BIU manages 6-byte command queue and performs address generation, and the EU interprets command function. Each unit operates in the async mode and enhances high throughput by the use of the pipe line processing.

It is possible to directly access the memory up to 1MB. Using A0 and BHE lines of the 8086, data may be used as either 8-bit or 16-bit data.

Since the 8086/8086-II is operated under the maximum mode for the MZ-5500/5600, it requires the 8284 Clock Generator and the 8288 Bus Controller in order to operate the 8086 as the CPU. Not only the 8284 supplies the clock (4.9152MHz) to the 8086, but, it has the function to synchronize the READY signal generated in the ready control circuit with the clock to send it to the CPU. The 8288 is the bus controller/driver when the 8086 is operated in the maximum mode. Command and control signals are decoded from the status output, S0 - S2, from the CPU to issue control signal to the I/O device and the memory.

As a coprocessor for a high speed numerical operation of the 8086, it permits direct connection of the 8087 (MZ-5500), 8087-II (MZ5600), and NDP (option). In terms of software, it can be assumed as an expansion of the 8086/8086-II command system. As Table 1-2 shows its execution speed, it becomes 100 times faster than operated with only the 8086/8086-II.

For key entry of the MZ-5500/5600, the exclusive 80C49 subprocessor is used. A key entry is transferred by means of interrupt only when there was a key entry so that it decreases the burden to the 8086 and allows faster system operation. The 80C49 is also used for handling of the mouse data.

Table 1-1 Features of 8086, 8086-II

(1) 16-bit microprocessor
(2) Basic commands: 90
(3) Direct accessing enabled 1MB memory space
(4) 14 x 16 bits register
(5) Arithmetical operation of signed or unsigned 8 or 16 bits data including multiplication and division
(6) 5MHz, single clock (8086)/8MHz (8086-II)
(7) Maskable (INTR) and non-maskable (NMI) external interrupt input
(8) Dual mode operation (minimum/maximum)
(9) N-channel MOS
(10) Single +5V supply
(11) 40-pin DIP

Table 1-2 8087 and emulator execution speed comparison

Item	Basic frequency 5MHz[us]	
	8087	8086 emulation
Multiply (single precision)	19	1600
Multiply (double precision)	27	2100
Add	17	1600
Divide (single precision)	39	3200
Compare	9	1300
Square root	36	19600
tan	90	13000
e^x	100	17100

MZ5500 SYSTEM BLOCK DIAGRAM

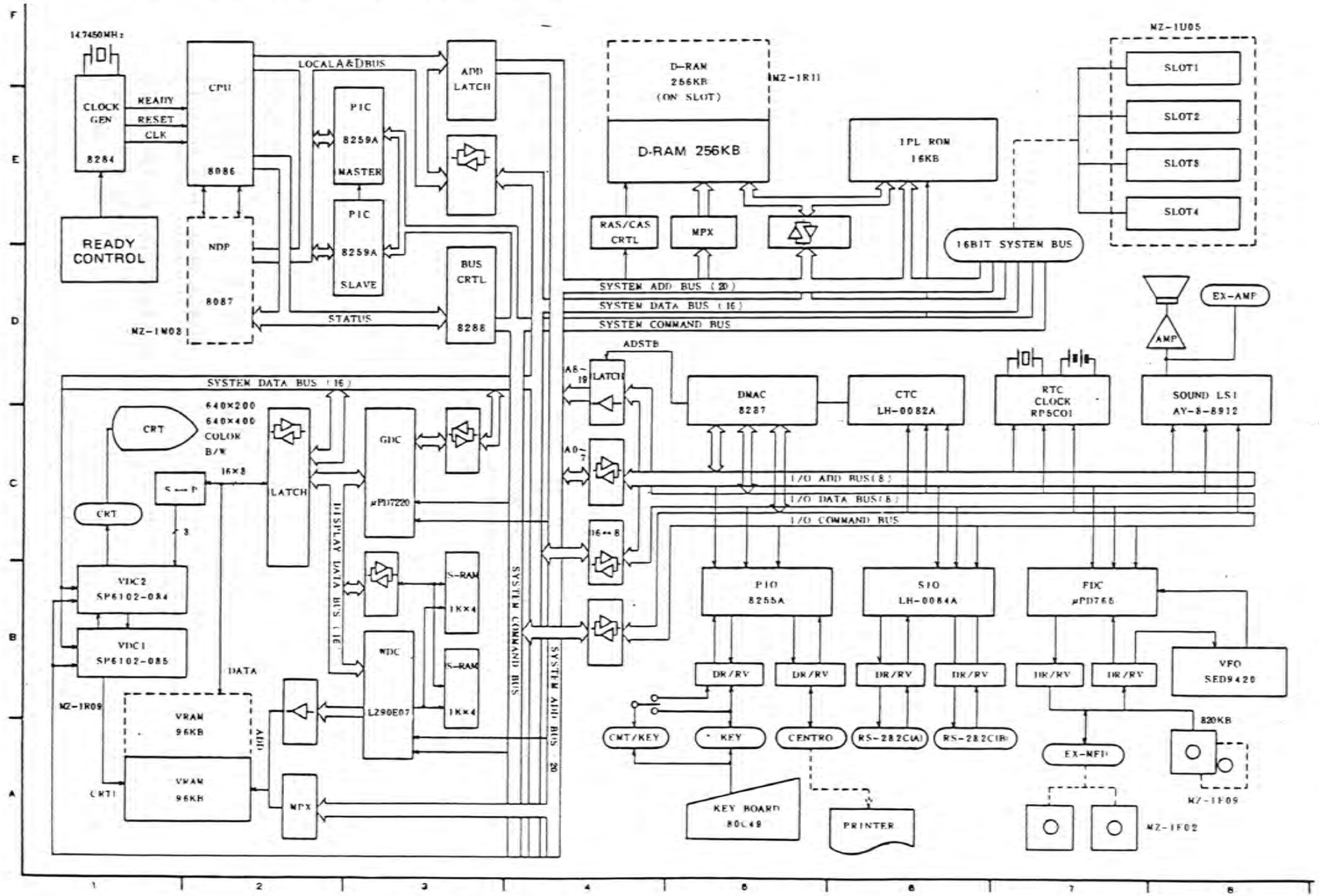
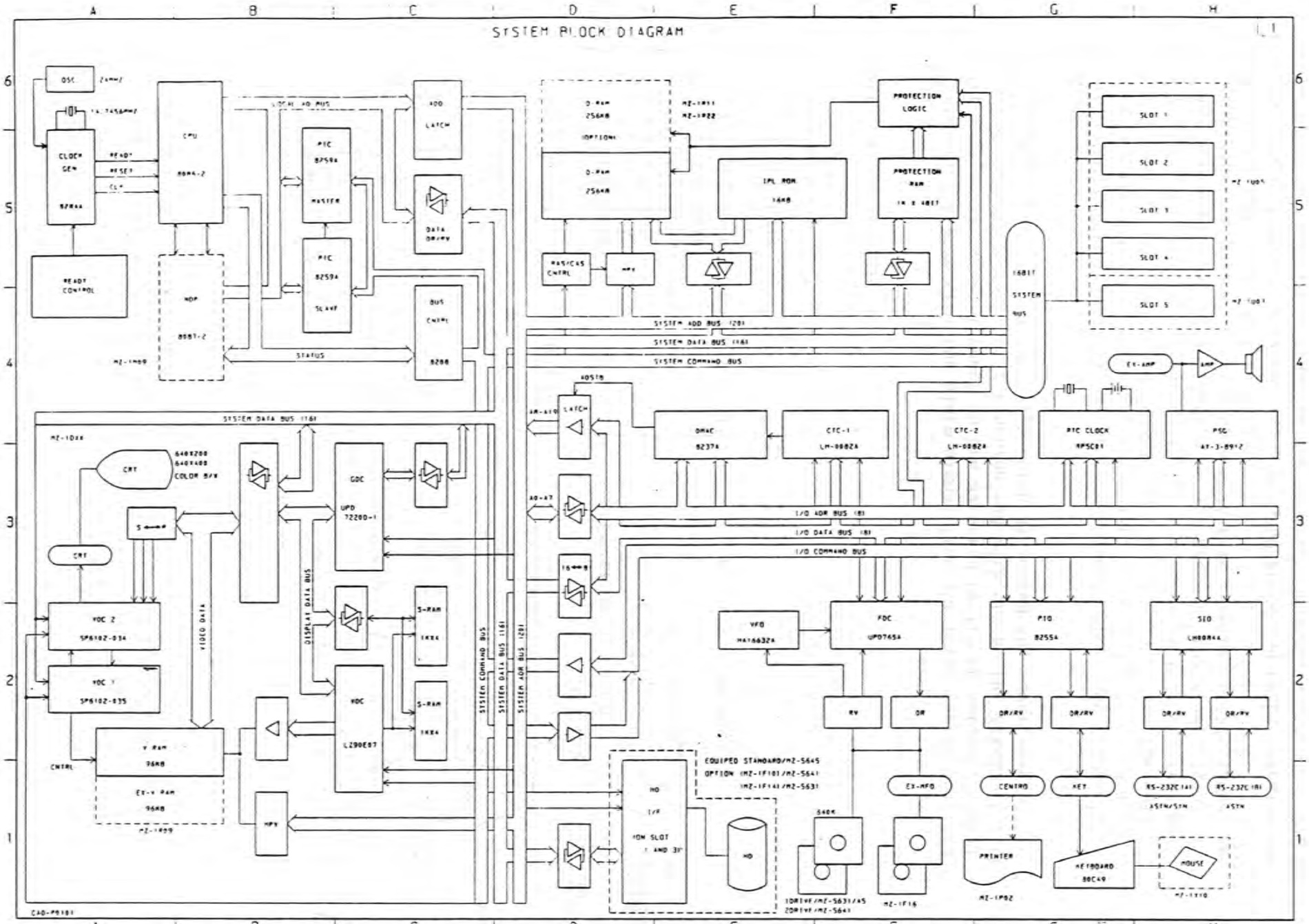


Fig. 1-1

MZ-5600 SYSTEM BLOCK DIAGRAM



o Bus control circuit

Fig.1-3 shows the block diagram of the MZ-5500/5600 bus control circuit. When the 8086 is operated under the maximum mode, command (RD, WR, INTA) is issued in a form of a status (S0-S2) which is decoded by the 8288 to send the control signal to the memory and the I/O device.

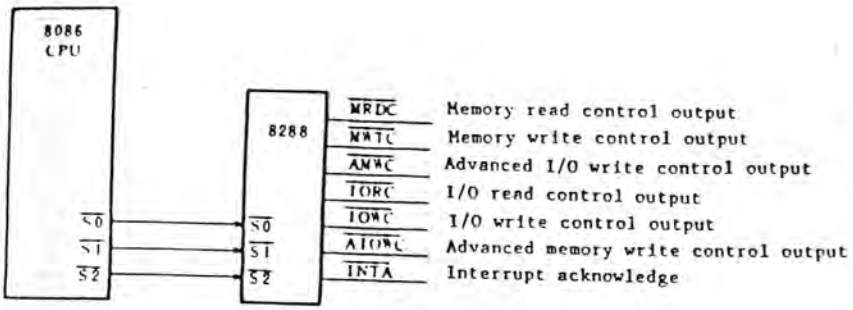


Fig.1-3 Bus control circuit block diagram

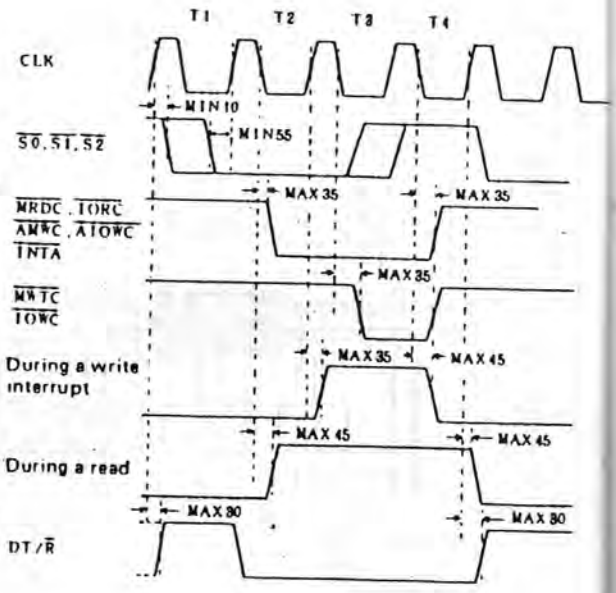


Fig.1-4 Timings

Table 1-3 8288 input vs output

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	Output
0	0	0	INTA
0	0	1	IORC
0	1	0	IOWC, AIOWC
0	1	1	Hold
1	0	0	MRDC (command fetch)
1	0	1	MRDC
1	1	0	MWTC, AMWC
1	1	1	Passive

o RESET, READY circuit

RESET

For reset of the 8086 CPU, the alarm signal from the power supply unit and a rising edge at the time of power on are detected by the CR network. RESET signal to the CPU is internally synchronized with CLK by the 8284A. For the alarm timing, refer to the paragraph which discussed the power supply.

READY

For the MZ-5500/5600 is normally a non-ready system, the ready signal is returned to the CPU against a valid accessing. Actually, memory and I/O decode signal is inputted to the 8284A, but, RDY is delayed in the wait timing circuit in synchronization with CLK for a device that requires wait. When the I/O and memory of the $\overline{XACK}$ area is accessed, the ready signal of timeout is automatically returned unless $\overline{XACK}$ is returned within 130μs, and NMI is issued to the CPU at the same time.

Fig.1-5 shows the block diagram of the MZ-5600 RESET and READY circuits and Table 1-4 shows wait count required for device. However, on the MZ-5500, the $\overline{LSPD}$ signal (for wait count adjustment according to the choice of 5MHz/8MHz clock) shown in the block diagram is not applicable, and signal name TG555 is changed to AN555. Wait counts are for the 5MHz mode in Table 1-4.

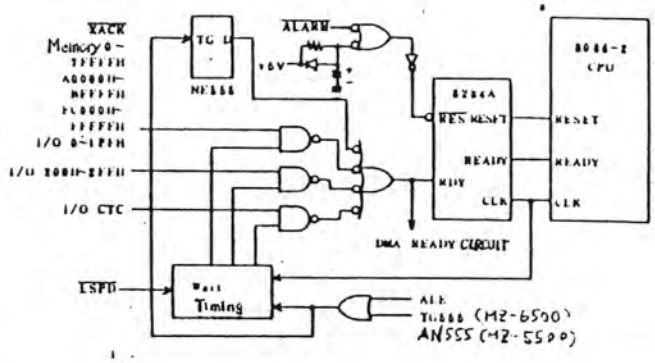


Fig.5 RESET and READY circuit block diagram

Table 1-4 Wait count of device

	8MHz mode	5MHz mode
°System RAM °IPL ROM °I/O other than below	1	0
°SIO °RTC °PSG °PB	3	3
°CTC °INTACK °INT RET	15	15
°VRAM °I/O(380H-3FFH) °Memory other than above	XACK or 1	XACK

READY signal timings

Figures next show READY signal timings for the MZ-5500 (5MHz) and MZ-5600 (8MHz/5MHz).

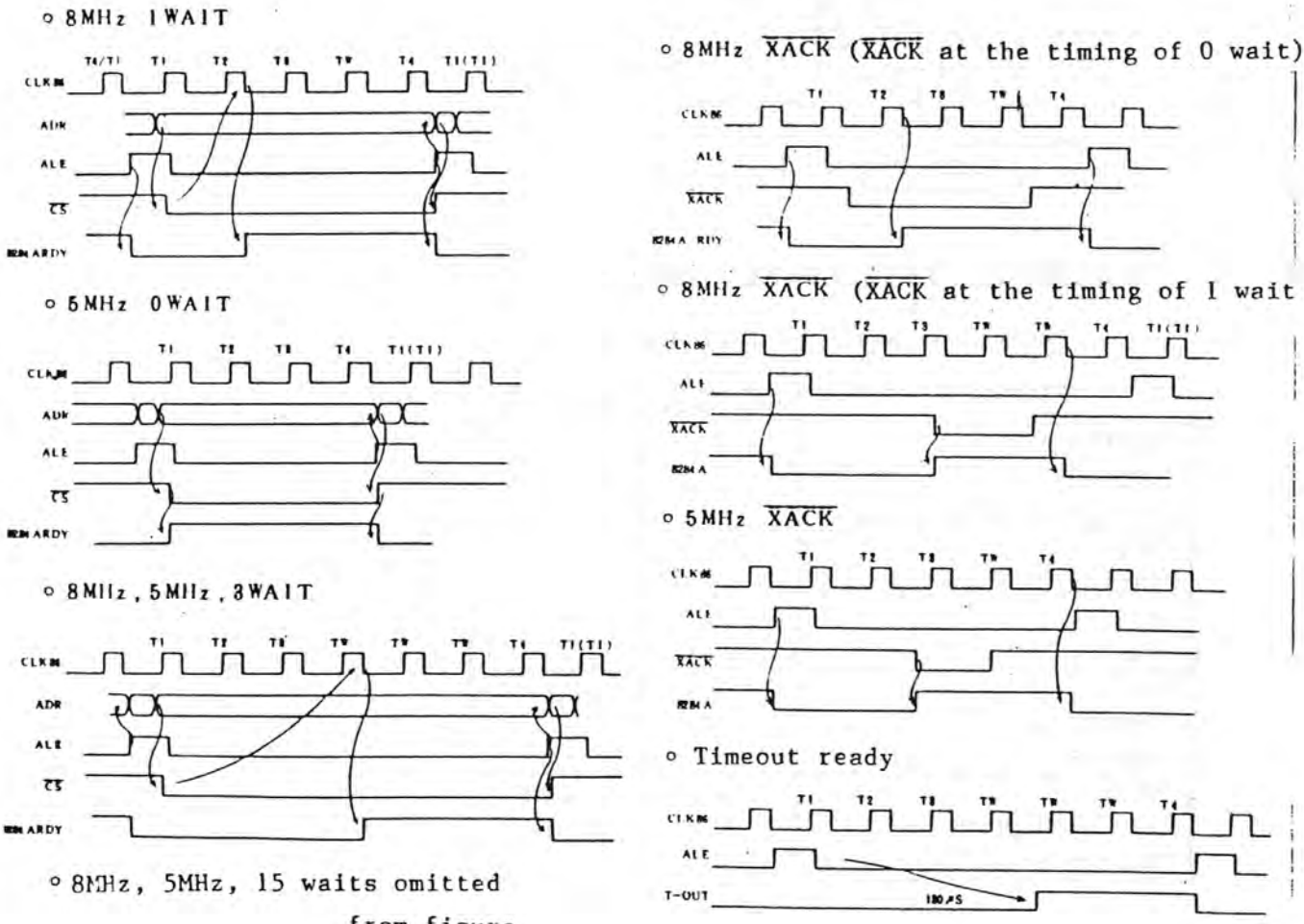


Fig.1-6 READY signal timings

2. Memory

2-1. MZ-5500/5600 memory and memory map

Fig.2-1 shows the memory map of the MZ-5500/5600.
For the memory, it is possible to expand the system RAM up to 512KB. 128KB is equipped standard for the MZ-5511 and 256KB for the MZ-5521 and MZ-5600 series.
For memory expansion, such as MZ-1R16 Expansion DRAM and the MZ-1R11 Expansion RAM Board are available.
In regard to the VRAM, 96KB is standard for the MZ-5500/5600 series, which can be expanded 96KB more by the use of the MZ-1R09 option.
16KB of the ROM is used for IPL (Initial Program Loader) which is used to initialize the system and load CP/M loader.
Since the CRT display is performed by the bit map method with the MZ-5500/5600, it does not use the CG ROM, but character patterns are contained in the IPL ROM.

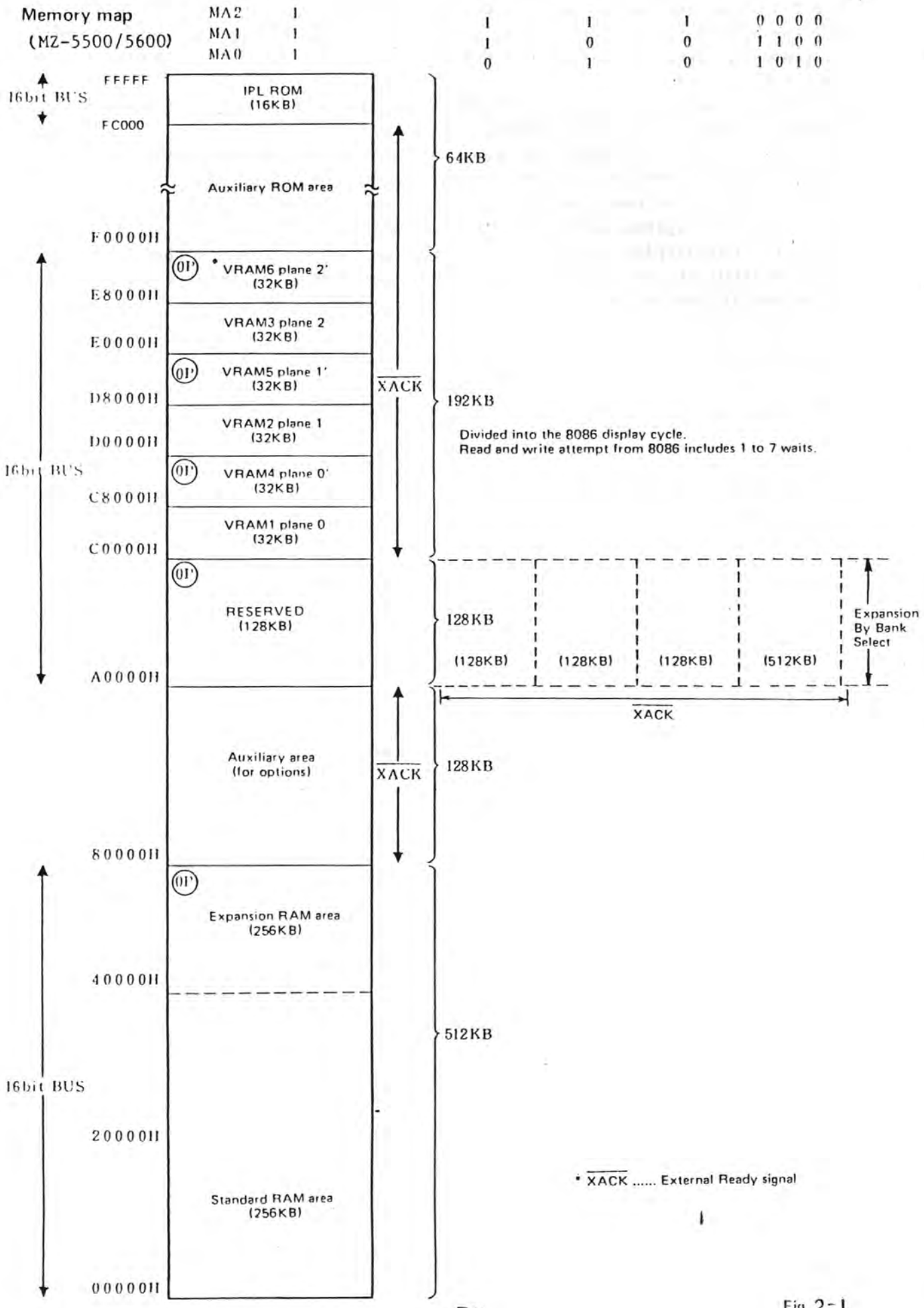

Memory map
(MZ-5500/5600)
MA2 1 1 1 0 0 0 0
MA1 1 1 0 1 1 0 0
MA0 1 0 0 1 0 1 0
16bit BUS
FFFFF
FC000
IPL ROM
(16KB)
Auxiliary ROM area
64KB
F00000H
E80000H
E00000H
D80000H
D00000H
C80000H
C00000H
A00000H
800000H
400000H
200000H
000000H
VRAM6 plane 2'
(32KB)
VRAM3 plane 2
(32KB)
VRAM5 plane 1'
(32KB)
VRAM2 plane 1
(32KB)
VRAM4 plane 0'
(32KB)
VRAM1 plane 0
(32KB)
RESERVED
(128KB)
XACK
192KB
Divided into the 8086 display cycle.
Read and write attempt from 8086 includes 1 to 7 waits.
128KB
(128KB)
(128KB)
(128KB)
(512KB)
Expansion
By Bank
Select
XACK
Auxiliary area
(for options)
XACK
128KB
Expansion RAM area
(256KB)
512KB
Standard RAM area
(256KB)
* XACK ..... External Ready signal

Fig. 2-1

2-2. I/O map

1) MZ-5500/5600 I/O map

For I/O of the MZ-5500, it needs 0 wait for accessing of 0 to 1FFH, 3 waits for 200 - 37FH, for which the ready signal is automatically created in the MZ-5500. Where noted "byte access" in the I/O indicates connection to the 8-bit bus. Where noted "reserved" is the area reserved by the system.
For the MZ-5600, the I/O map is basically the same as the MZ-5500, but, 1 wait is inserted for the area 0 - 1FFH only in the 8MHz mode. See Table 2-2 for the I/O bit map.

ii) I/O user area

For both the MZ-5500 and MZ-5600, three areas of 180 - 1AFH [0 wait (5MHz)/1 wait (8MHz)], 300 - 33FH (3 waits), and 3C0 - 3FFH ($\overline{XACK}$) are open for user's use.
In the 8MHz mode of the MZ-5600, 1 wait is automatically inserted when $\overline{XACK}$ is returned in the 0 wait timing.
If $\overline{XACK}$ is not returned within 130μs, CP/M initiates bootstrapping.
For practical examples of the I/O user area usage, refer to the paragraph discussing the expansion slot.

I/O address map (MZ-5500/5600)

Table 2-1

	HEX	15 – 12	11	10	9	8	7	6	5	4	3	2	1	0	DEVICE		WAIT
		ADDRESS															
System PWB	00– 0F	X – X	X	X	0	0	0	0	0	0	A3	A2	A1	A0	DMAC (8237)	ID0-7	Byte Access
	10– 1F				0	0	0	0	0	1	X	X	A1	A0	PIO (8255A)	ID0-7	
	20– 2F				0	0	0	0	1	0	X	X	X	A0	FDC (μPD765)	1D0-7	
	30– 3F				0	0	0	0	1	1	X	X	A1	0	PIC1 (8259A) MASTER	AD0-7	
	40– 4F				0	0	0	1	0	0	X	X	A1	0	PIC2 (8259A) SLAVE	AD0-7	
	50– 5F				0	0	0	1	0	1	X	X	X	X	DMAC high-order address latch	ID4-7	
	60– 6F				0	0	0	1	1	0	X	X	X	X	PORT-A	ID0-7	
	70– 7F	X – X	X	X	0	0	0	1	1	1	X	X	X	X	PORT-C	ID0-3	
I/O slot	80– 8F	X – X	X	X	0	0	1	0	0	0	X	X	A1	A0	Reserved	ID0-3	
	F8– FF	X – X	X	X	0	0	1	1	1	1	1	A2	A1	A0	Reserved		
CRT PWB	100–10F	X – X	X	X	0	1	0	0	0	0	X	X	A1	0	GDC (μPD7220)	D0-7	0 Wait/ 5MHz 1 Wait/ 8MHz
	110–11F				0	1	0	0	0	1	X	X	A1	0	WDC (T)	D0-7	
	120–12F				0	1	0	0	1	0	A3	A2	A1	0	VDC2 (H2)	D0-2	
	130–13F				0	1	0	0	1	1	X	X	X	0	VDC1 (H1)	D0-2	
	140–14F				0	1	0	1	0	0	X	A2	A1	1	RFL I	D8-10	
	150–15F				0	1	0	1	0	1	X	A2	A1	1	RFL II	D8-10	
	160–16F				0	1	0	1	1	0	X	X	X	1			
	170–17F	X – X	X	X	0	1	0	1	1	1							
I/O slot	180–18F	X – X	O	O	0	1	1	0	0	0	X	A2	A1	0	Note		
	190–19F				0	1	1	0	0	1	X	A2	A1	0	Note	User area	
	1A0–1AF				0	1	1	0	1	0	X	X	X	X	Note		
	1B0–1BF				0	1	1	0	1	1					Note		
	1C0 –1FF	X – X	O	O	0	1	1	1	1	1	X	X	X	X	Reserved		
CPU PWB	200–20F	X – X	X	X	1	0	0	0	0	0	X	X	A1	A0	SIO (LH0084A)	1D0-7	Byte Access
	210–21F				1	0	0	0	0	1	X	X	A1	A0	CTC (Z-80CTC)	1D0-7	
	220–22F				1	0	0	0	1	0	A3	A2	A1	A0	RTC (PR5C01)	1D0-7	
	230–23F				1	0	0	0	1	1	X	X	X	X	PSG (AY-3-8198)	1D0-3	
	240–24F				1	0	0	1	0	0	X	X	X	X	CTC INT Reset	X	
	250–25F				1	0	0	1	0	1	X	X	X	X	SIO INT Reset	X	
	260–26F				1	0	0	1	1	0	X	X	X	X	CTC Return INT	1D0-7	
	270–27F	X – X	X	X	1	0	0	1	1	1	X	X	X	X	PORT-B	1D0-3	
I/O slot	280– 2FF	X – X	O	O	1	0	1	0	0	0					Reserved		
		X – X	X	X	1	0	1	1	1	1							
	300– 37F	X – X	X	X	1	1	0	0	0	0					User area		3 Wait
	340–						0	1	0	0							
		X – X	X	X	1	1	0	1	1	1					Reserved		
	380 –3FF	X – X	X	X	1	1	1	0	0	0					Reserved For I/O slot		XACK
							1	1	1	1					Not Ready generates within the System Unit. User area		

Note: 180H to 1BFH: PWB checker

X: Not in Decode

D0-15 – 16 Bit system BUS
ID0-8 – 8 Bit I/O BUS

$\overline{XACK}$:
In the 8MHz mode of the MZ-5600, 1 wait is automatically inserted when $\overline{XACK}$ is returned in the 0 wait timing. If $\overline{XACK}$ was not returned within 130μs, CP/M initiates bootstrapping.

(1) System board

Table 2-2a

DEVICE	ADD	BIT	SIGNAL NAME	I/O		AFTER P/O	INITIAL DEFAULT
8255 [Group A, Mode 1 / Group B Mode 0]	010H	PA0	$\overline{\text{DATA1}}$	OUT	Data output to Centronics I/F (negative polarity). Null codes are hex FF.	Input mode (FFH)	Output mode (FFH)
		PA1	$\overline{\text{DATA2}}$				
		PA2	$\overline{\text{DATA3}}$				
		PA3	$\overline{\text{DATA4}}$				
		PA4	$\overline{\text{DATA5}}$				
		PA5	$\overline{\text{DATA6}}$				
		PA6	$\overline{\text{DATA7}}$				
		PA7	$\overline{\text{DATA8}}$				
	011H	PB0	$\overline{\text{BUSY}}$	IN	Centronics I/F busy (busy if zero.)	Mode input	Mode input
		PB1	$\overline{\text{PE}}$		Centronics I/F.		
		PB2	PDTR		Centronics I/F select signal (selects if one.)		
		PB3	DK		Data bit from keyboard } Key		
		PB4	SRK		Output requested from keyboard } Key		
		PB5	$\overline{\text{CD}}$		Carrier sense } for synchronous mode		
		PB6	$\overline{\text{CI}}$		Called signal } for synchronous mode		
		PB7	MOTOR ON		MFD motor on status input		
	012H (013H)	PC0	DC	OUT	Data bit to keyboard }	Input mode (FFH)	1
		PC1	STC	OUT	Strobe to keyboard }		0
		PC2	$\overline{\text{EXCLK EN}}$	OUT	BSC external clock (BSC if High)		0
		PC3	IR-PRT	OUT	Interrupt by ACK input to Centronics I/F.		0
		PC4					0
		PC5	$\overline{\text{STROBE}}$	OUT	Centronics I/F $\overline{\text{STROBE}}$ output (⊓⊔)		1
		PC6	$\overline{\text{ACK}}$	IN	Centronics I/F $\overline{\text{ACK}}$ input		X
		PC7		OUT	Not used.		X

NOTES:
1) Group A is used in Mode 1.
2) Group B is used in Mode 0.
3) The desired bit of the output to Group C may be set or reset using the control register (013H).
4) The bit PC6 is an interrupt enable flag (INTE), and is set or reset by the CPU.
5) While the $\overline{\text{ACK}}$ may be read by PC3, is needs not be read as its status is known to the CPU via the PIC.

Table 2-2b

DEVICE	ADD	BIT	SIGNAL NAME	I/O		AFTER P/O	INITIAL DEFAULT
AY-3-8912 (Sound IC)	230H			OUT		Input mode (FFH)	0
							0
							0
							0
		IOA4	$\overline{\text{MOTOR ON}}$		Drive motor on signal (on if Low.)		1
		IOA5	MA0		Area (A0000H~BFFFFH) bank select signal		0
		IOA6	MA1				0
		IOA7	MA2				
PORT-A (LS541)	060H	ID0	$\overline{\text{High Den}}$	IN	RESET switch input (on if zero) ← MFD selection	Input mode	Input mode
		ID1	$\overline{\text{RSTSW}}$				
		ID2	DIP SW1		SW1 } System DIP switches (see next page)		
		ID3	DIP SW2		SW2		
		ID4	DIP SW3		SW3		
		ID5	DIP SW4		SW4		
		ID6	DIP SW5		SW5		
		ID7	DIP SW6		SW6 }		

(1) When accessing the I/O port of the AY-3-8912 sound IC), load I/O register address into 231H, then write the I/O data to 230H.

(2) When initializing the IOA port, write the data to be output (described above), then place the port in the output mode. This is needed to maintain the SEL and MOTOR ON signals inactive during initialization.

*I/O address area shown in the table below may differ between the MZ-5500 and the MZ-5600.

Table 2-3a MZ-5500.

DEVICE	ADD	BIT	SIGNAL NAME	I/O		AFTER P/O	INITIAL DEFAULT
PORT-C (LS175)	070H	ID0	$\overline{WRCT}$	OUT	Dedicated cassette Write signal (No use)	Indefinite	
		ID1	MOTOR		Dedicated cassette Motor signal (No use)		
		ID2					
		ID3	FDCRST		FDC Reset signal (reset when one.)		
PORT-B (LS125)	270H	ID0	$\overline{RDCT}$	IN	Dedicated cassette Read signal (No use)	Input mode	
		ID1	SENSE		Dedicated cassette Sense signal (No use) (0: SW OFF, 1: SW ON and CPU)		
		ID2	DIP SW7		SW7 } System DIP Switches (See page.)		
		ID3	DIP SW8		SW8 }		

Table 2-3b MZ-5600

DEVICE	ADD	BIT	Signal name	I/O		After power on	Initialize
PORT-C (LS74)	070H	ID0		OUT		Don't care	
		ID1					
		ID2	High Den		MFD *1M/640K alternate signal		
		ID3	FDCRST		FDC reset signal (reset with "1")		
PORT-B (LS367)	270H	ID0		IN		Input mode	
		ID1					
		ID2	DIP SW7		("0" – SW OFF "1" – SW ON & CPU) SW7 } System DIP SW (See separate page)		
		ID3	DIP SW8		SW8 }		

v) System switch

Table 2-4-a System dip switch definition (MZ-5500)

Switch No.	OFF			ON
SW1	400 raster (1 D 10,11) CRT			200-raster CRT
SW2	Normal mode			Selfcheck mode
SW3	SW3	SW4	SW5	
⎫	0	0	0	Standard MFD drive (54B) DT/DD, 1F02,07,09
SW5	1	0	0	MZ-80BF
				Reserved
	SW6	8086 operated		8087 operated
	SW7	Open to user		
	SW8			

Table 2-4-b System dip switch definition (MZ-5600)

		Description	Factory setup			Description	Factory setup
SW1	OFF	High resolution display (400 rasters) used	OFF	SW5	OFF	8MHz CPU clock	OFF
	ON	Medium resolution display (200 rasters) used			ON	5MHz CPU clock	
SW2	OFF	Normally OFF		SW6	OFF	8087 numerical processor not used	
	ON	Selfcheck mode*			ON	8087 numerical processor used	
SW3		Fixed to ON	ON	SW7			
SW4		Fixed to OFF	OFF	SW8			

System switches of the MZ-5500/5600 are assigned to functions shown in Tables 2-3-a and 2-3-b. As these switches are assigned to bit, ID2 - ID7 of the I/O address 60H for all models, they are sensed by the IPL at power on.

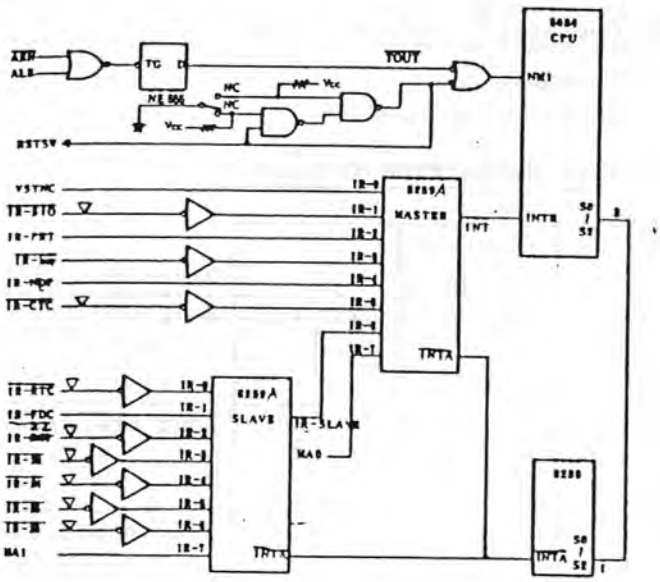
3. Interrupt circuit

3-1. Interrupt circuit

i) Circuit description

Two chips of 8259A PIC are used for the MZ-5500/5600 series, and, their circuits are shown below.

A high on the interrupt request line of the 8259A Interrupt Controller applies an interrupt to device. As the state of the mask and priority of the interrupt input is interrogated, the INT signal is issued to CPU. Because the INTR line of the CPU is asynchronous, an interrupt request can be accepted at any time unless it has been prohibited by the software. When the CPU receives the interrupt, $\overline{\text{INTA}}$ is returned via the 8288 Bus Controller. To which the 8259A forces the data bus high impedance. As the second $\overline{\text{INTA}}$ is sent from the CPU via the 8288, an 8-bit vector is sent on the data bus.



Legend: The ▽ mark represents the 6.8 kΩ pullup resistor.

Timings

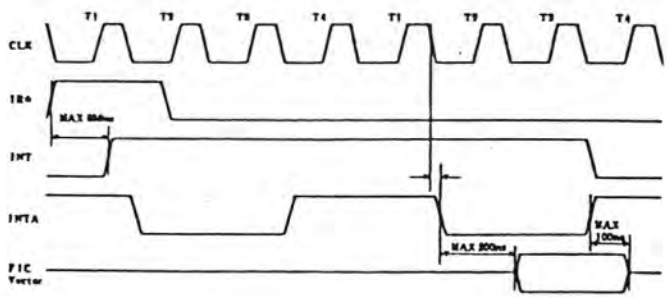


Fig.3-1 Interrupt circuit diagram and timings

ii) NMI (Non-Maskable Interrupt)

With the MZ-5500/5600 series, NMI to the 8086 CPU is used for the following two purposes:

(1) System reset

The 8086 does not have the function to send the dynamic RAM refresh signal as with the Z-80. Whereas, DREQ is issued in the prescribed period from the CTC to DMA read the dynamic RAM to refresh it. If the system is reset hardware-wise, refresh is suspended for a certain period which may possibly destruct the memory contents. Therefore, the system will be re-initialized with NMI by the software, instead of reset.

(2) Timeout monitor

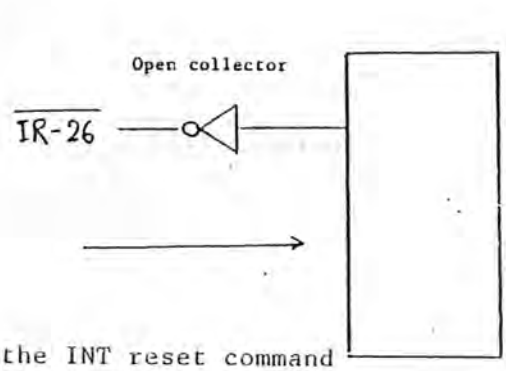
Since the MZ-5500/5600 is normally a non-ready system, accessing the memory or I/O area from which no ready signal is returned due to a software bug, it makes the CPU stopped in appearance. So, the timeout monitor circuit is provided by which the ready signal is forced to return unless the ready signal was not returned within the predetermined time and NMI is issued to the CPU at the same time to inform a timeout error.

3-2. Handling of user interrupt

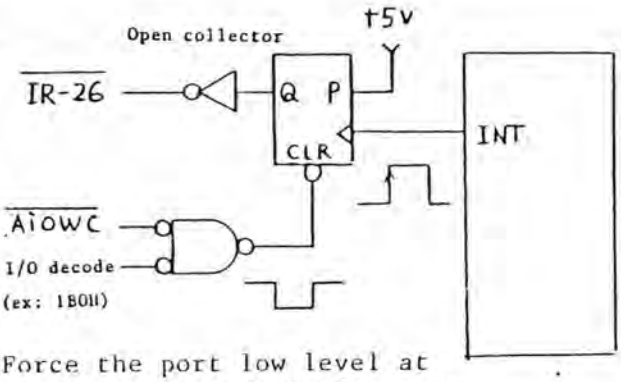
i) Hardware

As there are several interrupt signals used for the MZ-5500/5600 expansion slots, only the IR-26 is open for user's use. The user must pay attention to the following conditions when designing the interrupt circuit.

°Since the 8259A applies the interrupt to the CPU upon detection of high state of interrupt request, the interrupt request signal has to be retained until the CPU acknowledges it. Therefore, it is necessary to use the device that can clear the interrupt request by a software command or the hardware that may clear it via the I/O port.



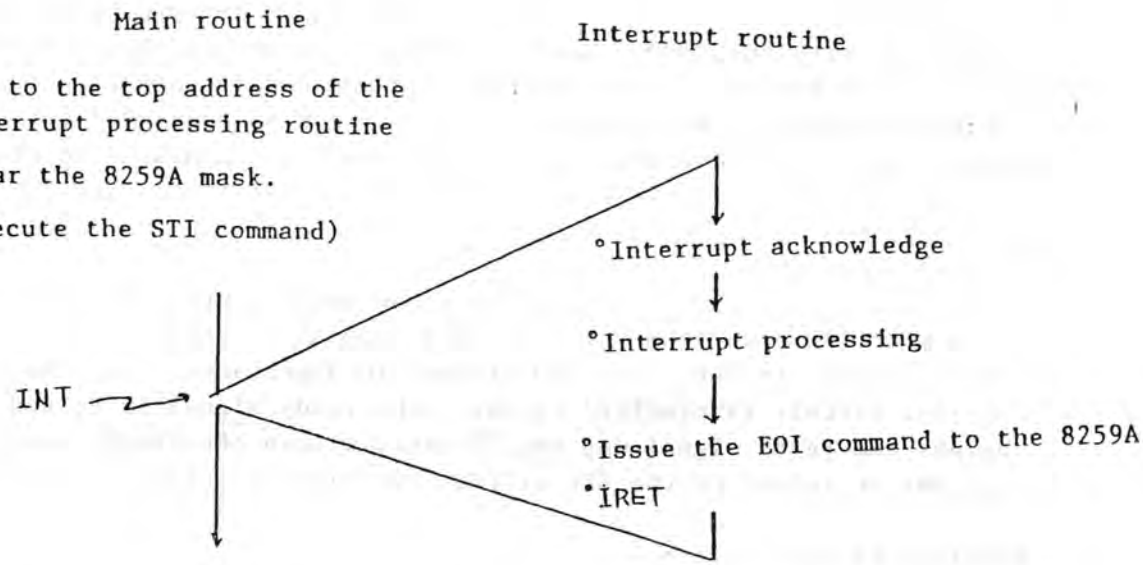
Issue the INT reset command at the beginning of the interrupt processing routine.



Force the port low level at the beginning of the interrupt processing routine.

ii) Software

The following programming is required in order to perform interrupt processing using the machine language.



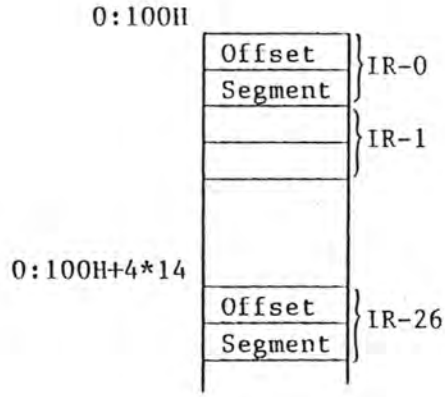
°For the MZ-5500/5600, the following modes are assigned to the 8259A PIC.

-Level trigger mode
-8086 mode
-Normal EOI mode
-Free nested mode

Interrupt routine programming mode

(1) Interrupt address designation

The top address of the interrupt processing routine must be assigned at the start of the main routine.
As shown in the figure right, the top address of each interrupt routine can be set in sequence from "segment 0: offset: 100H". The top address of the interrupt routine for the IR-26 must be written in 14th address.
Segment 0:
Offset 100H+4*14



(2) PIC mask register clear

Since the IR-26 has been masked initially, it does not permit to accept the interrupt unless the mask register is cleared.

PIC mask register I/O address: Master PIC...32H
Slave PIC....42H

The IR-26 should be programmed as follows;

```
IN  AL, 42H
AND AL, 0BFH
OUT 42H, AL
```

(3) EOI generation

At the termination of the interrupt routine, there is a need of informing the end of the interrupt processing to the PIC.

```
      :
MOV   AL, 20H
OUT   40H, AL
OUT   30H, AL
IRET
```

Example:

```
        CSEG
        ORG   100H
        ;
        XOR   BX, BX              ) Programming the
        MOV   BS, BX              ) interrupt address
        MOV   BX, 100H+4*14       )
        MOV   AX, OFFSET_INT26    )
        MOV   [BX], AX            )
        INC   BX                  )
        INC   BX                  )
        MOV   [BX], CS            )
        ;
        PUSH  CS                  ) Assign the 8080 model
        POP   DS                  )
          :
        CLI
        IN    AL, 42H             ) Clear the mask register
        AND   AL, 0BFH            )
        OUT   42H, AL             )
        STI
          :                       )
          :                       ) Interrupt enabled
          :                       )
INT26:  MOV   DX, 1B0H            ) Interrupt acknowledge
        OUT   DX, AL              )
          :
        MOVE  AL, 20H             ) EOI generated
        OUT   40H, AL             )
        OUT   30H, AL             )
        IRET
```

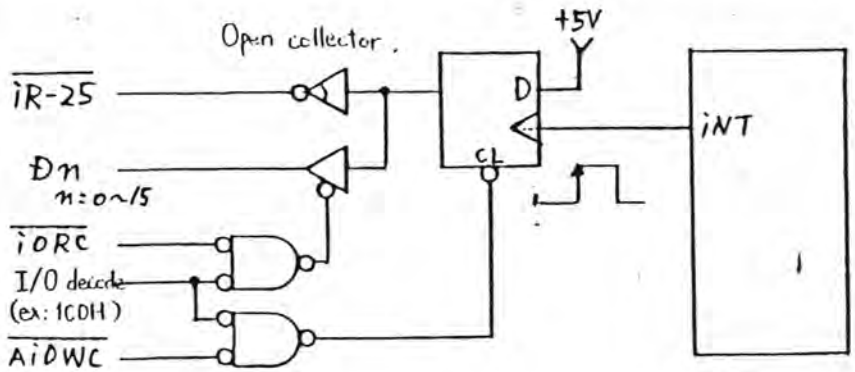
3-3. System interrupt (IR-25) specification

The MZ-5500/5600 expansion slots have several interrupt request input lines, and the IR-25 is used for system expansion. As it supports multiple interrupts of eight levels, attention must be paid to the following points when designing the interrupt circuit.

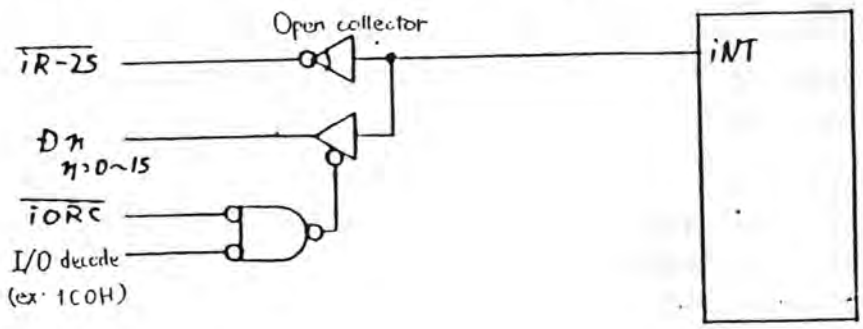
i) Hardware

Since the 8259A Interrupt Controller issues the interrupt to the CPU with a high state of an interrupt request input (low on the I/O slot), the interrupt request signal has to be retained until the CPU recognizes the interrupt. Therefore, there is a need of using the device that can clear the interrupt request by the software or the software that clears it on the I/O port. As As the IR-25 interrogates multiple interrupt by a software polling, it is so designed as to detect the device with the interrupt request on the I/O port.

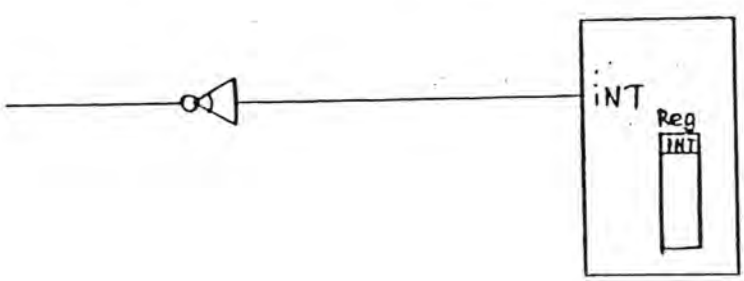
a) When the interrupt clear and port output functions are hardware comprised.



b) When using the device that has the interrupt clear function.

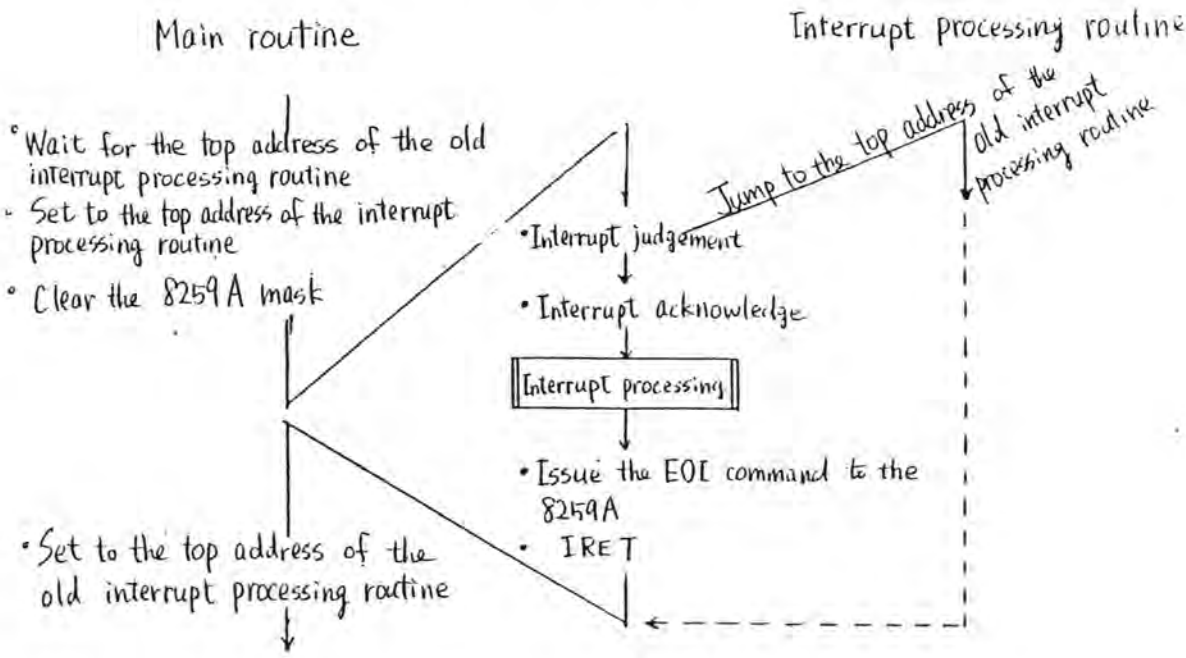


c) When using the device that has the interrupt clear function and the internal register interrupt request flag sensing function.



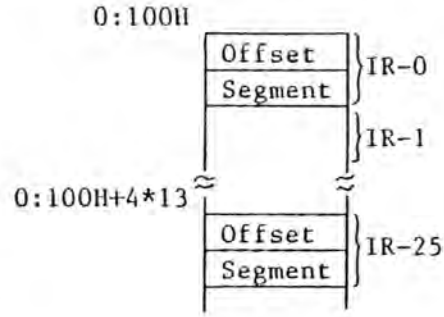
ii) Software

The following procedure is required when interrupt is processed using the machine language.



For the MZ-5500/5600, the following modes are assigned to the 8259A PIC. For more details, refer to the 8259A specification sheet.

°Level trigger mode
°8086 mode
°Normal EOI
°Free nested mode



Interrupt routine programming mode

(1) Interrupt address designation

The top address of the interrupt processing routine must be assigned at the start of the main routine. As shown in the figure right, the top address of each interrupt routine can be set in sequence from "segment 0: offset: 100H". The top address of the interrupt routine for the IR-25 must be written in 13th address.

Segment 0:
Offset 100H+4*13

Before writing the address, be sure to save the address previously written.

(2) PIC mask register clear

Since the IR-25 has been masked initially, it does not permit to accept the interrupt unless the mask register is cleared.

PIC mask register I/O address: Master PIC...32H
Slave PIC....42H

The IR-25 should be programmed as follows;

```
IN  AL, 42H
AND AL, 0DFH
OUT 42H, AL
```

(3) EOI generation

At the termination of the interrupt routine, there is a need of informing the end of the interrupt processing to the PIC.

```
MOV   AL, 20H
OUT   40H, AL
OUT   30H, AL
IRET
```

Programming example (for the circuit example-):

```
        CSEG
        ORG     100H                    ┐
        CLI                             │
        XOR     AX, AX                  │  Saving and setting
        MOV     DS, AX                  │  interrupt address
        MOV     BX, 100H+4*13           │
        MOV     AX, [BX]                │
        MOV     CS=INTADR, AX           │
        MOV     AX, OFFSET INT25        │
        MOV     [BX], AX                │
        ADD     BX, 2                   │
        MOV     AX, [BX]                │
        MOV     CS:INTADR+2, AX         │
        MOV     AX, CS                  │
        MOV     [BX], AX                ┘
        ;
        PUSH    CS                      ┐  8080 model
        POP     DS                      ┘
        ;
        IN      AL, 42H                 ┐  Clear the mask register
        AND     AL, 0DFH                │
        OUT     42H, AL                 ┘
        STI                             ┐
          :                             │
          :                             │  Interrupt enabled
INTADR  DB      0, 0, 0, 0              │
          :                             ↓
INT25:  PUSH    AX                      ┐  Interrogate interrupt
        PUSH    DX                      │
        MOV     DX, 1C0H                │
        IN      AX, DX                  │
        AND     AX, 1                   │
        JNZ     INTA                    │
        POP     DX                      │
        POP     AX                      ┘
        JMPF    CS=INTADR               ┐  To next level interrupt
                                        ┘  routine
INTA:   OUT     DX, AX                  ┐  Interrupt acknowledge
          :                             ┘
                Interrupt processing
        MOV     AL, 20H                 ┐  EOI generated and return
        OUT     40H, AL                 │
        OUT     30H, AL                 │
        POP     DX                      │
        POP     AX                      ┘
        IRET
```

4. Software timer

i) Hardware

One chip of the Z-80A CTC is used for the software timer of the MZ-5500 and it has four channels. For the MZ-5600, two chips of the Z-80A CTC which have eight channels are used.

Each channel has the specification as shown in Table 4-1. Channels, 4 to 7, however, are the specification applicable for the MZ-5600 only.

Fig.4-1 shows the block diagram of the MZ-5600 software timer. The CTC controlling channels, 4 to 7, must be omitted from the figure for the MZ-5500. A timing control circuit is added to control the Z-80A CTC I/O read, write, interrupt acknowledge, and interrupt return cycles by the 8086 CPU. Input of "0EDH" and "04DH" to the I/O port (260H) for the interrupt acknowledge cycle and the interrupt return cycle correspond to "RETI" of the Z-80 CPU.

A different CTC timing control circuit is provided for the MZ-5500 and the MZ-5600, and it has 3 waits for the I/O accessing timing of the MZ-5500 and 15 waits for the MZ-5600.

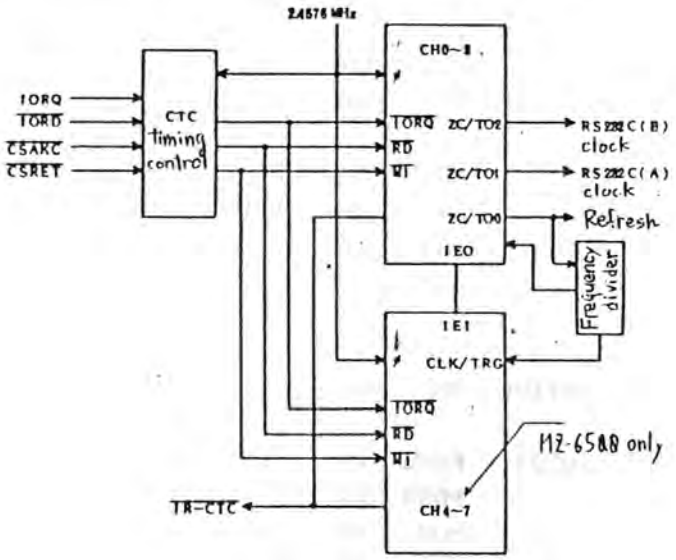


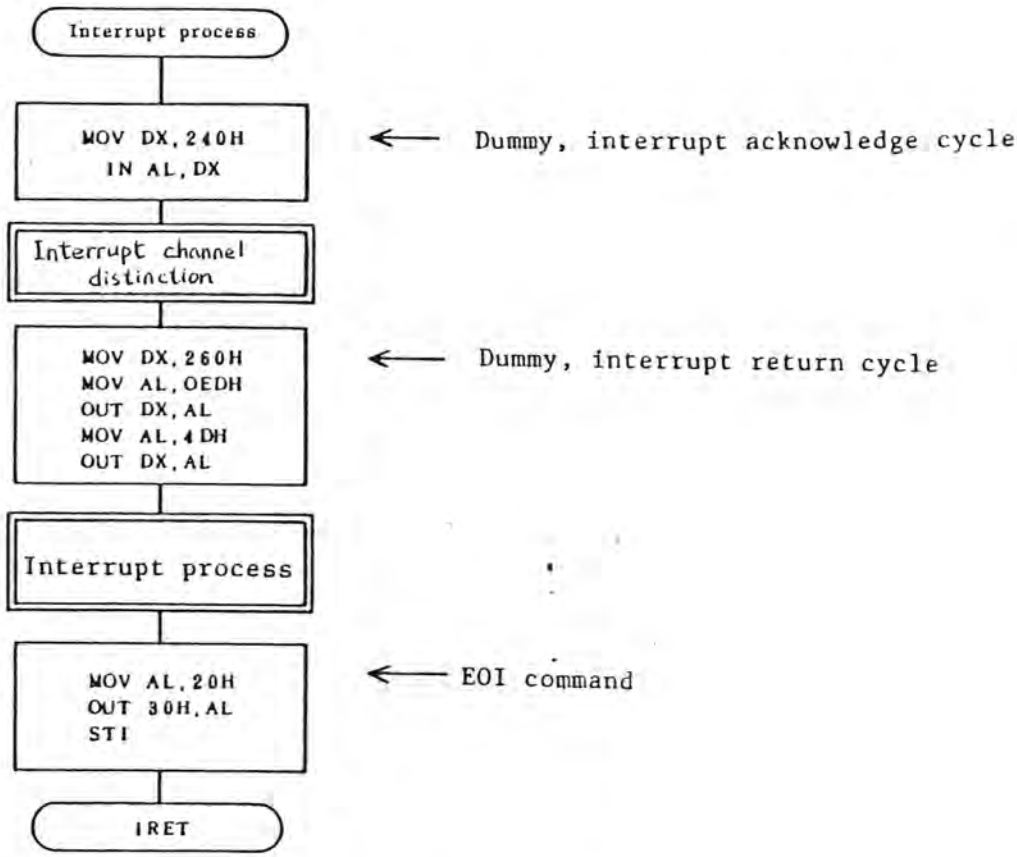
Fig.4-1 Block diagram

Table 4-1 Channel specification

Ch	I/O adr	Mode	Prescale	Int	Time constant, etc.		Model
0	210H	Timer	1/16	x	2	Refresh timer 158/2ms	5500/ 5600
1	211H	↑	↑	x	1 9600b/s 2 4800b/s 4 2400b/s 8 1200b/s	RS232C Ch A Tx, Rx	
2	212H	↑	↑	x	16 600b/s 32 300b/s 64 150b/s 87 110b/s	RS232C Ch B Tx, Rx	
3	213H	Counter		0	0.832ms-213ms	System timer	
4	214H	↑		0	0.052ms-13.313ms	Reserved	5600 only
5	215H	↑		0	0.832ms-213ms	Reserved	
6	216H	↑		0	0.832ms-213ms	Reserved	
7	217H	↑		0	3.328ms-852ms	Reserved	

ii) Interrupt processing

If the CPU is the Z-80A, the Z-80A CTC automatically executes the interrupt acknowledge cycle and the interrupt return cycle by its hardware. But, in the case of the MZ-5600, there is a need of executing the interrupt processing routine by the software. Besides, as the 8259A manages the interrupt of the MZ-5500/5600, the interrupt terminate command (EOI) must be issued to the 8259A, when it is possible to accept an interrupt of a higher priority at the end of the interrupt processing routine. The following describes the operational flow.



iii) Checking interrupt channel (MZ-5600 only)

The Z-80A CTC sends out the interrupt vector in the interrupt acknowledge cycle. Since the vector is set in the AL register when the MZ-5600 executes the dummy interrupt acknowledge cycle, the channel can be known from the state of the register. Because the vector "0H" has been set in the CTC-1, the vector "08H" must be set in the CTC-2.

Ch	Vector
3	06H
4	08H
5	0AH
6	0CH
7	0EH

iv) Interrupt cycle computing method and time factor setup

The software timer interrupt cycle must be obtained with the following formula.

t = K x T / 19200

Where, t: Interrupt cycle [s]

T: Time factor...Value set in the CTC
0 must be handled as 256.

K: Constant dependent on the channel

Ch 3: 16
Ch 4: 1
Ch 5: 16
Ch 6: 16
Ch 7: 64

Since the channel 3 is already used by the system, channels, 4 to 7, must be used.

Ex: To generate interrupt at every 10ms on the channel 6.

Time constant (T) : $10 \times 10^{-3} \times 19200 / 16 = 12$

```
MOV  DX, 216H
MOV  AL, 0C5H
OUT  DX, AL
MOV  AL, 12
OUT  DX, AL
```

To disable interrupt to the channel 6.

```
MOV  DX, 216H
MOV  AL, 41H
OUT  DX, AL
```

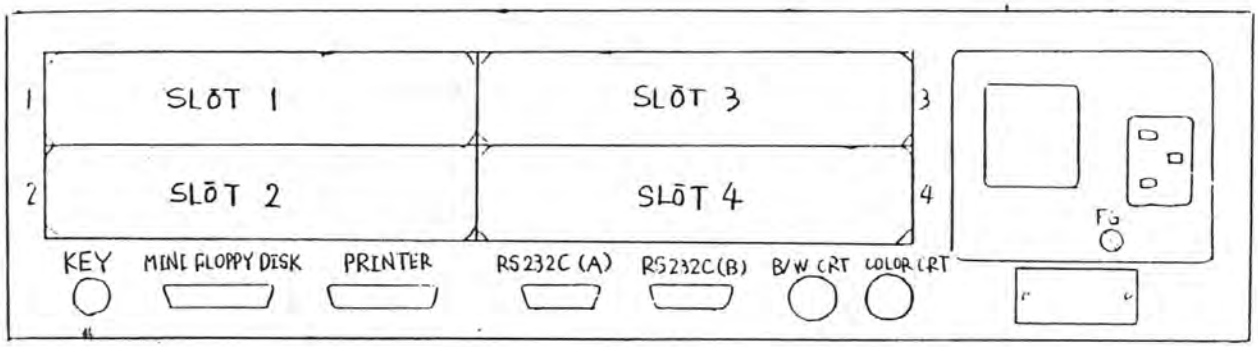
NOTE:
Range of the time factor set in the CTC is as follows:

0 to 255 ("0" signifies "256")

5. Expansion slot

5-1. MZ-5500/5600 expansion slot (MZ-1U05)

The figure below shows the condition when the MZ-1U05 Expansion Slot is installed to the MZ-5500/5600 series.

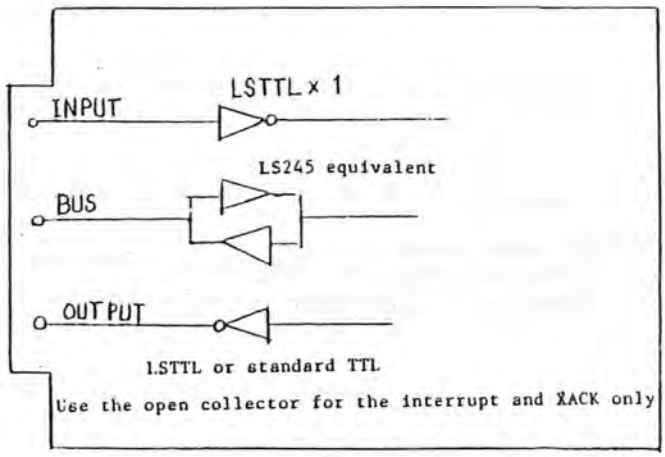


Board inserted in the slot

Since all signal lines are arrangement common for all slots, it is possible to insert the board in any slot, with exception for the HD interface board which should be inserted in the slot-1 or slot-3. In this event, the guide tab between the slot-1 and slot-3 must be removed.

Slot signal line interface

I/O signal lines of the board to be inserted in the slot must be treated as follows:



*See the hardware information for terminal arrangement and board size.

Current limit for slot (MZ-5500 series)

	VCC(+5V)	VDD(+12V)	VGG(-12V)
Per slot	500mA	50mA	10mA

5-2. Expansion signal description (common for the MZ-5500 and MZ-5600)

<table>
<tr><th>Signal name</th><th>In/Out</th><th>Function</th></tr>
<tr><td>A0-A19</td><td>Out</td><td>°Memory, I/O address signal which represents:
$\overline{IOACC}$=1: Memory address
$\overline{IOACC}$=0: I/O address
°A0 functions the same as $\overline{BHE}$ for low order byte (D0-D7) of the data bus.
°Pay attention to it that an invalid address may be issued at a time when addressing signal changes.</td></tr>
<tr><td>D0-D15</td><td>In/Out</td><td>°A 16-bit data signal which is used for transfer between the CPU and the memory or the I/O, or, data transfer between the memory and the I/O during DMA.</td></tr>
<tr><td>$\overline{MRDC}$</td><td>Out</td><td>°Memory read signal.</td></tr>
<tr><td>$\overline{MWTC}$, $\overline{AMWC}$</td><td>Out</td><td>°Memory write signal.
°The $\overline{MWTC}$ signal is shorter by one CPU clock than the $\overline{AMWC}$ signal, and the write data is established at a high to low transition of the signal.
°During DMA, these two signals are issued at the same timing.</td></tr>
<tr><td>$\overline{IORC}$</td><td>Out</td><td>°I/O read signal.</td></tr>
<tr><td>$\overline{IOWC}$, $\overline{AIOWC}$</td><td>Out</td><td>°I/O write signal.
°The $\overline{IOWC}$ signal is shorter by one CPU clock than the $\overline{AIOWC}$ signal, and the write data is established at a high to low transition of the signal.
°During DMA, these two signals are issued at the same timing.</td></tr>
<tr><td>$\overline{INTA}$</td><td>Out</td><td>°Interrupt acknowledge signal from the CPU.</td></tr>
<tr><td>$\overline{IOACC}$</td><td>Out</td><td>°The signal used to indicate that the CPU is accessing the I/O. The memory decoder must be enabled with $\overline{IOACC}$=1 and the I/O decoder must be enabled with $\overline{IOACC}$=0.</td></tr>
<tr><td>MA0-MA2</td><td>Out</td><td>°Bank select signal for the memory address, A0000H-BFFFFH. Each bank is used in the following manner:
<table>
<tr><th>MA0</th><th>MA1</th><th>MA2</th><th></th></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Reserved</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Not used</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Not used</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Not used</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Not used</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Not used</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Not used</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Not used</td></tr>
</table></td></tr>
<tr><td>$\overline{XACK}$</td><td>In</td><td>°Ready signal returned from the device which is mapped on the $\overline{XACK}$ area of the memory map and I/O map.
°Must be driven by the open collector to perform wired-OR.</td></tr>
</table>

Signal name	In/Out	Function
$\overline{IR-22}$-$\overline{IR-26}$	In	°Interrupt request input from the device on the I/O slot. IR-22 For HD interface IR-23 For SFD interface IR-24 Not used IR-25 Not used IR-26 For user's use
$\overline{DACK2}$	Out	°System RAM refresh signal.
$\overline{DREQ0}$, $\overline{DREQ3}$	In	°DMA transfer request and acknowledge signal.
$\overline{DACK0}$, $\overline{DACK3}$	Out	°Channel 0 for the hard disk and the channel 3 for the standard floppy disk.
CLK86, CL4M $\overline{OSC}$	Out	°CLK86 is the CPU clock which is 4.9152MHz with the MZ-5500 and 8MHz when the system switch-5 is set off and 4.9152MHz when the switch-5 is set on with the MZ-5600. It is a narrow high period clock of 1/3 duty. °CLK4M is 4MH and $\overline{OSC}$ is 14.7456MHz clock.
RESET	Out	°Power-on-reset signal which is normally low.
$\overline{RSTSW}$	Out	°The signal is forced low while the front panel RESET switch is kept depressed. At the moment the switch is pushed, an NMI is issued to the CPU.

*See the next page for the timing chart.

5-3. I/O address setup

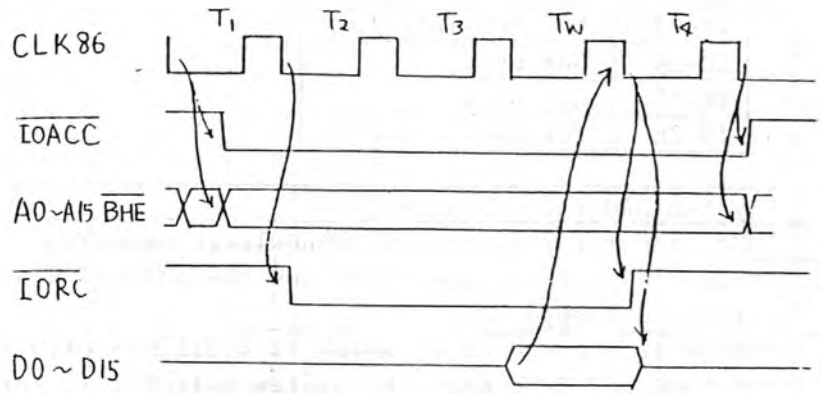
When an I/O port is to be expanded on the expansion slot by the user, the port address must be set as in the table below in reference to the specification such as accessing time of the device to be used.

Access time from IORC (tACC)	Port address
tACC $\leq$ 300ns	180H - 1BFH
300ns $<$ tACC $\leq$ 550ns	300H - 33FH
550ns $<$ tACC $\leq$ 100us	3C0H - 3FFH

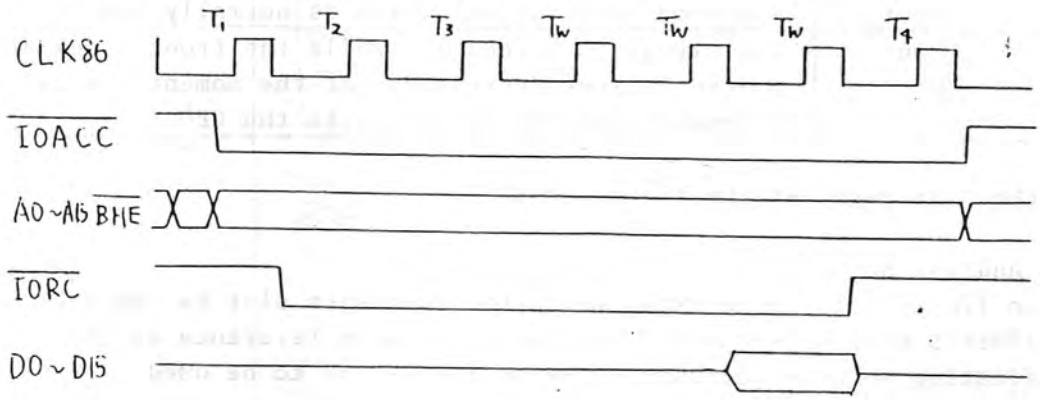
*Because the access time shown in the table is just for reference, it will need more study before the actual designing.

5-4. I/O slot timings

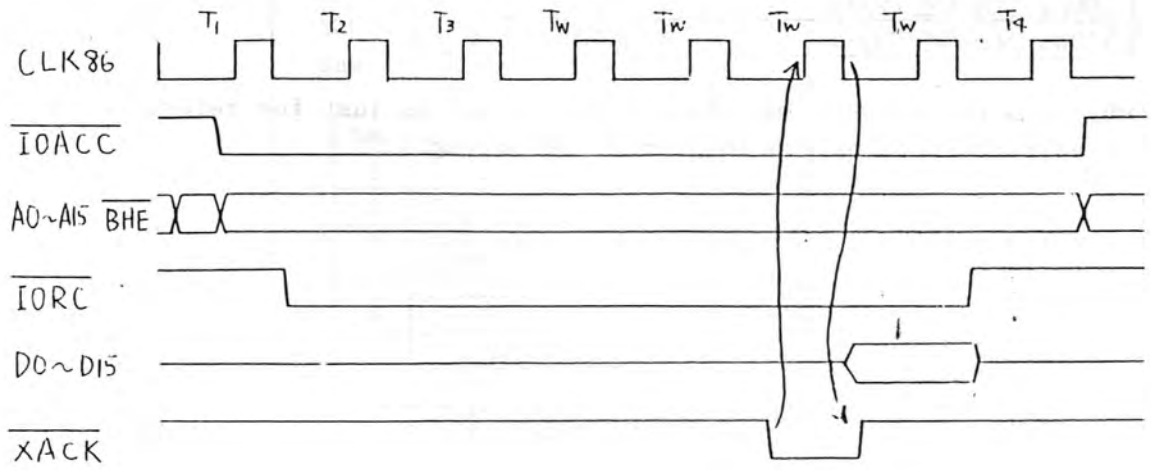
1) I/O read, 8MHz, 1 wait (I/O address: 180H - 1B0H)



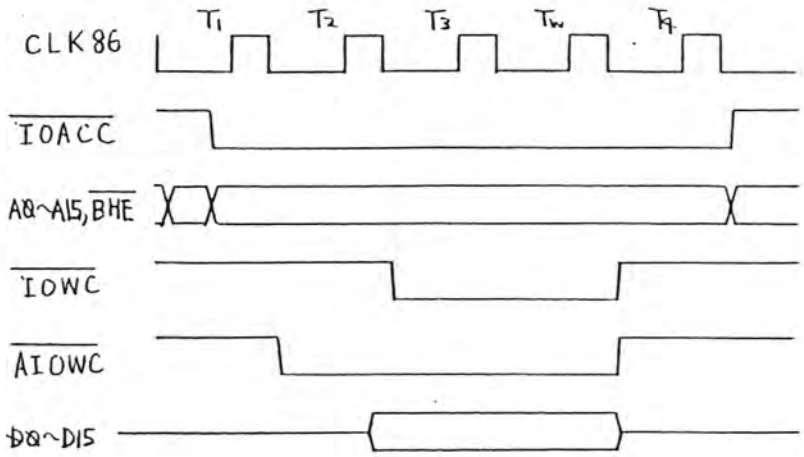
2) I/O read, 8MHz, 3 waits (I/O address: 300H - 33FH)



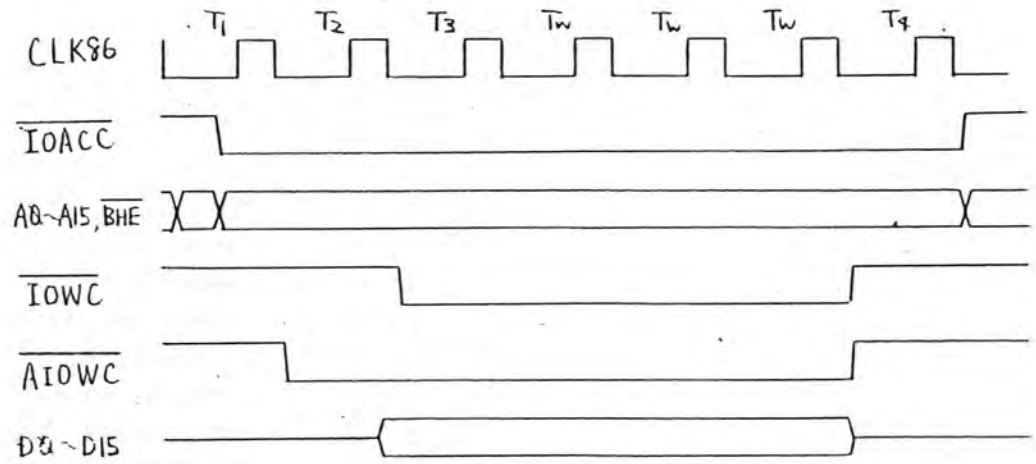
3) I/O read, 8MHz, XACK (I/O address: 3C0H - 3FFH)



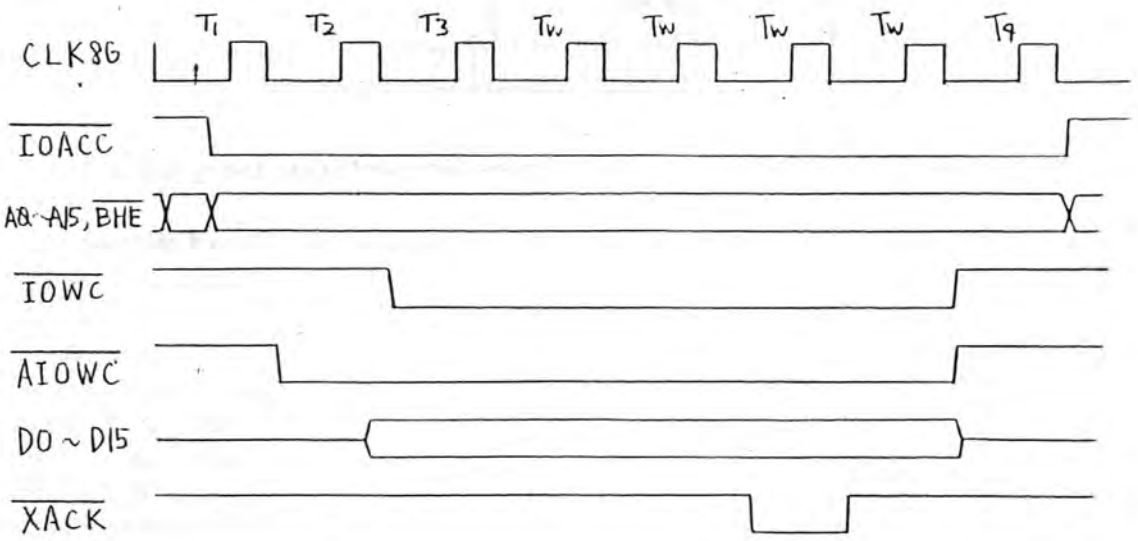
4) I/O write, 8MHz, 1 wait (I/O address: 180H - 1B0H)



5) I/O write, 8MHz, 3 waits (I/O address: 300H - 33FH)

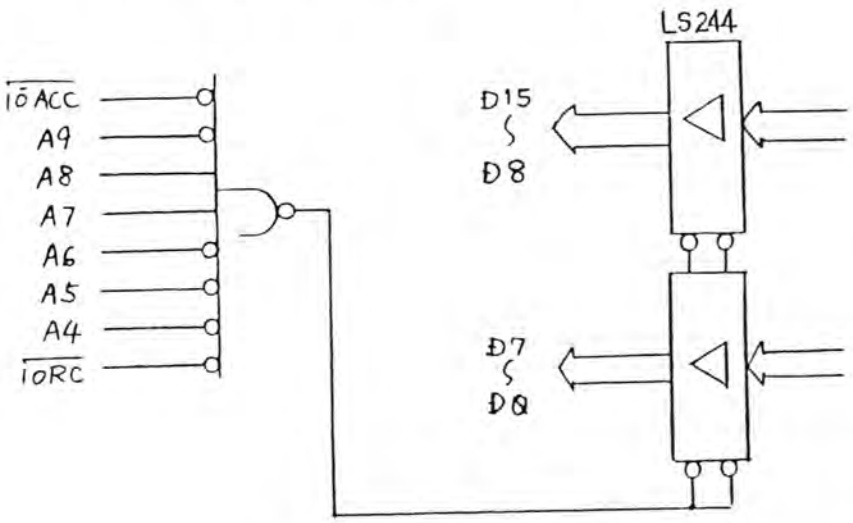


6) I/O write, 8MHz, $\overline{\text{XACK}}$ (I/O address: 3C0H - 3FFH)



5-5. I/O port interfacing examples (user's job)

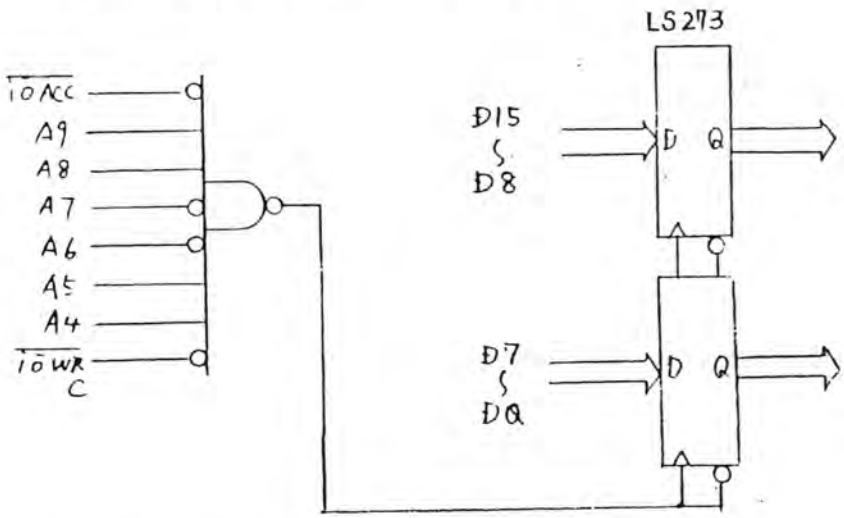
(1) 16-bit input port (I/O address: 180H)



Machine language programming example:

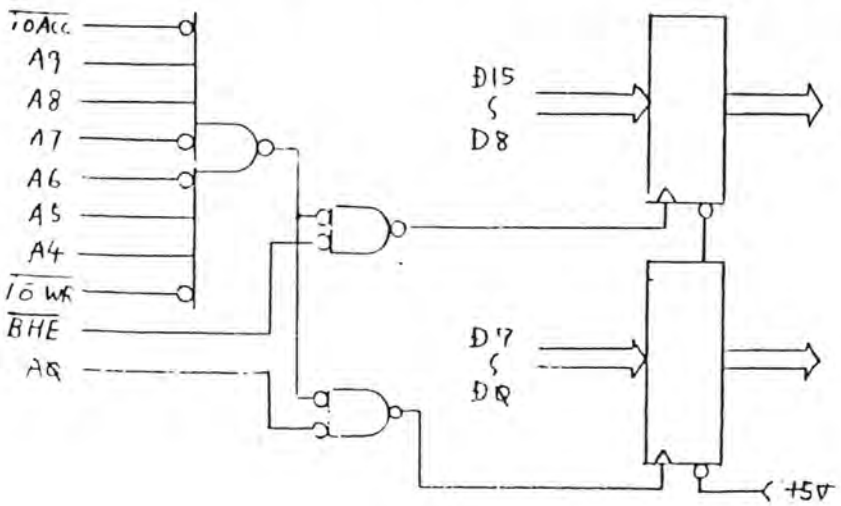
°Word input
```
MOV  DX, 180H
IN   AX, DX
```
°Low order byte input
```
MOV  DX, 180H
IN   AL, DX
```
°High order byte input
```
MOV  DX, 181H
IN   AL, DX
```

(2) 16-bit output port (I/O address: 320H)
°When only word write is done



°Word output
```
MOV  DX, 180H
MOV  AX, ——
OUT  DX, AX
```
°Insignificant data will be stored in the other byte when the byte write is done.

(3) When the high order and low order bytes are written independently



°Word output
```
MOV  DX, 180H
MOV  AX, ——
OUT  DX, AX
```
°Low order byte output
```
MOV  DX, 180H
MOV  AL, ——
OUT  DX, AL
```
°High order byte output
```
MOV  DX, 181H
MOV  AL, ——
OUT  DX, AL
```

6. DMA (*1)

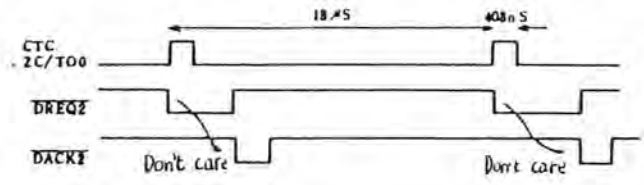
6-1. DMA control with MZ-5500/5600

A different bus privilege acquiring method is used for the 8086 maximum mode and minimum mode. In the minimum mode, the use of the bus is requested with HOLD by the peripheral unit, and granted with HLDA by the 8086. In the maximum mode, the peripheral unit first sends the bus request pulse $\overline{RQ}$ to the $\overline{RQ}/\overline{GT}$ line, to which the 8086 sends the $\overline{GT}$ pulse on the same line to grant the request. When the bus has been released from the use, the peripheral unit sends a release pulse on the same line.
With the MZ-5500/5600, the DMAC is used for data transfer between the disk and the memory and for DRAM refreshing. The hold request sequence of the 8237A(*2) is suitable for the minimum mode of the 8086. But it has to be converted into HOLD and HLDA of the 8237A since the 8086 must be operated in the maximum mode in order to interface with the 8087 Coprocessor. As this conversion circuit is rather complicated, the conversion is done in the following manner. When receiving HOLD from the 8237A, the 8086 recognizes it at the end of the bus access cycle or in the idle cycle, and returns HLDA. Simultaneously, it is put into the non-ready condition and separated from the wywtem bus, during which time the 8237A executes DMA transfer, and, upon completion, releases HOLD. In this manner, the 8237A deprives the CPU of the bus for six clocks. If the CPU goes into the bus cycle after receiving HOLD, waits are inserted for six clocks at the maximum, and accessing is continued thereafter as if nothing happened.

As four channels are provided for the 8237A; channel 1 for the MFD, channel 2 for the RAM refresh, and channels, 0 and 3, for the I/O slot (expansion slot), it is expected to use the channel 0 for exclusive use of the hard disk and the channel 3 for other device. Discussion will be provided separately in regard to the channel 3.
Although there are several modes for the DMA transfer with the 8237A, the single transfer mode must be used in order to assure proper refreshing.

6-2. Operational theory

The 8237A Programmable DMA Controller has four independent DMA channels. The channel 1 is for the standard MFD interface in which the DREQ delay circuit is provided to meet the specification from DREQ to $\overline{IORD}$ of the FDC(*3). The channel 2 is for refresh of the system RAM which is refreshed as the CTC reads DRAM by means of a request at every 13 microseconds.



(*1): DMA
It is a short words for Direct Memory Access which the memory is read, written, and refreshed without intervention of the CPU.
(*2): 8237A
It is the DMA controller which has four independent channels.
(*3): FDC
It is a short words for Floppy Disk Controller.

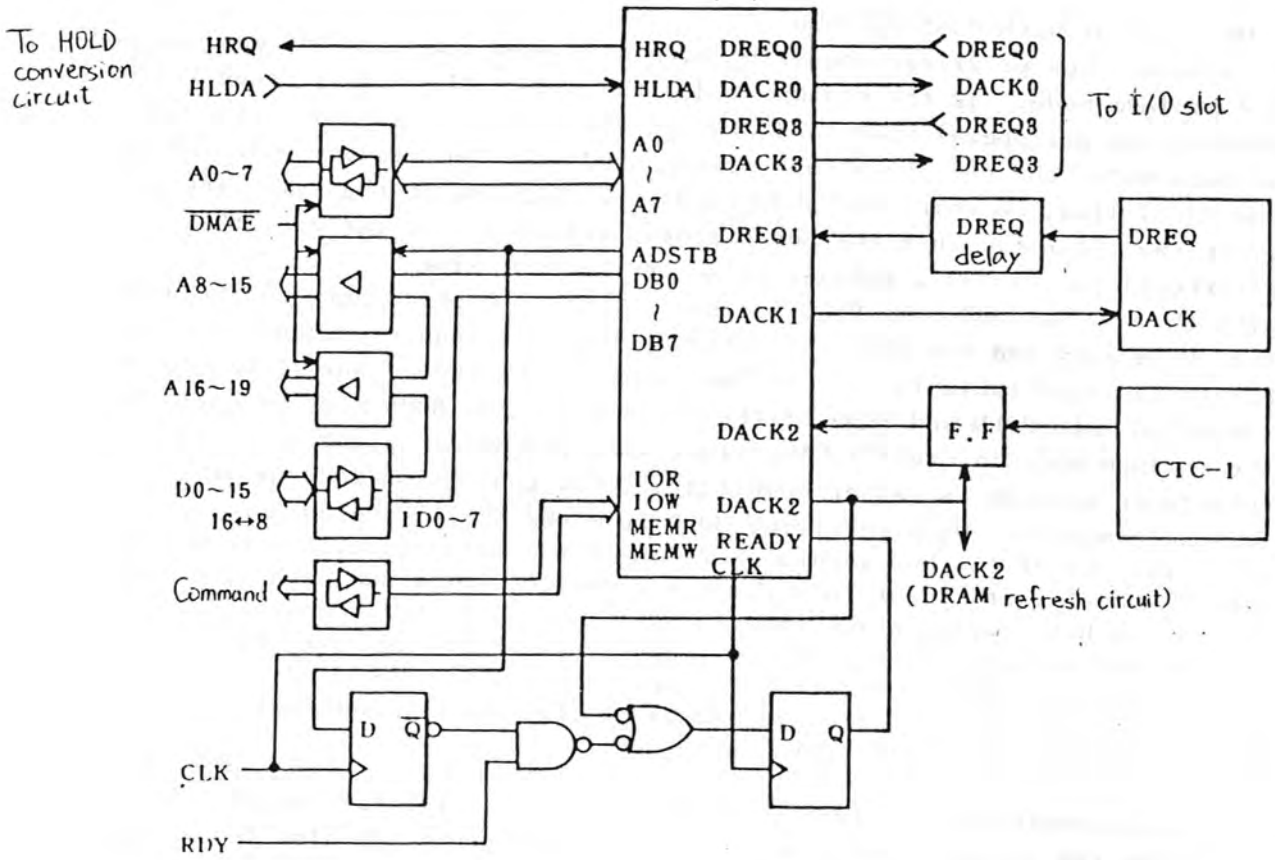
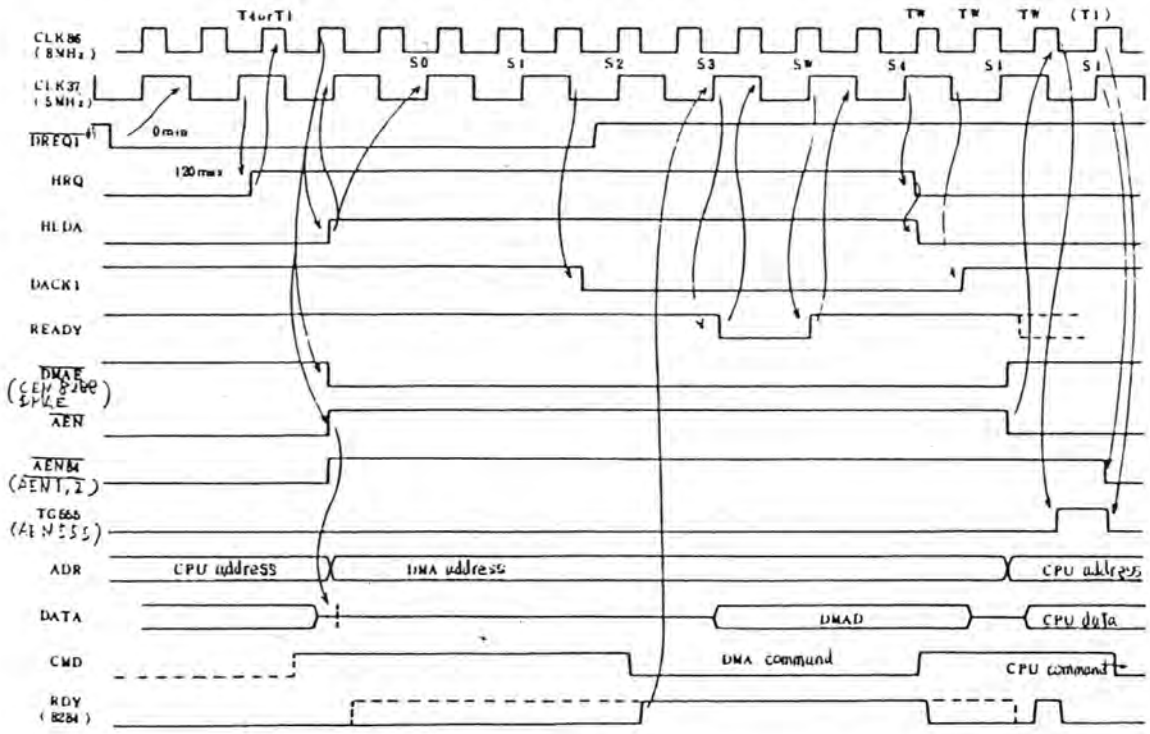


Fig.6-1 DMA circuit block diagram

°DMA channel 1 (SW is not used for the channel 2)



°Since some of signal names differs between the MZ-5500 and MZ-5600, the signal name given parenthesized is for the MZ-5500.
°The CPU clock CLK86 and the DMA clock CLK37 are completely async clocks.

Fig.6-2 DMA timing

Upon receiving of DREQ from a channel, the DMAC issues the hold request signal (HRQ) to the CPU. As the HOLD conversion circuit receives this signal, it makes the CPU in the non-ready state and the system bus is released. At the same time, the hold acknowledge signal (HLDA) and the DMA enable signal (DMAE) are returned to the DMAC to perform the DMA transfer. The 8237 DMAC controls DMA transfer of any 16-bit area (64KB) represented by address signals, A0 - A7, and A8 - A15 which latch DB0 - DB7 with ADSTB at the beginning of the DMA transfer. Also, 1D4 - 7 latch signals of I/O (50H) are used as A16 - A19 in order to cover up the 1MB memory address space of the 8086 CPU.
The DMAC goes ready with the DMA transferred memory ready signal, but the ready signal returned with 0 wait is automatically attached with 1 wait. However, it is 0 wait at all time during refreshing.

6-3. Use of DMA channel 3

For the MZ-5500/5600 series, four DMA channels are provided standard. Since the channels 1 and 2 are already used by the machine, channels 0 and 3 are open for the I/O slot. However, the channel 0 is used for the hard disk interface and the channel 3 is reserved for the standard floppy disk interface.

The channel 3, however, permits multiple-DMA up to eight levels (Table below). Attention must be paid to the following conditions when performing direct data transfer with the main memory by means of DMA.

Ch 0		Hard disk interface	
Ch 1		MFD interface	
Ch 2		Main memory refresh	
Ch 3	A	Reserved	I/O AEH to 01H
	B	Reserved	I/O AEH to 02H
	C	SFD interface, MFD interface	I/O AEH to 04H
	D	Reserved	I/O AEH to 08H
	E	Reserved	I/O AEH to 10H
	F	Reserved	I/O AEH to 20H
	G	Reserved	I/O AEH to 40H
	H	User	I/O AEH to 80H

1) Hardware

(1) Channel 3H is used for the DMA channel.

(2) Only byte transfer mode is applicable for the DMA transfer.

(3) $\overline{\text{DREQ3}}$ (channel 3 DMA request) must be outputted by the open collector as it is wired-OR.

(4) Provide an output port to the bit 7 of the I/O address 0AEH to permit input through the bit 7 of the I/O address 0AFH.

(5) $\overline{\text{DREQ3}}$ and $\overline{\text{DACK3}}$ are gated by the above output port.

(6) $\overline{\text{DREQ3}}$ must be maintained active until $\overline{\text{DACK3}}$ is returned.

(7) System data bus, D8 - D15, must be pulled up with a proper resistance.

(8) Some means must be provided to know a DMA termination (interrupt, for instance).

ii) Software

(1) Since the user DMA is not at all supported by the OS, the user program must be developed by the assembler.

(2) Assign only the channel 3 for the DMAC. Never reset and mask the channel 2 with the master clear command, for example.

(3) Before the DMA, send 80H to the I/O address AEH to open the user DMA.

(4) 64KB is the maximum that can be subjected to DMA at one time.

(5) Assign the single transfer mode for the DMA operation.

Circuit example

The analog waveform is converted into the digital signal via the A/D converter, and data of 32KB are transferred to the main memory area, 40000H to 47FFFH at every 100 microseconds.

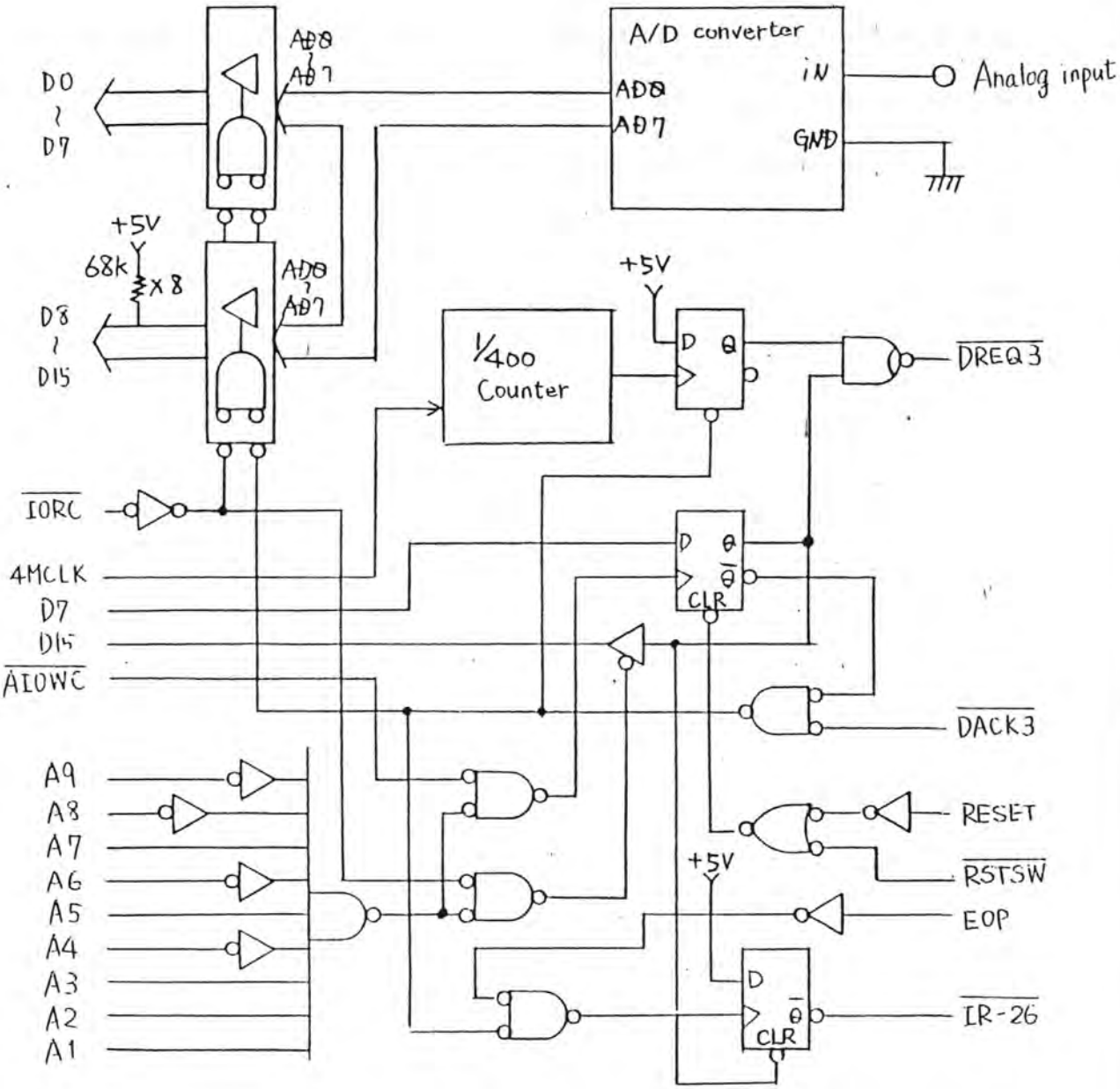
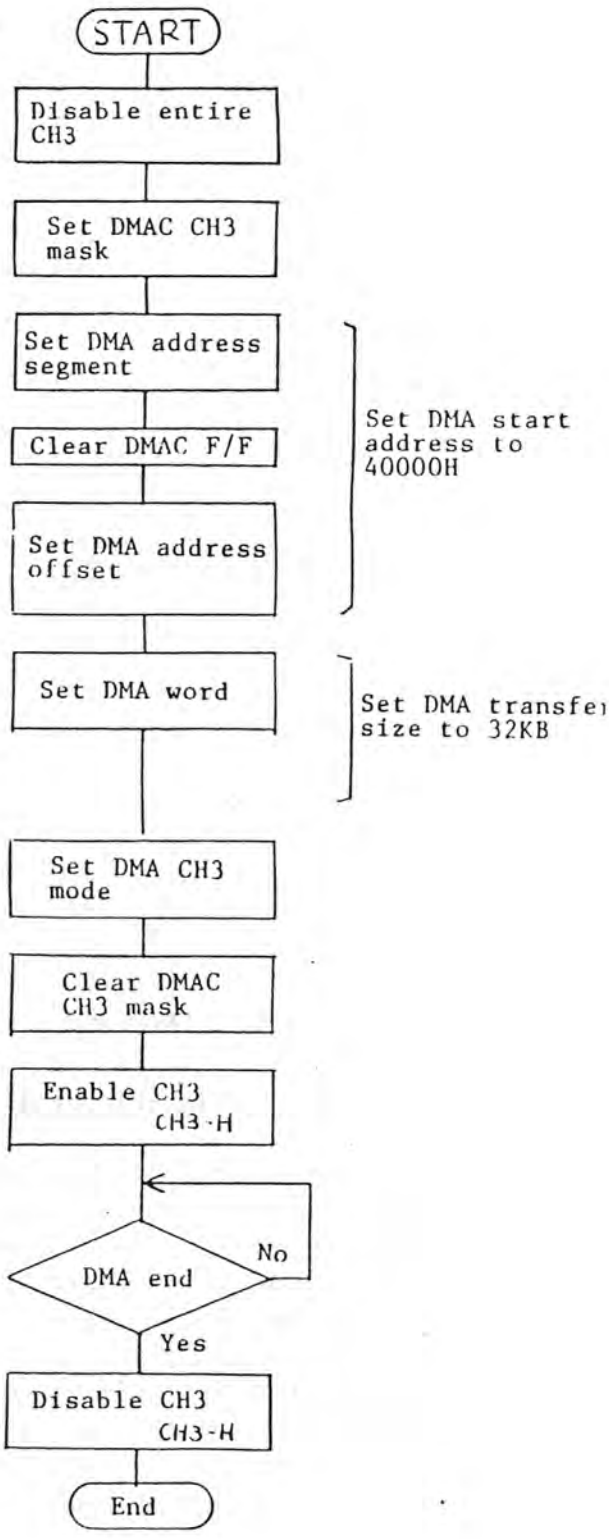


Fig.1 Circuit example

°Software (in reference to the circuit example in the preceding page)

```
        CSEG
        ORG   100H
        MOV   AL, 0
        OUT   0AEH, AL

        MOV   AL, 07H
        OUT   0AH, AL

        MOV   AL, 40H   ;Only high order
        OUT   50H, AL   ;4 bits are valid

        OUT   0CH, AL

        MOV   AL, 0
        OUT   06H, AL
        OUT   06H, AL

        MOV   AL, 0FFH
        OUT   07H, AL
        MOV   AL, 7FH
        OUT   07H, AL

        MOV   AL, 47H
        OUT   0BH, AL

        MOV   AL, 03H
        OUT   0AH, AL

        MOV   AL, 80H
        OUT   0AEH, AL

L1:     IN    AL, 40H
        AND   AL, 40H
        JZ    L1

        MOV   AL, 0
        OUT   0AEH, 0

        XOR   CX, CX
        XOR   DX, DX
        INT   224

        END
```



*1: $\overline{\text{IR-26}}$ is used simply as an input port.

7. Mini-floppy disk interface

7-1. General description (MZ-5500)

Every MZ-5500 series personal computer is equipped with a 320KB (formatted) mini-floppy disk interface which can control up to a maximum of four mini-floppy drive units. As there is a mini-floppy disk expansion interface connector on the back of the machine, it permits external installation of two more drives for the MZ-5511 that has one internal drive unit and the MZ-5521 that has two internal drive units. The MZ-5501 that has no internal drive unit permits expansion with the internal disk drive unit or four external drive unit.

Fig.7-1 shows the block diagram of the mini-floppy disk circuit.

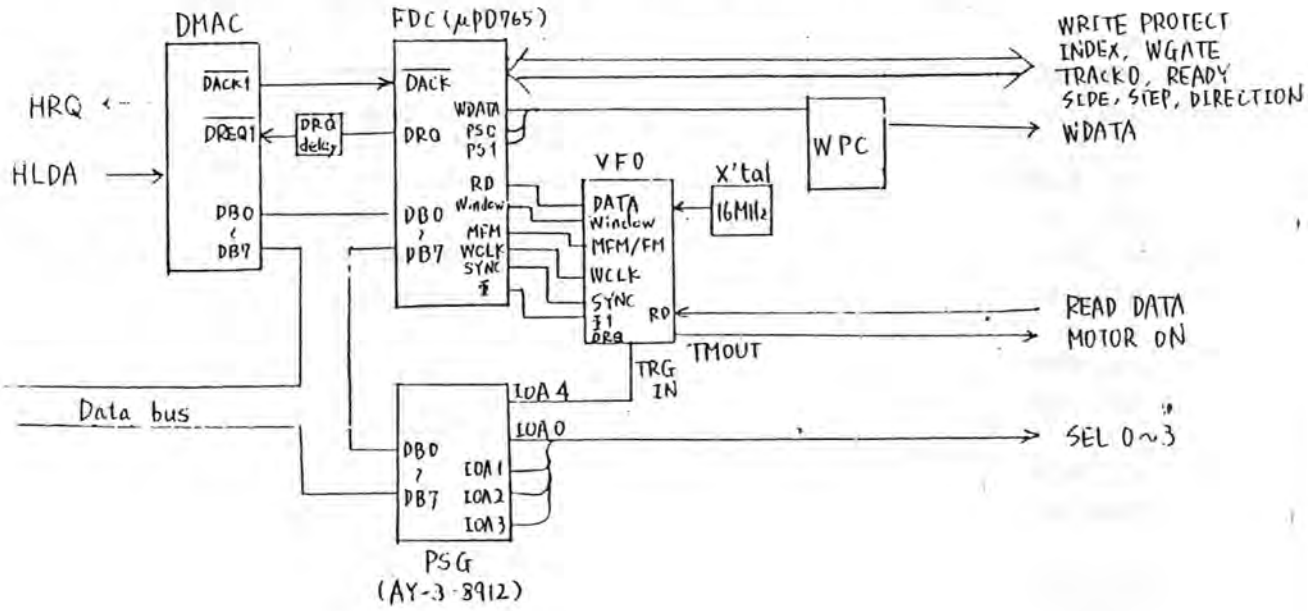


Fig.7-1 Mini-floppy disk interface block diagram

The recording surface of the mini-floppy disk is divided into forty tracks along the radius (Fig.7-2). Track number begins from 0 and ends at 39 on both sides and sector number are assigned from 1 to 16 on both sides. A specific point on the disk is represented with the track number and the sector number. It permits to record 256 bytes in one sector and read/write is possible in terms of sector.

Fig.7-2 also shows the soft sector. In the ID field is recorded the address (track, side, sector) of the sector. The information in this ID field is used to read/write data. The ID field is created during formatting (initialization).

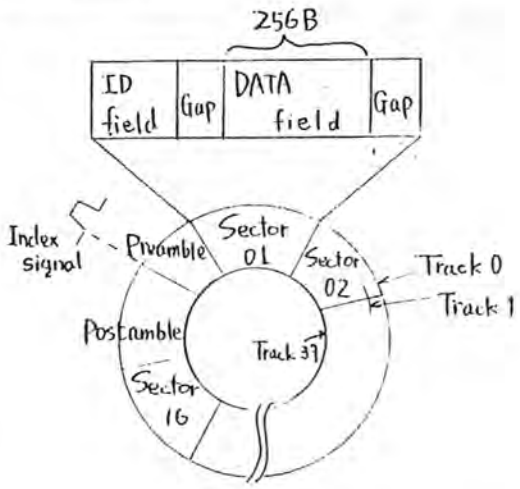


Fig.7-2 Disk and software sector example

The MFD drive unit has three major actions of write, read, and seek which are directly controlled by the μPD765 Floppy Disk Controller (FDC) shown in Fig.7-1. As the side of disk (front or reverse side), track, sector, and command (write, read, seek) to the FDC are specified from the CPU by the software, the FDC automatically controls the MFD drive unit.
The 8237 DMAC is used to transfer read/write data between the FDC and the memory to perform fast DMA transfer. The following are required in order that the FDC reads from or writes to the disk.

(1) The DMA request signal (DRQ) is issued from the FDC to the DMAC and VFO/data separator (*1).
(2) As the DMAC receives DRQ, HRQ (request) is sent from the DMAC to the CPU.
(3) As the CPU receives HRQ, the bus line is opened, and HLDA is returned. To which the DMAC returns DACK to the FDC.
(4) Data are transferred between the memory and FDD via FDC under the bus control by the DMAC.

The receive circuit from the MFD drive to the FDC is simplified by the use of the SED 9420 VFO/Data Separator IC . As it internally incorporates the window clock (*2) by which the read data signal is fetched from the floppy disk drive which is then divided into the clock pulse and data pulse and the timer circuit. This controls the MFD motor stop signal.
MFD drive select signal is sent out through the I/O port which is incorporated in the AY-3-8912 Programmable Sound Generator (PSG).

*1): VFO *2): Window
Read data output from the MFD are composed of the data pulse and the clock pulse, and they must be separated from each other by the reliable data window, in order to obtain the data of a low error rate. It is the VFO circuit that is designed for that purpose. Read data input from the MFD delivered by the VFO is rearranged to the mid-point of the window, before being sent out as a data signal.

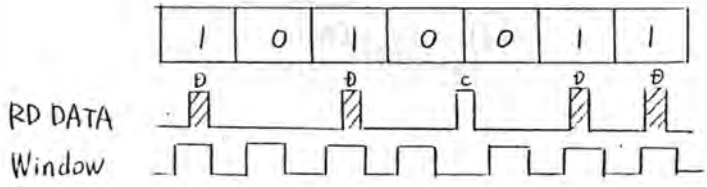


Table 7-1 FDD specification

Recording capacity (formatted)	: 320KB
Sectors	: 16 sectors/track
Tracks	: 40 tracks/side
Recording surface	: Two sides
Track density (TPI)	: 48
Recording density (BPI)	: 5876 (max)
Data transfer rate	: 250KB/s
Recording method	: MFM
Transfer method	: MFM
Access time:	
Average	: 93ms
Track to track	: 6ms
Settling	: 15ms
Head load mechanism	: None (head load time=0)

7-2. MZ-5600 MFD (640KB) interface general description (MZ-5600)

Since the MZ-5600 series are equipped with a large capacity mini-floppy disk drive, the MFD interface for the MZ-5600 series is different from that for the MZ-5500 series in detail.

The MFD interface can control up to four units of the MFD drives and, in addition, the MZ-5600 has the expansion MFD interface connector on the back of the machine which permits expansion of two more units of the external MZ-1F13 mini-floppy disk drive options. The MZ-5631 permits internal expansion with the MZ-1F15 mini-floppy disk drive.

When using the 640KB (2DD) disk on the MZ-5600, it is possible to read from and write to the disk. However, when using the 320KB disk, only reading is possible as it is designed to read the disk which has been created by other model of personal computers such as the MZ-5500. To read the 320KB disk, "0" must be specified for the FD logical number. For more details, refer to the CP/M-86 and MS-DOS manuals.

In the case of the 640KB mode, the disk recording surface is divided into 80 tracks along the radius of the disk as shown in Fig.7-3. Track numbers from 0 to 79 are provided for both sides of the disk, respectively. Sector numbers from 1 to 16 are assigned on each side. Track number and the sector number are used altogether to represent the specific disk location. 256 bytes of data can be stored in one sector, and read/write is permitted in terms of sector. Fig.7-3 indicates the soft sector. Sector address information (track, side, sector) is contained in the ID field which is searched for when reading or writing data. The ID field is created at the time of disk formatting (initialization).

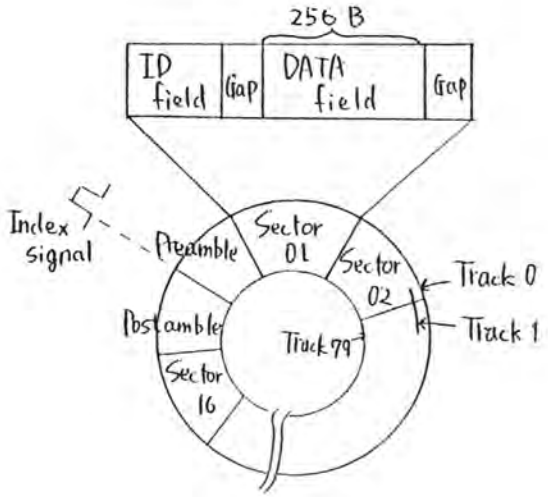


Fig.7-3 Disk and software example (640KB)

Fig.7-4 shows the block diagram of the MFD interface.
The MFD drive unit has three major actions of write, read, and seek which are directly controlled by the μPD765 Floppy Disk Controller (FDC). As the side of disk (front or reverse side), track, sector, and command (write, read, seek) to the FDC are specified from the CPU by the software, the FDC automatically control the MFD drive unit.
The 8237 DMAC is used to transfer read/write data between the FDC and the memory to perform fast DMA transfer.

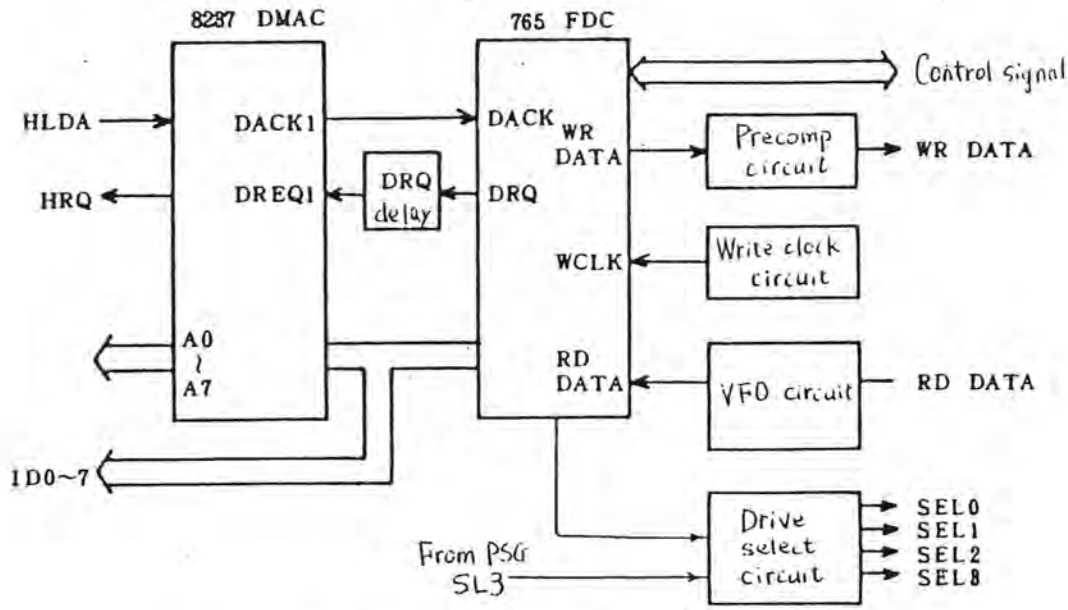


Fig.7-4 MFD interface block diagram

The following are required in order that the FDC reads from or writes to the disk.

(1) The DMA request signal (DRQ) is issued from the FDC to the DMAC and VFO/data separator (*1).
(2) As the DMAC receives DRQ, HRQ (request) is sent from the DMAC to the CPU.
(3) As the CPU receives HRQ, the bus line is opened, and HLDA is returned. To which the DMAC returns DACK to the FDC.
(4) Data are transferred between the memory and FDD via FDC under the bus control by the DMAC.

The receive circuit from the MFD drive to the FDC is simplified by the use of the HA16632AP VFO/Data Separator. As it internally incorporates the window clock by which the read data signal is fetched from the floppy disk drive which is then divided into the clock pulse and data pulse and the timer circuit.
MFD drive select signals, SEL0 - 2, are sent out from the FDC and only SEL3 is sent out through the I/O port which is incorporated in the AY-3-8912 Programmable Sound Generator (PSG).

Table 7-2 640KB FDD specification

Recording capacity	: 640KB
Sectors	: 16 sectors/track
Tracks	: 80 tracks/side
Recording surface	: Two sides
Track density (TPI)	: 96
Recording density (BPI)	: 5922
Data transfer rate	: 250KB/s
Recording method	: MFM
Transfer method	: MFM
Access time:	
Average	: 94ms
Track to track	: 3ms
Settling	: 15ms
Revolutions (RPM)	: 300

8. Hard disk interface general description

Any of the MZ-5500/5600 series can be interfaced with the hard disk that has a formatted capacity of 10.7 B (one unit is equipped standard for the MZ-5645). Especially in the MZ-5645, a maximum of two hard disks can be installed via the internal hard disk interface.

MZ-5631/5641	MZ-1F10* (with the hard disk interface)
MZ-5645 (with an internal 10.7MB hard disk drive)	MZ-1F18* (without the hard disk interface)
MZ-5511/5521	MZ-1F10* (with the hard disk interface)

*MZ-1F18 is equipped with the drive unit only.

The MZ-5500/5600 hard disk has four disk recording surfaces as shown in Fig.8-1 and each surface consists of 320 tracks developed along the radius of the disk. Track numbers, 0 to 319, are assigned and sector numbers, 1 to 17, are assigned, to represents the specific location with the track number, sector number, and head number (0 to 3).
Fig.8-1 also shows the soft sector. In the ID field is contained the sector address information (track, head, sector) which is normally used to access the specified sector.

For better reliability, retrial is made possible. If recovery was not successful with retrial, correction (ECC) is automatically carried out to a burst data of up to eleven bits. In addition to it, alternate track is provided on Track 0 or Track 1 to permit to replace data or program by a whole sector, in case there is an unrecoverable damage in the disk such as a physical disk damage.
So, tracks actually usable are 317 tracks of track number 2 to 318, with the track number 319 being used for the test of the hard disk. The ID field, however, cannot be created by the user.

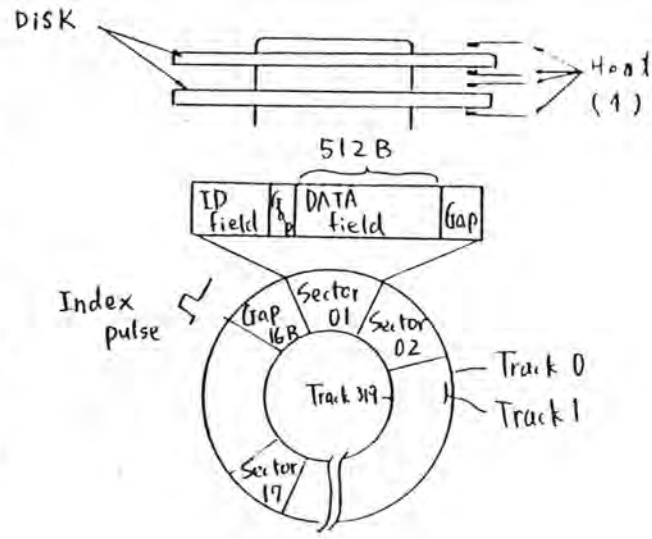


Fig.8-1 Disk and software sector example (physical)

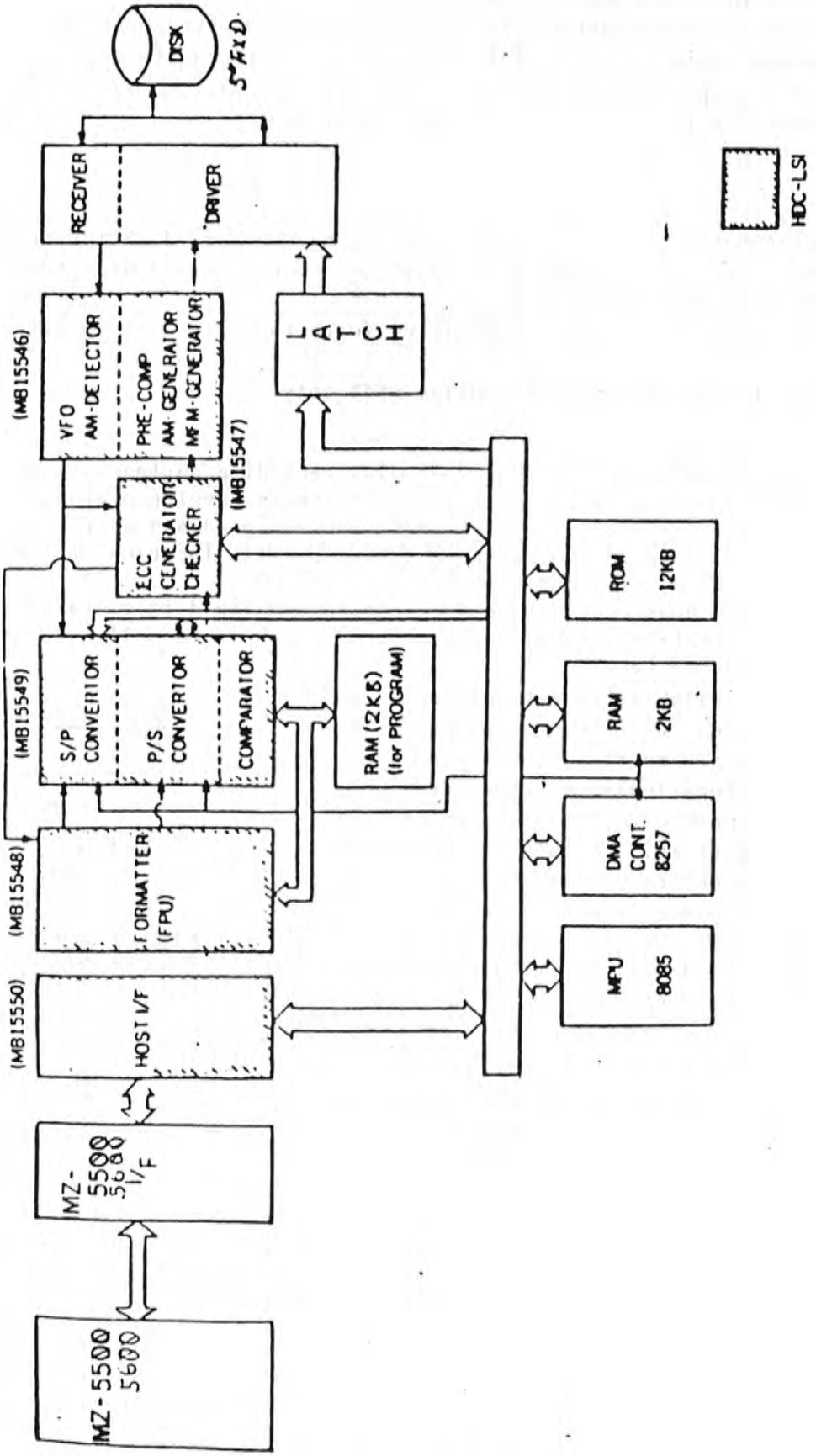


Fig. 8-2 HD block diagram

Fig.8-2 shows the block diagram of the hard disk interface. Similar to the MFD, action of the hard disk drive is divided into three major actions of write, read, and seek. Data transfer with the host is conducted in the DMA mode under the control of the 8237 DMAC. After data are set in the host interface chip internal register, the data are transferred to the M58725 RAM in the DMA mode, then the command is executed to the hard disk drive automatically by the firmware of the interface. This firmware automatically starts to test (ready, read/write, seek) the hard disk upon power on. If any error has been encountered during the test, the condition is displayed on the video unit by the OS.

Table 8-2 640KB FDD specification

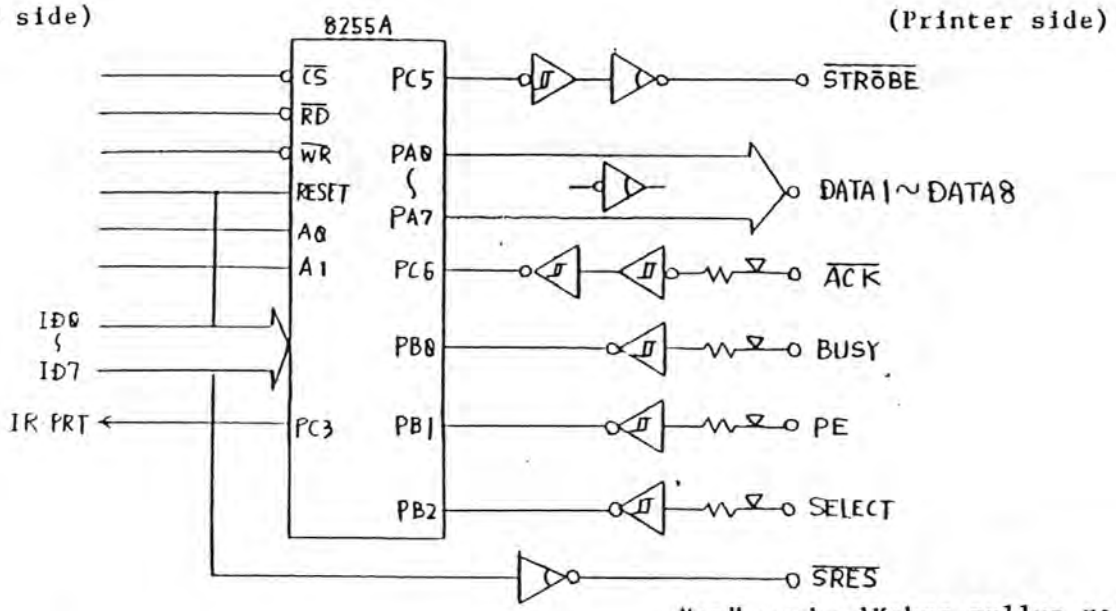
	(physical)	(CP/M-86 spec)
Recording capacity	: 10.7MB	(10.7MB)
Disks	: 2	
Heads	: 4	
Recording surfaces	: 4	
Cylinders	: 317	
Tracks	: 317 x 4 tracks	(673 x 2 tracks)
Sectors	: 17 sectors/track	(16 sectors/track)
Track density (TPI)	: 360	
Recording density (BPI)	: 9260, maximum	
Recording method	: MFM	
Transfer method	: MFM	
Data transfer speed	: 5MB/s	
Access time (including settling time):		
Average	: 85ms	
Minimum	: 18ms	
Maximum	: 15ms	

9. Printer interface

*Common for the MZ-5500 and MZ-5600.

9-1. Circuit description

The 8255A is used for the parallel interface controller which is operated under the following mode setup. For the Centronics interface, Group A of the 8255A is operated under the mode-1 and the $\overline{ACK}$ signal from the printer applies the interrupt to the CPU.

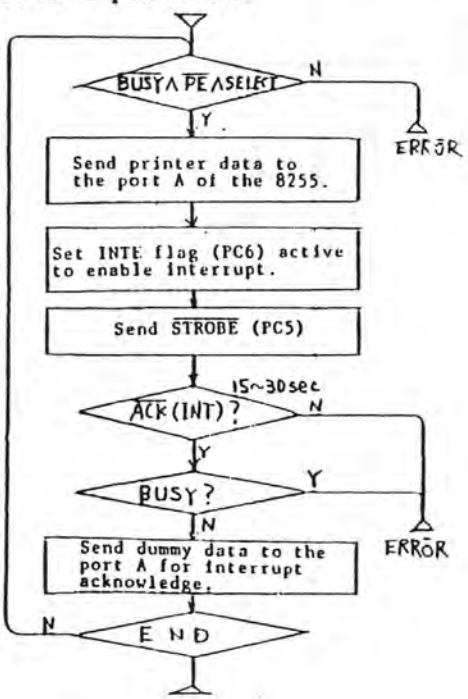


"▽" mark: 1Kohms pullup resistor

8255A mode

MODE1 output	PA0	
	I	
	PA7	
	PC7	
	PC6	$\overline{ACK}$
	PC5	OUT
	PC4	OUT
	PC8	INT
MODE0 output	PC2	OUT
	PC1	
	PC0	
MODE0 input	PB0	IN
	I	
	PB7	

°IOCS control procedure



*Centronics interface

Printer interface method which is popular worldwide.

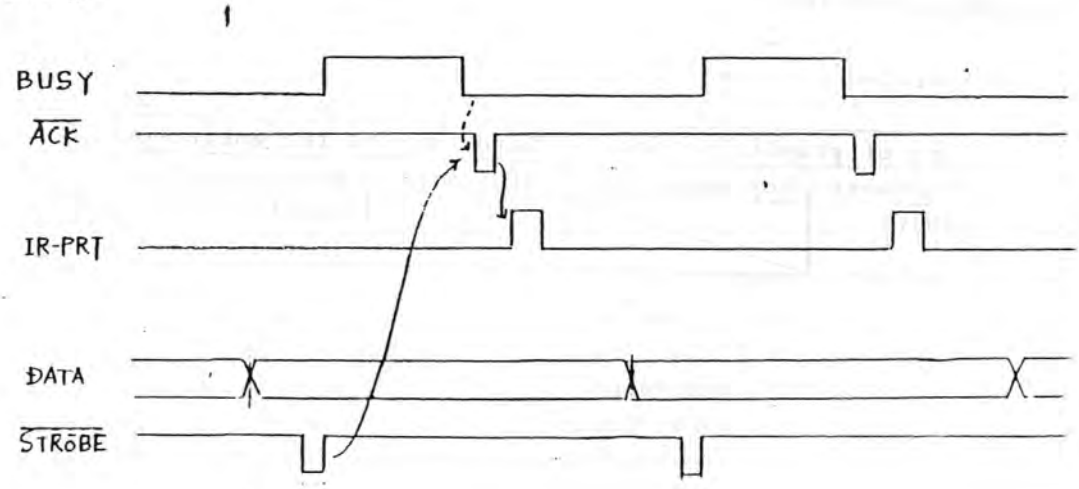
Parallel interface signal description

Pin No.	Signal name	In/Out	Function
1	$\overline{\text{STROBE}}$	In	The printer samples data at the rising edge.
2	DATA1	In	Data output to the printer.
3	DATA2		
4	DATA3		
5	DATA4		
6	DATA5		
7	DATA6		
8	DATA7		
9	DATA8		
10	$\overline{\text{ACK}}$	In	Completion of data or function input
11	BUSY	Out	Data receive enable (low)
12	PE	Out	Paper empty (high)
24	$\overline{\text{SRES}}$	In	Reset signal
25	SELCT	Out	Indicates the select (receive enabled) condition (high)

*14 - 23: GND

*18: Error insertion protected

Timings



9-2. Handling printer control code (function code)

As minor control functions are furnished to each MZ series printer, control is executed with the control code that follows the ESC code (1BH).

How to send a control code "XX (hex)"

BASIC operating the personal computer	Transmission of control code	Example: To send the code "1BH" and data "6" with the linefeed pitch set to 1/6"
MZ-3500 MZ-5500/5600 (BASIC-3)	PRINT CHR$ &XX	PRINT CHR$ & 1B;"6";

NOTE:
The machine language routine is required for the MZ-2000 series.

9-3. Making a hard copy of the video screen

Since the MZ-5500/5600 has the multiwindow capability, it can be copied on the printer with windows overlaid in the display screen.

°CP/M-86 and MS-DOS incorporated hard copy function

Push the [BREAK] key first. Push the [COPY] key in the wait state in which time the [CAPS] key is blinking. This will produce a hard copy of the display screen. This function is supported for the application software of the CP/M-86 and MS-DOS.

°BASIC incorporated hard copy function

	Copy of graphic screen		Hard copy of the entire screen	
	Statement	Key operation	Statement	Key operation
BASIC-3	GPRINT			[SHIFT] + [BREAK], then [COPY]

10. RS232C interface

Two channels of RS232C interface are provided standard for the MZ-5500 and MZ-5600 in order to permit a serial data transfer with a variety of peripheral devices. The RS232C is the standards set forth by EIA (Electronic Industries Association of the U.S.A.) for interfacing the modem (modulator/demodulator) with the communication control device, and serial binary digital data signals, control signals, and timing signals transferred between the modem and the data terminal.

The RS232C interface of the MZ-5500/5600 has been designed in compliance with these EIA requirements to make connection with the acoustic coupler, printer, plotter, etc. However, attention must be paid to it that even the device that has the interface that conforms to the RS232C requirements may not be connected satisfactorily depending on the case.

10-1. Specification

Input/output method	: RS232C bit serial input/output
Channels	: 2 channels Channel A (BSC conforming)* Channel B
Code used	: JIS 7-channel code system JIS 8-channel code system
Baud rate	: 110, 150, 200, 300, 600, 1200, 2400, 4800, 9600 BPS
Transmission method	: Half-duplex (Channel A and B)
Transmission control procedure	: Non-procedure
Data format	: 1 stop bit Parity option of even, odd, and non parity
Signal level	: High: +5 to +15V Low: -5 to -15V

*BSC

BSC is a short words for Binary Synchronous Communication which means the binary data synchronous data communication. It is the character type protocol for which a series of standard control characters and control characters are used for the synchronous binary data transmission between two stations of the data communication system. Though the following signals are provided in the hardware for the synchronous transmission, they are not supported by CP/M-86, MS-DOS, and BASIC.

*Since the Z-80 SIO is used for the serial interface, the specification of that LSI is attached at the end of this text.

10-2. Input/output signals and control signals

(1) Data input/output signals

Pin No.	Signal name	Signal symbol	In/Out	Function
2	Transmit signal	SD(TxD)	Out	Output data
3	Receive signal	RD(RxD)	In	Input data from device

↑
Those in parentheses are the EIA symbols.

(2) Control signals

Pin No.	Signal name	Signal symbol	In/Out	Function
1	Signal ground	SG		
4	Send request	RS(RTS)	Out	ON during data transmission. OFF when transmission is completed.
5	Transmit enable	CS(CTS)	In	The signal with which data output is permitted. Data transmission is enabled when ON. Data transmission is disabled when OFF. NOTE: Even when the signal is turned OFF from ON, a maximum of 2 bytes of data may be sended until transmission is completed.
6	Receive enable	READY (DTR)	Out	The signal which indicates whether data input is enabled. ON: Enabled. OFF: Disabled.
7	Signal ground	SG		
8	Data set ready	DR(DCD)	In	The signal which indicates whether the device is ready for the operation. ON: Operation enabled. OFF: Operation not enabled. When this signal goes OFF during the data input/output, it results in an error.
9	Signal ground	SG		
12	Terminal ready	ER	Out	The signal which indicates that the power is on to the machine. ON: Power on state

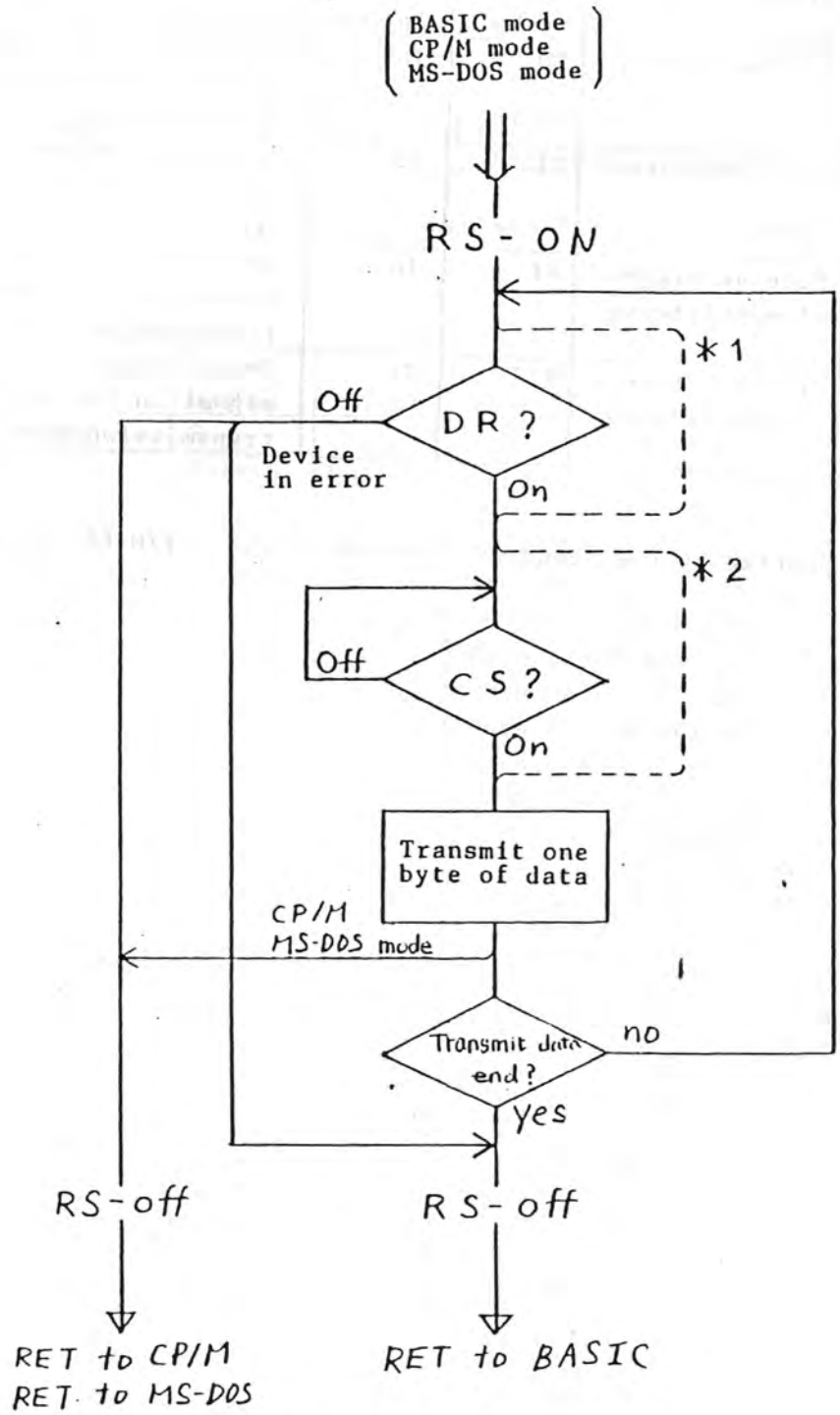
(3) Other control signals (channel A only)

Pin No.	Signal name	Signal symbol	In/Out	Function
10	Carrier detect	CD	In	The signal which indicates that the carrier is received by the device.
11	Call indicator	CI	In	The signal which indicates reception of the call signal from the line.
14	Receive signal element/timing	RT	In	Input signal element/timing signal in the synchronous transmission mode.
15	Transmit signal element/timing	ST2	In	Output signal element/timing signal in the synchronous transmission mode.

NOTE:
Not supported by the standard software (BASIC, CP/M-86, MS-DOS).

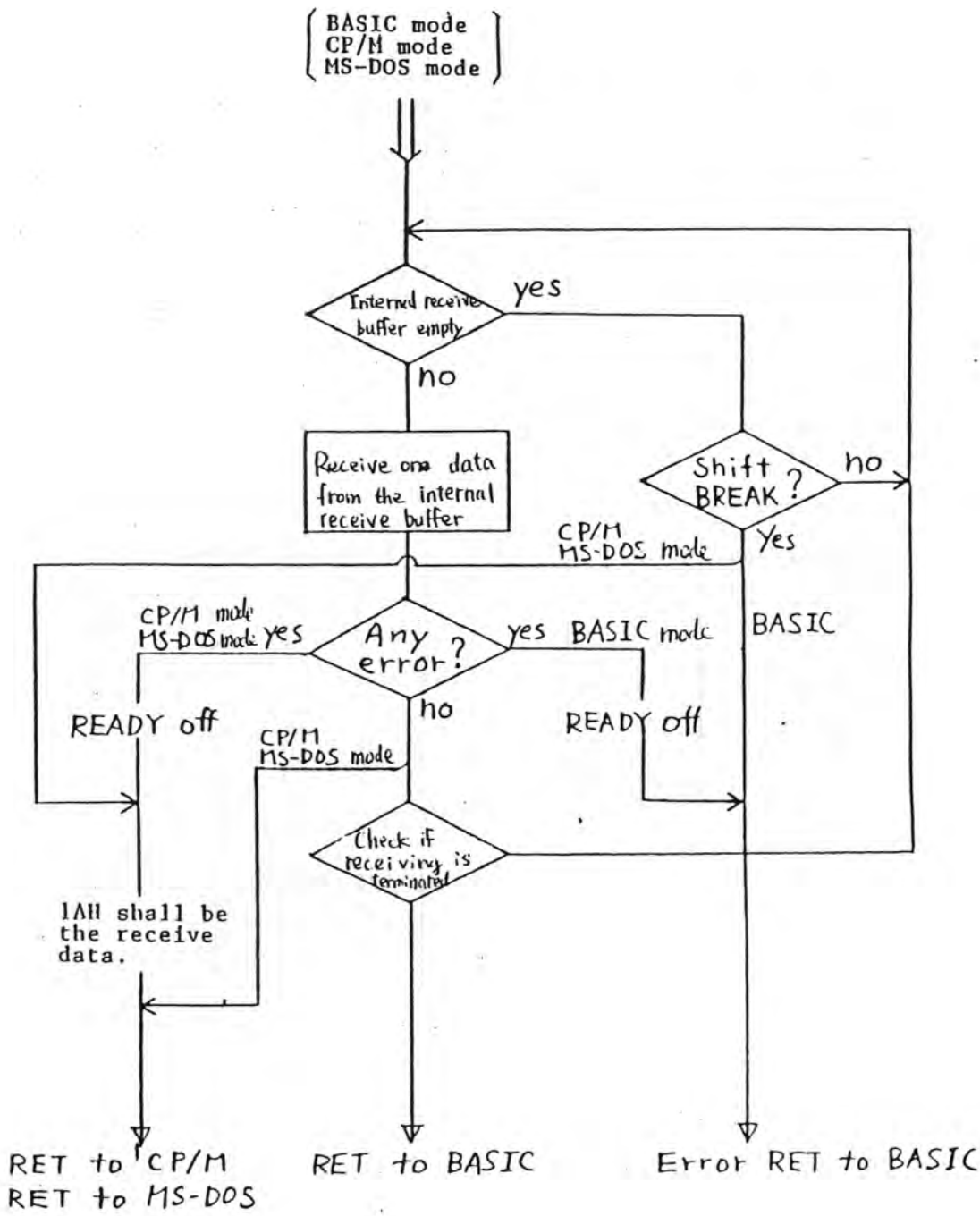
10-3. Process outline

Transmission



*1: When masked in the DR monitoring mode. See the CP/M or MS-DOS Manual.
*2: When masked in the CS monitoring mode. See the CP/M or MS-DOS Manual.

Receiving



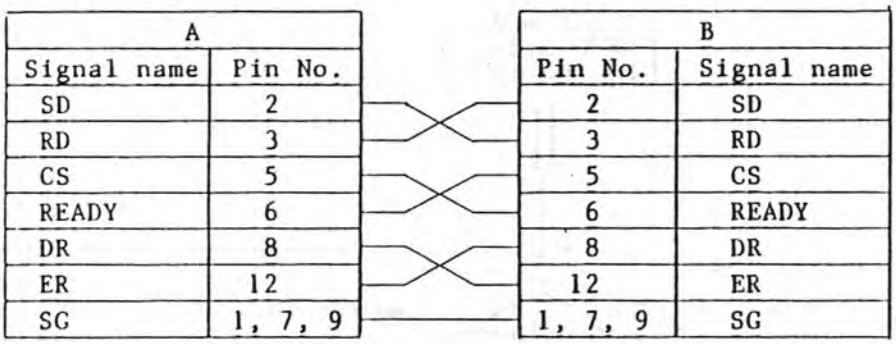
NOTES:
1. Data will be received in the divided mode.
   But, the data input when READY is OFF will be invalid.

2. Although READY goes OFF upon occurrence of a receive error in the CP/M mode, depression of the [CTRL-C] key clears the error.

10-4. Wiring example

(1) MZ-5500/5600 to/from MZ-5500/5600

(A) (B)



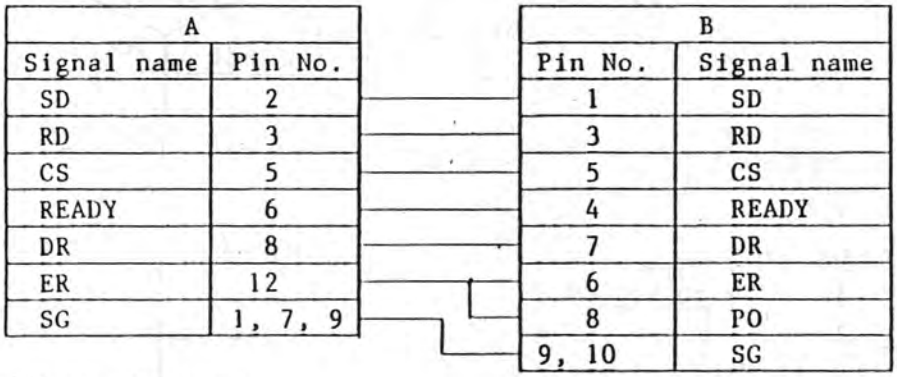
A	
Signal name	Pin No.
SD	2
RD	3
CS	5
READY	6
DR	8
ER	12
SG	1, 7, 9

B	
Pin No.	Signal name
2	SD
3	RD
5	CS
6	READY
8	DR
12	ER
1, 7, 9	SG

Others are open.

(2) MZ-5500/5600 to/from MZ-3500

(A) (B)



A	
Signal name	Pin No.
SD	2
RD	3
CS	5
READY	6
DR	8
ER	12
SG	1, 7, 9

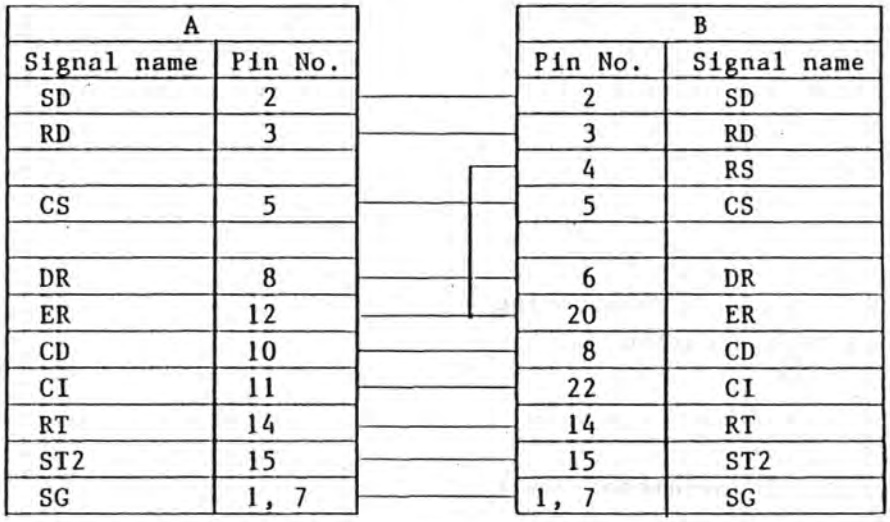
B	
Pin No.	Signal name
1	SD
3	RD
5	CS
4	READY
7	DR
6	ER
8	PO
9, 10	SG

Others are open.

Dip switch	
5	ON
6	ON
7	OFF

(3) MZ-5500/5600 to/from MZ-1X11 (acoustic coupler)

(A) (B)



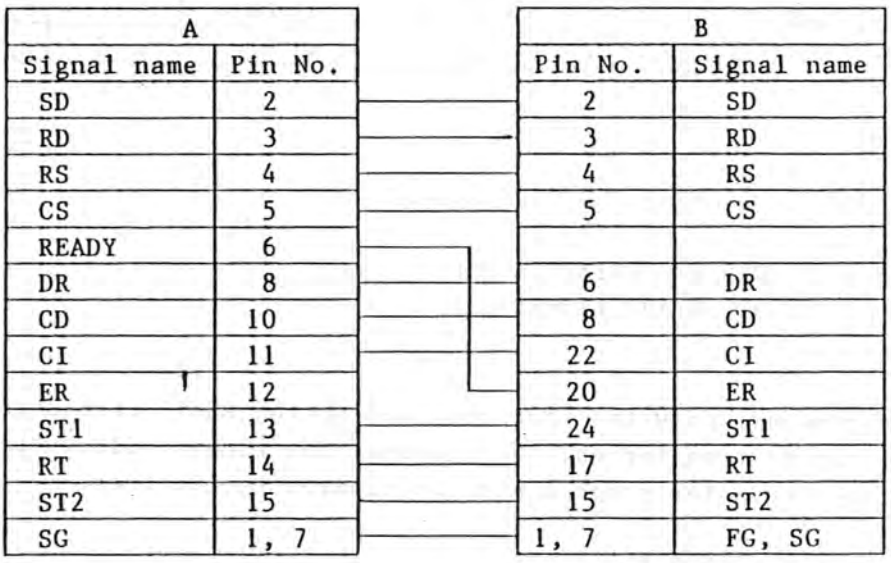
A		B	
Signal name	Pin No.	Pin No.	Signal name
SD	2	2	SD
RD	3	3	RD
		4	RS
CS	5	5	CS
DR	8	6	DR
ER	12	20	ER
CD	10	8	CD
CI	11	22	CI
RT	14	14	RT
ST2	15	15	ST2
SG	1, 7	1, 7	SG

Others are open.

*: Use the MZ-1C36 cable.

(4) MS-5500/5600 to/from the modem (CCITT V24 compliance)

(A) (B)



A		B	
Signal name	Pin No.	Pin No.	Signal name
SD	2	2	SD
RD	3	3	RD
RS	4	4	RS
CS	5	5	CS
READY	6		
DR	8	6	DR
CD	10	8	CD
CI	11	22	CI
ER	12	20	ER
ST1	13	24	ST1
RT	14	17	RT
ST2	15	15	ST2
SG	1, 7	1, 7	FG, SG

*Use the MZ-1C40 cable.

10-5. RS232C sample program

(1) In the case of the example-1

°The file name "ABC.LST" is transferred on CP/M-86.
Set the following using the RSPARM utility for both transmit and receive sides.

```
F1:  1200   Baud rate
F2:  8      Word length
F3:  None   Parity
F4:  2      Stop bits
F5:  No     Send/receive DR monitoring
F6:  No     Send CS monitoring
F7:  No     Echo back
F8:  No     Xon/Xoff
F9:         Exit
F10:        Set RS232C parameter and exit
```

Also, set the following using the ASSIGN utility.

	Input device			Output device			
	Key	Port A	Port B	Screen	Port A	Port B	Printer
F1: Console IN	ON			---	---	---	---
F2: Console OUT	---	---	---	ON			
F3: Auxiliary IN		ON		---	---	---	---
F4: Auxiliary OUT	---	---	---		ON		
F5: List Out	---	---	---				ON

F9: Exit
F10: Assign and exit

Now, transfer the file using the PIP command.

•Transmit side: A>PIP AXO:=A:ABC.LST ↵
•Receive side: A>PIP A:ABC.LST=AXI: ↵

NOTE:
With this PIP command, only the file composed of the ASCII code such as the list file can be transferred. To transfer the binary file such as the command file, the transfer program must be created by the user.

°Data are transferred on BASIC-3.

•Transmit side

```
10  CHANNEL 0, 9600, "8N2"
20  X$="ABCDE"
30  SEND X$;"@";
40  END
```

•Receive side

```
10  CHANNEL 0, 9600, "8N2"
20  RCV X$, 0, "@"
30  X$=LEFT$(X$, LEN X$-1)
40  DISP X$
50  END
```

(2) In the case of the example-2

Although it is identical to the CO/M-86 and BASIC programming example for the example-1, reference must be made to the MZ-3500 manual as it differs in the RS232C parameter setup.

11. KEYBOARD AND KEYBOARD INTERFACE

11-1 Keyboard specifications

- Intelligent keyboard containing the 80C49 processor.
- 63 byte input buffer.
- Two key roll-over.
- Mode indicators for CAPS, and GRAPH.
- Two types of repeat functions can be specified by CPU commands.

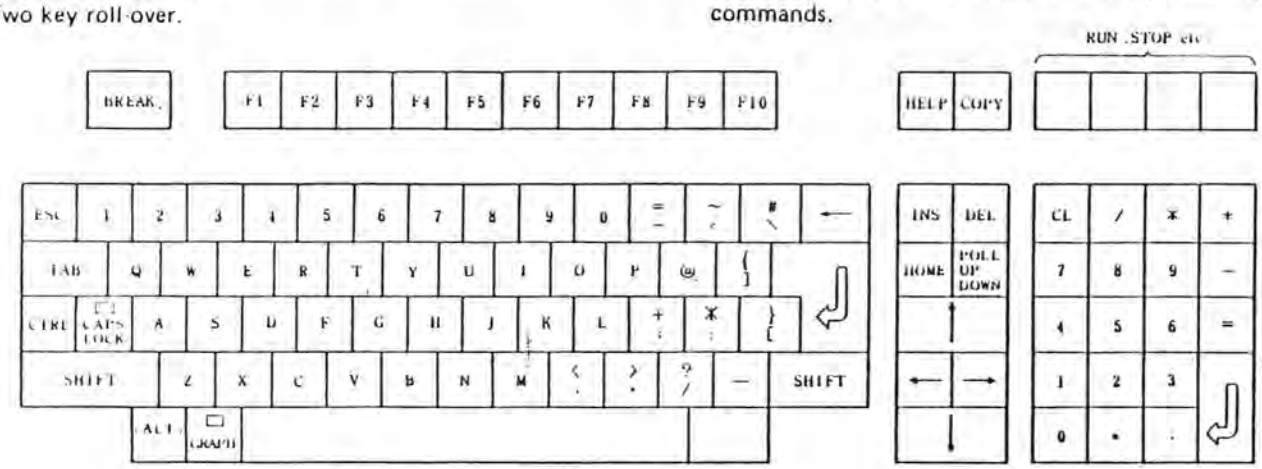


Fig. 11-1 (In the case of English type)

Special Keys

SHIFT: Used for uppercase shift or to provide the upper case shift functions (F11–F20) for the function keys (F1–F10).

CAPS LOCK: Used to fix shift character selection. If it is used with the Shift key, the shift and normal mode will be reversed.

GRAPH: Selects Graphic mode.

CTRL: Used to generate compressed commands.

ALT: Used to generate extended commands.

Keyboard mode

1) NORMAL mode: All keys on the keyboard are operative (to generate one byte data).

2) GRAPH mode: Selected with the GRAPH key to place the keyboard in the graphic mode (1 byte data).

Notes:
- To clear the selected mode, operate the same mode select key or keys a second time.
- If the CTRL and ALT keys are depressed, the keyboard is placed in the normal mode (CAPS and SHIFT keys operative), with the exception that every piece of data consists of two bytes, with the first byte assigned to a CTRL ALG code, and the second byte assigned to the entry code.

Description of special keys

(A) SHIFT key
- Used to place the keyboard in the shift mode (used with other keys).
- Operation of the SHIFT key alone is invalid (no code is transferred to the CPU).

(B) CAPS key
- Used for shift character selection.
- Operative only in the normal mode.
- If used with the SHIFT key, shift and normal selection will be reversed.
- If the CAPS key alone is used, no operation will result (no code is transferred to the CPU).

(C) GRAPH key
- Used to place the keyboard in the Graphic mode. When operated, the pertinent code is transferred to the CPU (operation of the GRAPH key alone is valid).
- All other keys produce the codes the same as those in the normal mode.

(D) CTRL key
- When this key is operated, entry data consists of two bytes: a normal-mode key code followed by a CTRL code. Operation of the mode keys (GRAPH) are ignored. After the CTRL key is operated, the CAPS and SHIFT keys remain valid.
- Operation of the CTRL key alone is not valid (no code is assigned).

(E) ALT key
- After the ALT key is operated, entry data consists of two bytes (same as for CTRL).
- Used to generate extended command codes.
- Effective when used with other keys.
- The pertinent code is transferred to the CPU when operated.

11-2 Keyboard interface

(1) Block diagram

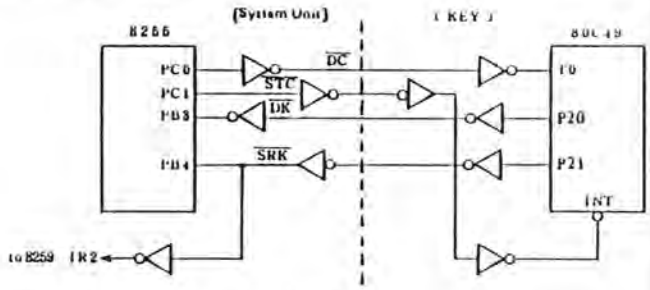


Fig. 11-2

Table 11-1

Direction / Signal name	CPU to keyboard	Keyboard to CPU
$\overline{DC}$	Send data	'READY' signal
$\overline{STC}$	Strobe	Request to Send (strobe for key data)
$\overline{DK}$	READY and ACK signals	Send data
$\overline{SRK}$	None	Request to Receive (CPU)

(2) Key data transfer procedure

1) From keyboard to CPU

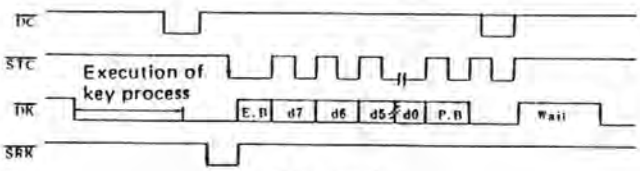


Fig. 11-3

To disable both the keyboard and the CPU interrupt, set both $\overline{DC}$ and $\overline{DK}$ to zero.

Keyboard: When key search, code translation, and other necessary entry data processing is completed, the keyboard starts transferring entry data to the CPU. First, it waits until $\overline{DC}$ is set to one. The waiting time is normally 3ms; for direct keys, it is 1ms. If a time-out occurred, the keyboard exits the data send sequence. When $\overline{DC}$ is set to one, the keyboard sets $\overline{SRK}$ to zero to interrupt the CPU.

CPU: After acknowledging the interrupt, the CPU verifies that $\overline{DK}$ is zero. If $\overline{DK}$ is one, the CPU identifies the transferred data as noise, and exits the interrupt service routine. It then sets $\overline{STC}$ to zero.

Keyboard: When $\overline{STC}$ is set to one, the keyboard waits until $\overline{STC}$ is set to zero. The maximum waiting time is 500ms. If a time-out occurred, keyboard control returns to the initialization routine. When verifying $\overline{STC}$=0, the keyboard send data EB and $\overline{SRK}$ to one.

CPU: Receiving the EB, the CPU sets STC to 1 to request the keyboard for the next data send.

Keyboard: Seeing $\overline{STC}$ is set to one, the keyboard waits for $\overline{STC}$ to be set to zero.

CPU: Sets $\overline{STC}$ to zero to read data from the keyboard, then sets $\overline{STC}$ again to one to request the keyboard for the next data send.

Keyboard: When $\overline{STC}$ is set to one, the keyboard sets P.B. and waits for $\overline{STC}$ to be reset to zero. When $\overline{STC}$ is set again to one, it sets DK to zero.

CPU: Sets $\overline{STC}$ to zero to read P.B. then sets $\overline{STC}$ to one to set the result of the parity check into $\overline{DC}$. If a parity error occurred, $\overline{DC}$ is zero; if no parity error occurred, $\overline{DC}$ is 1. The CPU sets $\overline{STC}$ to one to complete the transfer sequence.

Keyboard: When $\overline{STC}$ is set to zero, the keyboard reads the result of the parity check. When $\overline{STC}$ is set to one, it sets $\overline{DK}$ to one to enable an interrupt from the CPU, and completes the data transfer sequence. If a parity error was detected, the keyboard terminates the data transfer sequence, then tries the same data send again.

* Repeat nine times.

2) Form CPU to keyboard

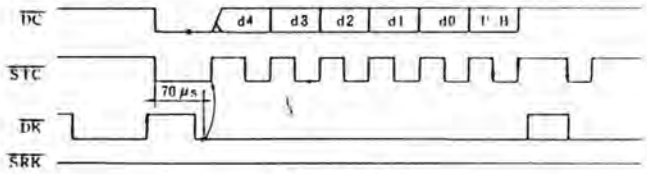


Fig. 11-4

CPU: Waits for up to 100ms for $\overline{DK}$ to be set to one. If $\overline{DK}$ is still zero 100ms later, the CPU identifies it as a keyboard error and exits the sequence. After verifying that $\overline{DK}$ is one, the CPU sets $\overline{DC}$ and $\overline{STC}$ to zero, to interrupt the keyboard.

Keyboard: When the keyboard is interrupted by the CPU, it enters the data receive sequence and verifies $\overline{DC}$=0. If $\overline{DC}$ is one, the keyboard identifies $\overline{STC}$=0 as noise, and exits the interrupt sequence. If $\overline{DC}$ is zero, it sets $\overline{DK}$ to zero.

CPU: Verifies that $\overline{DK}$ is zero 70μs after interrupting the keyboard. The CPU then sets STC to one to set d4, then resets $\overline{STC}$ to zero again.

Keyboard: Seeing $\overline{STC}$ is set to one, the keyboard reads data when $\overline{STC}$ is reset to zero.

CPU: Sets $\overline{STC}$ to one to set data, then resets $\overline{STC}$ to zero.

Keyboard: Reads P.B. to check parity, then sets the result of this parity check when $\overline{STC}$ is set to 1. If no parity error occurred, it sets $\overline{DK}$ to one; if a parity error occurred, $\overline{DK}$ is zero. The keyboard sets $\overline{DK}$ to zero when $\overline{STC}$ is reset to zero.

CPU: Sets $\overline{STC}$ to one to read the result of the parity check. It then temporarily sets $\overline{STC}$ to zero and then sets it again to one, to terminate operations.

* Repeat five times.

(3) Keyboard check method

(A) If the keyboard is locked up:

Checking the keyboard processor

Connect the keyboard to the System Unit, then turn on the system without operating any keys. If only the CAPS indicator comes on, ROM check for the keyboard processor (80C49) is normal. If all the indicators come on, it indicates a ROM check error occurred. Probably the keyboard processor (80C49) is malfunctioning.

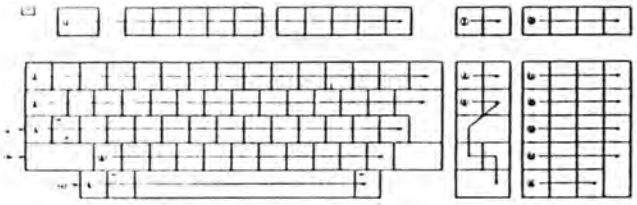


Fig. 11-5

(B) Some keys are inoperative:

Checking key contacts

Connect the keyboard to the System Unit, and turn on the system with the CTRL and ALG (a, c) keys depressed and held. After making sure all the indicators come on, press the keys in the order shown by the arrows in the above figure. If no defective key contact exists, all the indicators will go off. If any defective contact exists, all the indicators will remain on. If a wrong key is pressed and the indicators come on, they will go off when the correct key is subsequently pressed.

If no contact trouble exists when all the keys have been operated, the CAPS indicator will come on, indicating that the key check was normal.

11-3 Key search timing

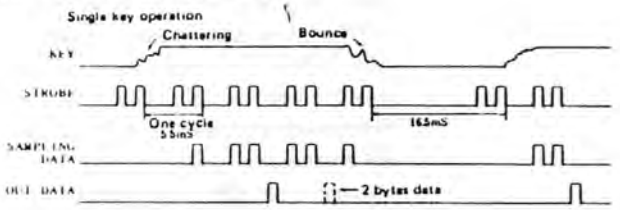


Fig. 11-6

To prevent chattering and bounce, the same key data is checked twice during each search, and only matching key data is regarded as correct. While the search cycle is 5.5ms, it is extended to 16.5ms if a bounce occurs.

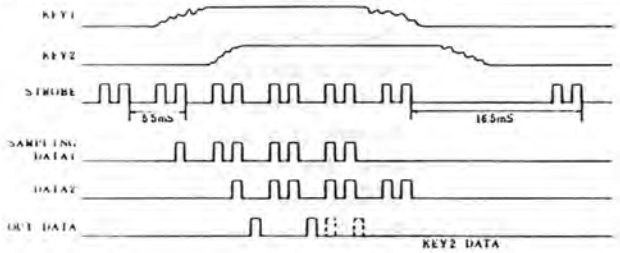


Fig. 11-7

Key search sequence for two-key operation is the same as that for single key operation. When two keys are simultaneously pressed, key data for the first and second keys are successively transferred.

11-4 Eight-bit keyboard processor μPD80C49

Highlights

1) Single-chip, 8-bit microprocessor.
2) Built-in 2K x 8 bit ROM.
3) On-chip 128K x 8 bit RAM.
4) Interruption service capability.
5) I/O port: 8 bits x 2
   Data bus (serving also as I/O port): 8 bits x 1
6) Built-in clock generator.
7) Single +2.5 to +6V power supply.

Pin configuration

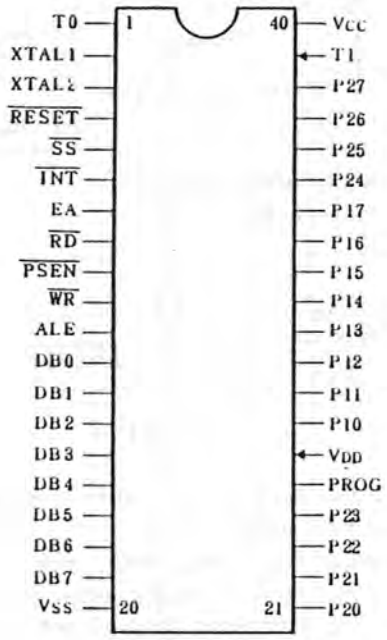


Fig. 11-8

Pin functions

P10-P17:	I/O port (port 1)
P20-P27:	I/O port (port 2)
DB0-DB7:	Data bus
T0, T1:	Test
$\overline{INT}$:	Interrupt
$\overline{RD}$:	Read
$\overline{WR}$:	Write
ALE.	Address latch enable
$\overline{PSEN}$:	Program store enable
$\overline{RESET}$:	Reset
$\overline{SS}$:	Single step
EA:	External access
XTAL1, 2:	Quartz inputs
VDD:	Standby control

Keyboard processor (80C49) signal functions

Table 11-2

Pin No.	Signal name	IN/OUT	Description
1	T0	IN	Data or $\overline{\text{READY}}$ signal input from the System Unit
2	XTAL1	IN	Accepts a quartz signal (6MHz) for the internal clock oscillator.
3	XTAL2	IN	Accepts a quartz signal (6MHz) for the internal clock oscillator.
4	RESET	IN	Initialization input of 80C49
5	SS	IN	+5V
6	$\overline{\text{INT}}$	IN	CPU interrupt strobe input ($\overline{\text{STC}}$)
7	EA	IN	GND
8	$\overline{\text{RD}}$	–	N.C
9	$\overline{\text{PSEN}}$	–	N.C
10	$\overline{\text{WR}}$	–	N.C
11	ALE	–	N.C
12 19	DB0 DB7	IN	Returns signals from the keyboard.
20	Vss	IN	GND
21	P20	OUT	Send data to the System Unit ($\overline{\text{DK}}$)
22	P21	OUT	Data enable/start signal ($\overline{\text{SRK}}$) to CPU
23	P22	OUT	Enables data send to the mouse (CTS)
24	P23	–	N.C
25	PROG	–	N.C
26	VDD	IN	+5V
27 30	P10 P13	OUT	Strobe to the keyboard.
31	P14	OUT	CAPS indicator drive signal
32	P15	OUT	GRAPH indicator drive signal
33	P16	OUT	N.C
34	P17	–	N.C
35	P24	–	N.C
36	P25	–	N.C
37	P26	–	N.C
38	P27	–	N.C
39	T1	IN	Mouse data input (TXD)
40	Vcc	IN	+5V power supply

12. Mouse (MZ-1X10)

The mouse is a new input device, a kind of pointing device, with which cursor movement is controlled by the manipulation of the mouse on the surface of such as the table. On the MZ-5500/5600 series, the mouse can be supported. Use it by connecting to the keyboard.

12-1. Operating principle

°As the mouse is moved on the flat surface of the desk, the ball at the center of the mouse rotates.

°The encoder elements are in contact with the ball at right angle (X and Y axes) and they move according to the rotation of the ball.

°Including both positive and negative coordinates, the encoder outputs are counted in the counter (U1).

°The value counted in U1 is read by the U2 (4-bit microcomputer) in the given cycle to be accumulated in the U2 internal counter. The U1 is reset as soon as the value has been read and performs relative counting at all times.

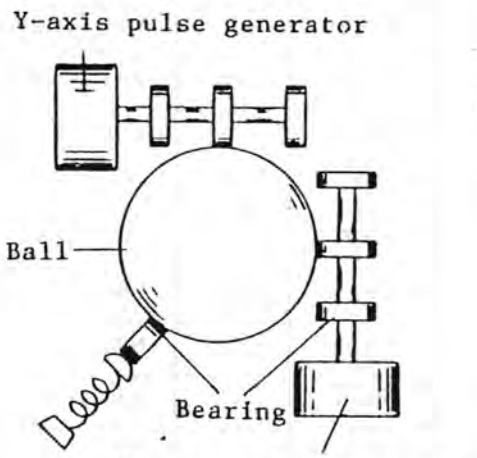


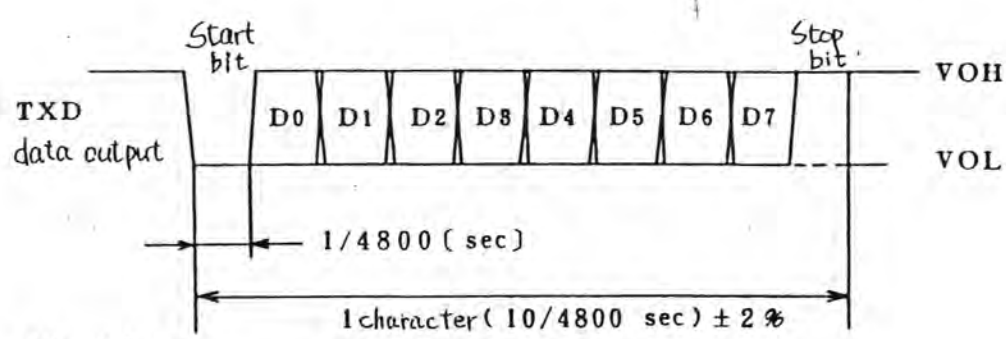
Fig.12-1 X-Y encoder of the mouse

°As the U2 reads the data request signal CTRL in the given cycle from the keyboard of the MZ-5500/5600, receiving of CTRL causes the U2 to send out the data on the TXD line in the given format.

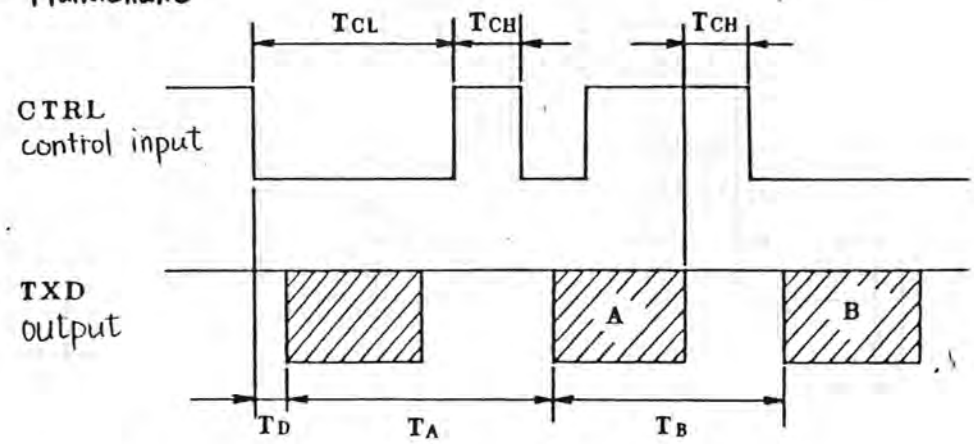
°The mouse is handshaked with the keyboard controller in the timing described in the next paragraph.

NOTES: The following are provided for the IOCS module to control the mouse.

1) MSMOVE
   Reads the coordinates of the cursor position which occurred by the mouse movement.
2) MSDIRECT
   Real time mouse data input.



- Handshake



Data request : CTRL becomes data request when the data output is terminated. In this condition, one data block is issued whereas no data block is issued when CTRL .

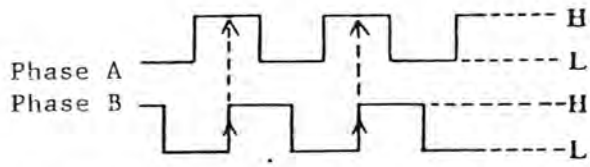
SW data : SW condition immediately before the data output (start bit) is issued.

X,Y data : X and Y coordinates within TA and TB are issued as data A and data B. (Relative coordinates are always issued.)

TCL	min	500μS	Control L pulse width
TCH	min	500μS	Control H pulse width
TD	max	750μS	Output data reply time

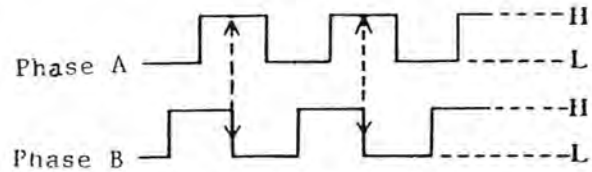
Encoder input wave form (X-ENC, Y-ENC)

Positive rotation



Direction in which phase B becomes positive when phase A is H.

Negative rotation



Direction in which phase B becomes negative when phase A is H.

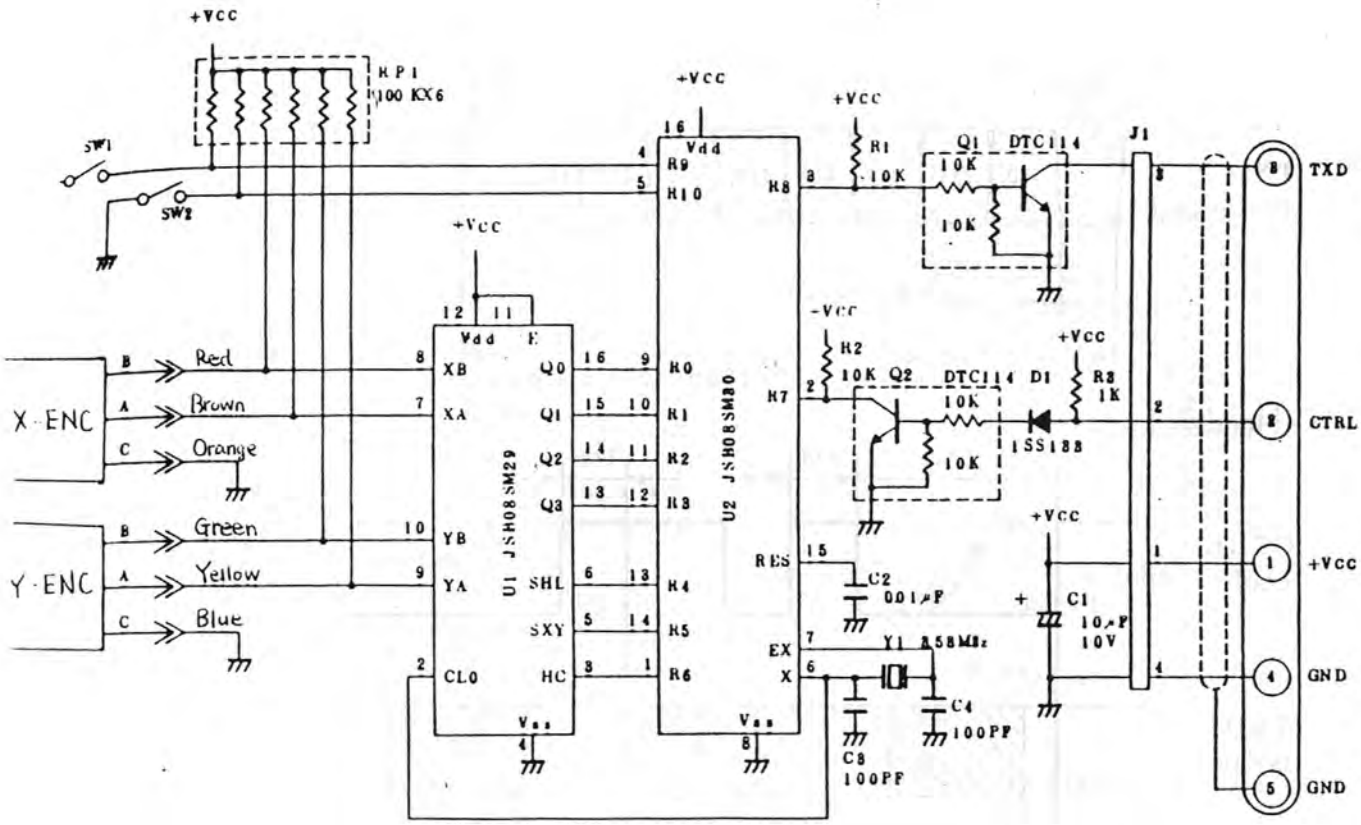


Fig.12-2 Mouse circuit

13. RTC (Real Time Clock)

13-1. Operational description

As the real time clock is implemented in the MZ-5500/5600, it has the circuit which is shown in Fig.2-13-1. The RP5C01 RTC is backed up by the battery power to retain the clock and the data in the internal RAM during power off. A part of the RAM can be accessed by the user.

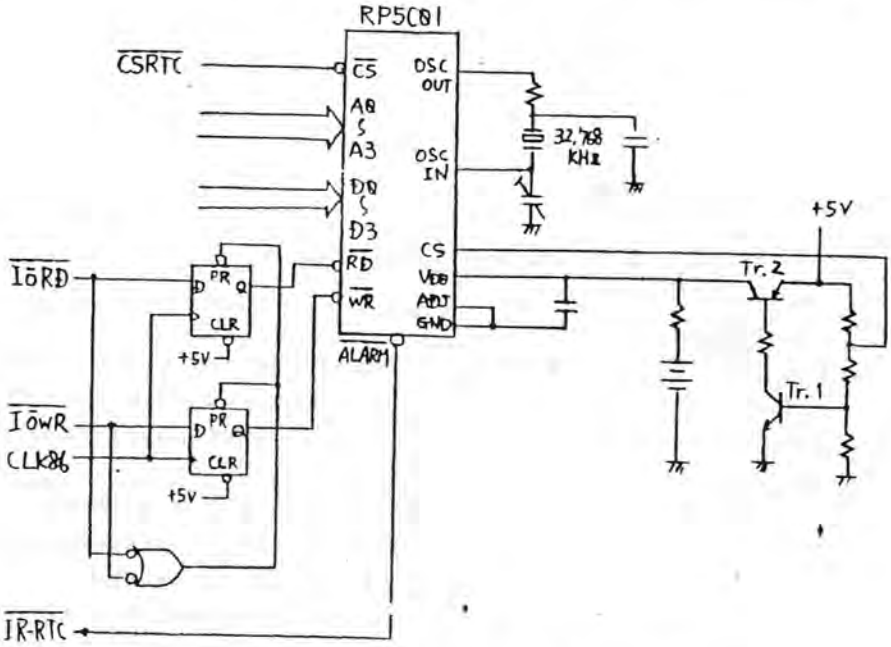


Fig.13-1 Real time clock circuit

°The RP5C01 in the figure is the LSI designed for the real time clock and it has the features shown in the table.
Although the RP5C01 is accessed with the I/O address 220H to 22FH, the setup time of IORD and IOWR is delayed via the LS74 D-flipflop to create RD and WR signals, because the read/write setup timing is rather slow.

Table 13-1 Features of the RP5C01

°4-bit bidirectional bus: D0 - D3
°4-bit address input: A0 - A3
°Internal timer to keep time (hours, minutes, seconds), calendar (100 years, leap year, month, day, day of the week)
°Choice of the 24 hours and 12 hours (am, pm) modes
°All timer data expressed by the BCD notation
°±30 seconds adjusting function
°Possible battery backup
°Internal 26 x 4-bit RAM
°Possible output of the alarm signal or 16Hz/1Hz timing pulse

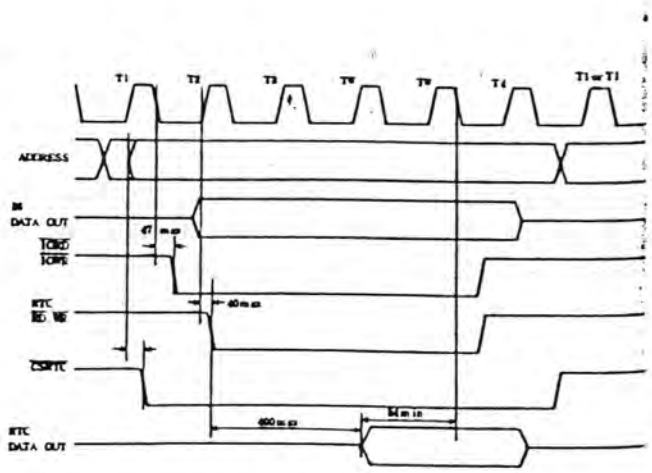


Fig.13-1 RP5C01 access timing

Table 13-2 RP5C01 pin names and functions

Pin name	Pin No.	Function
$\overline{CS}$, CS	1,2	For interfacing with the external device which becomes valid when CS=H, $\overline{CS}$=L. CS is connected with the power down detect circuit of the device power supply and $\overline{CS}$ is connected with the microcomputer.
ADJ	3	It has the function to adjust the seconds without intervention of the CPU. With ADJ=H the seconds are reset to zero when it is within 0 to 29 seconds. If it is within 30 to 59 seconds, the seconds are then incremented.
A0 - A3	4,5,6,7	Address pin to be connected with the address bus of the CPU.
$\overline{RD}$	8	I/O control input. Low for input from the RP5C01 to the CPU.
GND	9	0V
$\overline{WR}$	10	I/O control input. Low for input from the CPU to the RP5C01.
D0 - D3	11,12, 13,14	Bidirectional data bus. Connected with the CPU data bus.
$\overline{ALARM}$	15	Alarm, 16HzCK, 1HzCK pulse output. Open drain output.
OSCIN, OSCOUT	16,17	32.768KHz crystal oscillator connection pins.
VCC	18	+5V supply

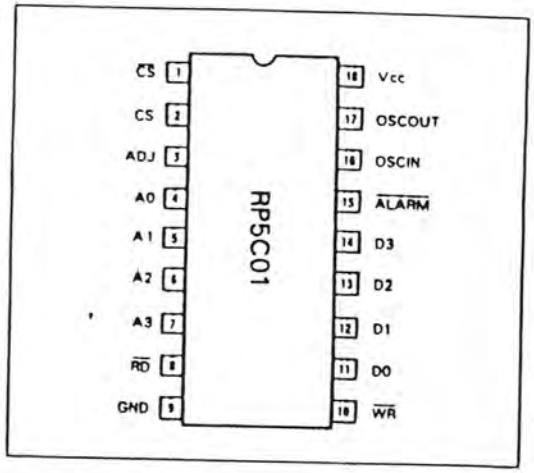


Fig.13-2 RP5C01 pin configuration

°The RP5C01 generates clock pulse internally by connecting the 32.768KHz ceramic oscillator and the CR network between OSCIN and OSCOUT, and divides it for the counter operation.

°The CS pin detects a power down, and then sets the circuit to the power down condition. When power is on to the personal computer, Tr1 and Tr2 in Fig.2-13-1 are active so that +5V is supplied to the RP5C01 and the backup battery is being recharged. When power is off, it makes Tr1 gone inactive first, then Tr2. This isolates the circuit on the right of Tr2. Then the backup battery supplies power to the RP5C01, which keeps the time along with the internal RAM.

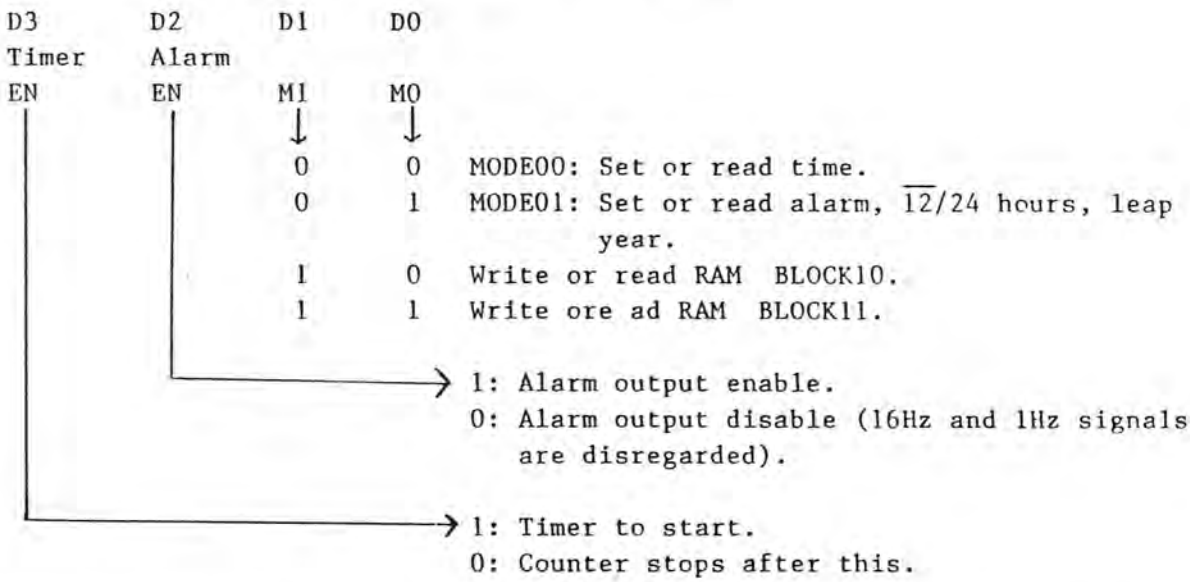
Table 13-3 RP5C01 internal address assignment

Mode	Mode 00					Mode 01					10	11
A0 - A3	Contents	D3	D2	D1	D0	Contents	D3	D2	D1	D0	Contents	Contents
0	1-second counter						x	x	x	x		
1	10-second counter	x					x	x	x	x		
2	1-minute counter					Alarm 1-minute register					Block 10	Block 10
3	10-minute counter	x				Alarm 10-minute register	x					
4	1-hour counter					Alarm 1-hour register						
5	10-hour counter	x	x			Alarm 10-hours register	x	x			4 bits	4 bits
6	Day of week counter	x				Alarm day of week register	x				x	x
7	1-day counter					Alarm 1-day register					13	13
8	10-day counter	x	x			Alarm 10-day register	x	x				
9	1-month counter						x	x	x	x	RAM	RAM
A	10-month counter	x	x	x		12-hour/24-hour selector	x	x	x			
B	1-year counter					Leap year counter	x	x				
C	10-year counter						x	x	x	x		
D	Mode register	Timer EN	Alarm EN	Mode register M1	M0		Timer EN	Alarm EN	Mode register M1	M0	←Same	←Same
E	Test register	Test 3	Test 2	Test 1	Test 0		Test 3	Test 2	Test 1	Test 0	←Same	←Same
F	Reset controller, etc.	1Hz ON	16Hz ON	Timer reset	Alarm reset		1Hz ON	16Hz ON	Timer reset	Alarm reset		

X is "don't care" when write and always "0" when read.

*Mode, 00, 01, 10, 11, has function to select the internal register and RAM banks which can be achieved by writing the select data in the mode register. Since mode registers are assigned to the same address, it can be revised under any mode.

MODE register (A3, A2, A1, A0) = (1,1,0,1) = D



*Leap year counter:
Leap year when D1=D0=0. Counted up at the same time the year is counted.
*$\overline{12}$/24 hours selector:
The 24 hours system is adopted when D0=1. The 12 hours system is adopted when D0=0. With D1=1, PM is selected. With D1=0, AM is selected.
*Reset controller:
16Hz/1HzCK register
(A3, A2, A1, A0)=(1,1,1,1)=F
All alarm registers are reset with D0=1.
Minutes above seconds are reset with D1=1.
16HzCK pulse is ON with D2=0.
1HzCK pulse is ON with D3=0.
*Address 0 - D
Read and write are possible.
*Address E - F
Only write is possible.
*The following are provided for the real time clock related IOCS module. and can be used when called as a subroutine by the machine language. For detail, refer to Section 3, Software.

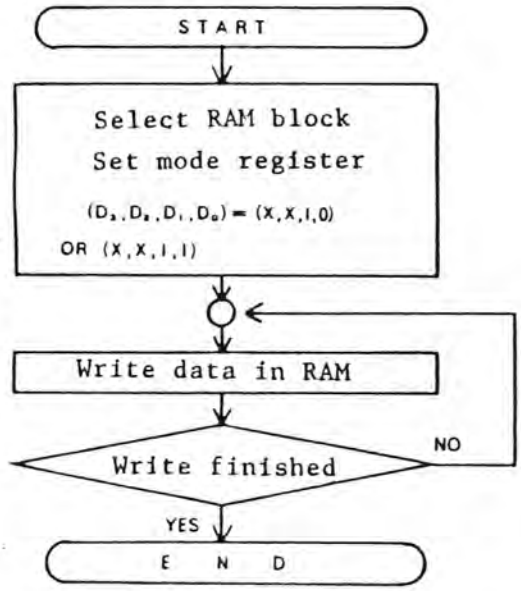
IOCS name	Function
TIMRD	Reads the real time clock.
TIMSET	Sets the real time clock.
ONTIM	Enables the alarm interrupt.
OFFTIM	Disables the alarm interrupt.

13-2. Accessing the RTC internal RAM

Total 26 nibbles internal RAM are provided in the RP5C01 RTC for the Mode 10 and 11 as shown in Table 2-13-3, they are the battery backed up RAM, though not so large in capacity. But, all RAMs for Mode 10 are reserved by the system and those Mode 11 are user accessible.

See the flowchart below for the accessing method.

(1) Write

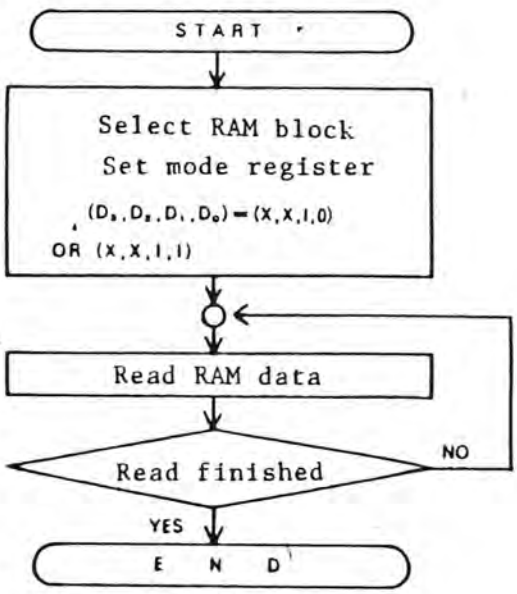


[Ex.]

To write the 4-bit data 5H in the address 0A of Mode 11.

```
        CALL   SSUB
        MOV    DX,22AH
        MOV    AL,05H
        OUT    DX,AL
        CALL   ESUB
         :
SSUB:   MOV    DX,22DH
        IN     AL,DX
        OR     AL,03H
        OUT    DX,AL
        RET
ESUB:   MOV    DX,22DH
        IN     AL,DX
        AND    AL,0CH
        OUT    DX,AL
        RET
```

(2) Read



To read the 4-bit data in the address 0A of Mode 11 and to store it in DL.

```
        CALL   SSUB
        MOV    DX,22AH
        IN     AL,DX
        AND    AL,0FH
        MOV    DL,AL
        CALL   ESUB
```

*Nibble = 4 bits

14. PSG (Programmable Sound Generator)

One channel of the PSG is provided for the MZ-5500/5600 series to generate eight octave, triple chords, and it has the following configuration.

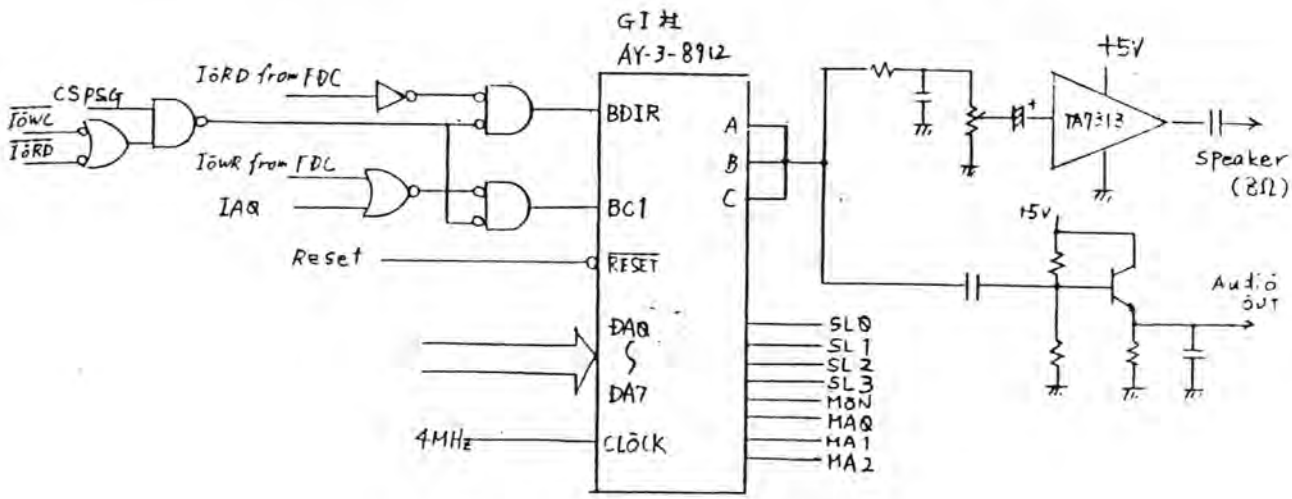


Fig.14-1 PSG circuit

Operational theory

°The figure above shows the AY-3-8912 PSG which can be accessed by the I/O address of 230H - 23FH.
As there are 16 registers in the PSG, control is done by writing the control command in the above I/O address. Those registers are permitted to read so as to enable to know the current state and data in the memory. Once 16 registers have been programmed, control is done via those registers to generate sound and manage it and the CPU is therefore open for other jobs.

°Not only the PSG incorporates the sound generating function, but, it also has the 8-bit parallel I/O port on which the mini-floppy disk interface drive select signal (SL0-SL3), motor-on signal, and address bank select signal (A0000H-BFFFFH) are sent.

°Three sound signal outputs (A, B, C) from the PSG are ORed in the analog mode to drive the speaker via the TA7313 Audio Amplifier and sent through the AUDIO OUT jack via the emitter follower transistor.

°The pin configuration and functions are shown in the next page.

°PSG related IOCS
The following three modules are provided for the IOCS which controls the PSG. For detail, refer to Section Three, Software. For detail of the PSG, refer to the PSG Descriptions published by GI.

MUSIC:
Drives the PSG with the contents of the music note.
EMUSIC:
Data are directly set in the channel A of the PSG to generate sound.
ZMUSIC:
Similar as MUSIC.

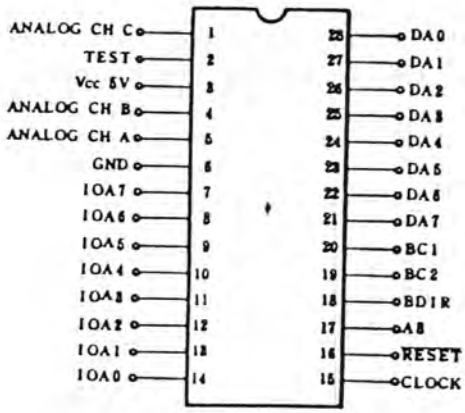


Fig.14-2 AY-3-8912 pin configuration

Table 14-1 AY-3-8912 signal description

Pin No.	Signal name	In/Out	Function
1	ANALOG CH C	Out	Analog output channel C
2	TEST1		Test pin during chip manufacture which should be unconnected.
3	VCC		+5V supply
4	ANALOG CH B	Out	Analog output channel B
5	ANALOG CH A	Out	Analog output channel A
6	GND		0V
7 - 14	IOA7 - 0	In/Out	I/O port
15	CLOCK	In	Tone noise, envelope generator timing reference input (2MHz)
16	$\overline{\text{RESET}}$	In	Input of a low (0) signal to this line at the start, it resets all registers.
17	A8	In	Auxiliary address bit which is provided to permit a memory space expansion in addition to the area specified by DA7-DA0.
18	BDIR	In	Bus direction
19	BC2	In	Bus control 1
20	BC1	In	Bus control 2

These bus control signals control all external and internal bus operation of the PSG. Signals are decoded in the following manner by the PSG.

BDIR	BC2	BC1	PSG function
0	0	0	INACTIVE The PSG/CPU bus becomes inactive and DA7-DA0 high impedance.

<table>
<tr><th>Pin No.</th><th>Signal name</th><th>In/Out</th><th>Function</th></tr>
<tr><td></td><td></td><td></td><td>
<table>
<tr><th>BDIR</th><th>BC2</th><th>BC1</th><th>PSG function</th></tr>
<tr><td>0</td><td>0</td><td>1</td><td>LATCH ADDRESS
Indicates that the bus retains the register address to be latched in the PSG.</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>INACTIVE</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>READ FROM PSG
Data in the register at current address are sent on the PSG/CPU bus.</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>LATCH ADDRESS</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>INACTIVE</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>WRITE TO PSG
Indicates that the bus retains the data in the register latched at the current address.</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>LATCH ADDRESS</td></tr>
</table>
</td></tr>
<tr><td>21 -28</td><td>DA7 - DA0</td><td>In/Out</td><td>In the data mode, corresponds to the register array bits, B7 - B0 in the data mode.
In the address mode, DA3 - DA0 are used to select the register number and DA7 - DA4 to comprise the address input.</td></tr>
</table>

15. Video display circuit

The video display circuit is basically the same for both the MZ-5500 and MZ-5600 which features the following.

15-1. Features of the video display circuit

°Bit map method, complete graphic display
°The μPD7220 Graphic Display Controller (GDC) is used for the video display controller.
°Meets resolution of 640 x 400, 640 x 200, 320 x 400, and 320 x 200 dots.
°Possible to perform multiple window display up to four windows by means of the Window Controller (WDC) of the hardware.
°Possible to access the video RAM from either the CPU or the GDC. As the display cycle is divided into the GDC cycle and the CPU cycle, it permits faster access from the CPU to the video RAM with less waits.
°Incorporation of the external clock input and the external vertical sync input permits superimposition on such as TV broadcasting, VTR, video disk, etc. However, both the software and the hardware do not support it at present.
°It has 96KB of the video RAM as a standard equipment and can be expanded to 192KB when the option is used.
°The hardware character generator is not provided as standard.
°Incorporates the pallet function and color priority function.
°Possible to handle eight colors and eight monochrome tone.

Table 15-1 Mode specification

[Color mode]
(Color CRT)
°Possible to make choice of eight colors for each dot for three planes of 0, 1, and 2.
°Possible to assign eight tones for the background color of each window.
°Possible to make choice of eight border colors. (200-raster CRT only)
°Possible to specify priority for desired four colors and any one color.
°Possible to change any color to any of other seven colors in terms of the hardware by means of the pallet function.

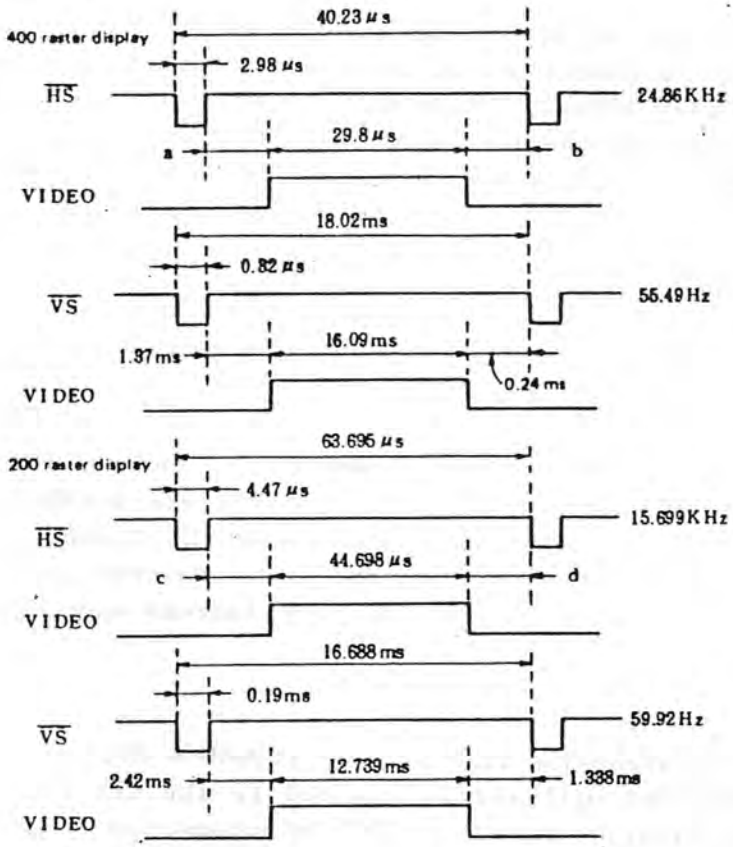
(Monochrome CRT tone)
°Possible to make choice of eight colors for each dot for three planes of 0, 1, and 2.
°Possible to assign eight stages of the background for each window.
°Possible to make choice of eight border tones. (200-raster CRT only)
°Possible to specify priority for desired four tones and any one tone.
°Possible to change any tone to any of other seven tones in terms of the hardware by means of the pallet function.

[Monochrome mode]
°Possible to overlay planes, 0, 1, and 2.
°Possible to reverse any window.

Table 15-2 Maximum screen frames by the hardware

Memory size	640x400 color	640x400 B/W	320x400 color	320x400 B/W	640x200 color	640x200 B/W	320x200 color	320x200 B/W
96KB	1	3	2	6	2	6	4	12
192KB	2	6	4	12	4	12	8	24

MZ-5500/5600 CRT timings



	640x400/640x200	320x400	At the base of GDC
a	4.85μs	5.08μs	3.73μs
b	2.60μs	2.42μs	3.73μs

	640x200	320x200	At the base of GDC
c	9.50μs	9.78μs	7.82μs
d	5.03μs	4.75μs	6.70μs

Clock

	640x400	320x400	640x200	
			MZ1D13 MZ1D14 MZ1D18	Others
DOT CK	21.48	10.74	21.48	14.32
2xCCLK	2.68	2.68	2.68	1.79

	320x200	
	MZ1D13 MZ1D14 MZ1D18	Others
DOT CK	10.74	7.16
2xCCLK	2.68	1.79

Unit: MHz

15-2. Use of video display circuit (software control)

i) Video RAM

To make data displayed on the video screen, each independent dot has to be written in the video RAM. A single bit of the video RAM corresponds to one bit position on the display screen. From what location of the video RAM has to be started to display can be specified in unit of word using the GDC* and window controller setup. Sixteen bits of the bit 0 to the bit 15 of the word will be displayed from left to right in their order. Fig.15-1 shows the memory map of the video RAM. The CPU accesses in unit of one byte (8 bits) and one word (16 bits), and the GDC accesses in unit of one word (16 bits). As many IOCS modules are provided for displaying, refer to Section Three, Software, for more details. It is recommended to use the IOCS* when programming by the machine language.

NOTE-1:

The display address is set by the SCROLL command of the GDC and VMA of the WDC. Only the low order 15 bits of the address (GDC) are decoded by the hardware to read three data for displaying from planes, 0, 1, and 2. Which data should be read is directed by VDS of the WDC. However, giving the address, 30000H - 3FFFFH (GDC) for the display address may cause the display to distort.

NOTE-2:

When the CPU accesses the expansion VRAM area of C8000H - CFFFFH, D8000H - DFFFFH, E8000H - EFFFFH, NMI will not be applied to the CPU even if the expansion VRAM* does not exist. (Normally, NMI is automatically applied if XACK is not returned. However, for the expansion VRAM, XACK is returned from the HI chip (CRT controller LSI) even if the VRAM does not exist.)

NOTE-3:

DMA is not permitted for the VRAM area of C0000H - EFFFFH, so that, it is not possible to make direct loading and saving from the floppy disk to the VRAM. And, do not set the VRAM area 0CH, 0DH, and 0EH in the high order 4 bits of the DMA, as it may cause the VRAM to be affected or result in malfunction.

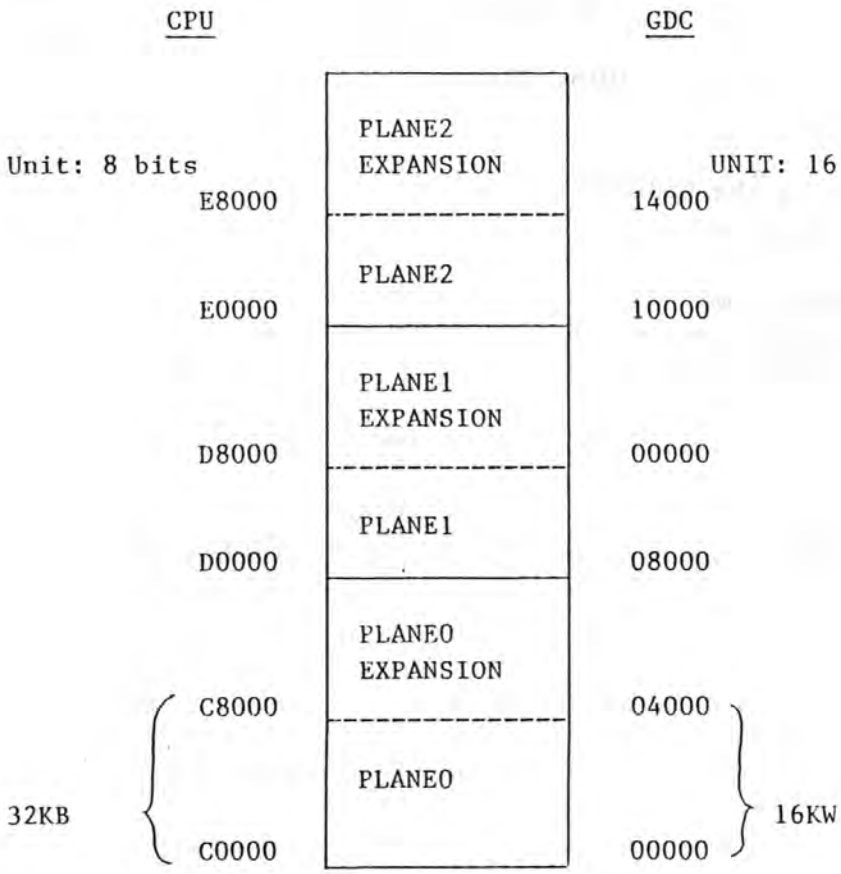
ii) GDC (μPD7220)

Since the GDC is used for the CRT controller, horizontal sync and vertical sync are generated from the GDC. Table 15-3 shows the list of parameters of the SYNC command of the GDC. The value set in the I/O port of the address 130H is also contained in the table. See Table 15-4 for others. Also, see NEC μPD7220 GDC User's Manual for the detail of the GDC. Summary is attached at the end of this text.

*IOCS:
Short words for I/O Control System which indicates the software module used to control the hardware. The user can use it when called as a subroutine by the machine language.

*GDC:
Short words for Graphic Display Controller (μPD7220) which is used for the MZ-5500/5600.

*VRAM:
Video RAM.



EXPANSION: Expansion VRAM

Fig.15-1 VRAM memory map

Table 15-3 GDC setup

Resolution	640x400	320x400	640x200		320x200	
Display	1D14,14,18	1D13,14,18	1D13,14,18	Others	1D13,14,16	Others
H display	40			40	---	40
HFP	5			6	---	6
HS	4			4	---	4
HBP	5			7	---	7
V display	400			200	---	200
VFP	6			21	---	21
VS	8			3	---	3
VBP	34			38	---	38
130 H (H1)	0	4	0	1	---	5
Others	---	NOTE-2	NOTE-1	---	---	NOTE-2

1D13: MZ1D13 1D14: MZ1D14 1D18: MZ1D18

NOTE-1:
Set to L/R=1 (2 lines) by the CSRFORM command.

NOTE-2:
Set to 1M=1 by the SCROLL command.
Set to double value of 640 dots mode by the PITCH command.
Set to DGD=1 by the VECTW command.

For graphics and display, refer to the μPD7220 User's Manual.

CAUTION:
320x200 mode is not applicable for the 1D13, 1D14, and 1D18.

iii) Window controller (LZ90E07, LZ91F07)

°General description of the WDC
The window controller displays a rectangular area from the VRAM in the desired location of the display screen as shown in Fig.15-2.

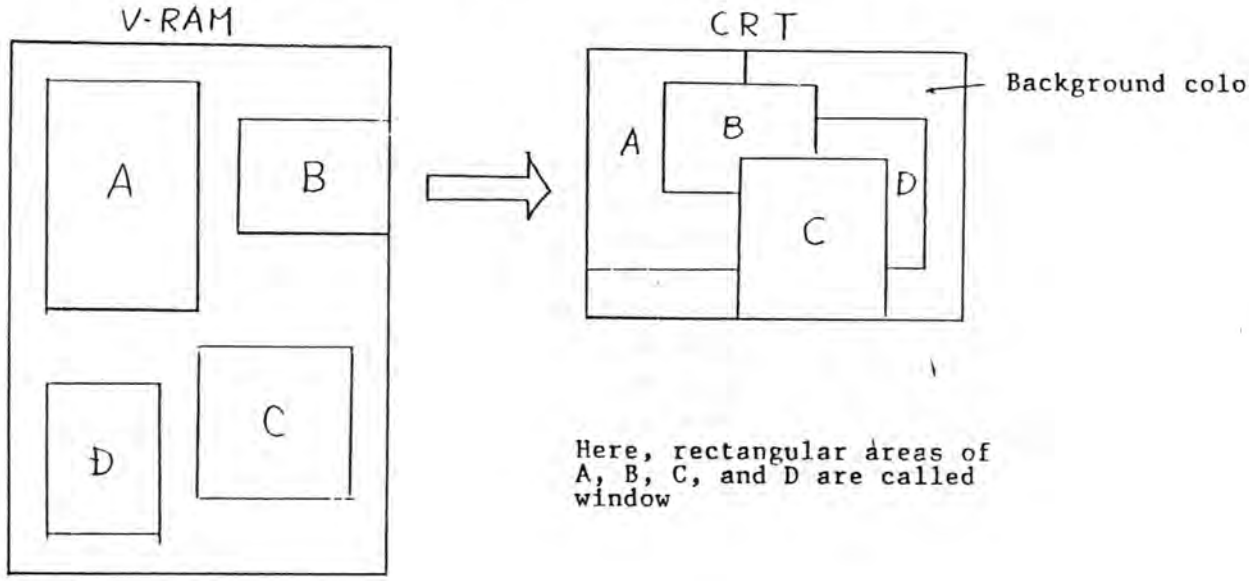


Fig.15-2

°Features

(1) A maximum of four windows can be displayed.
(2) Each window can have its priority specified, and, it allows overlay of windows.
(3) When there are three VRAM planes, it is possible to display by plane or overlaid display of two or three planes.
(4) It is possible to make direct output of the inputted address without the use of the window function.

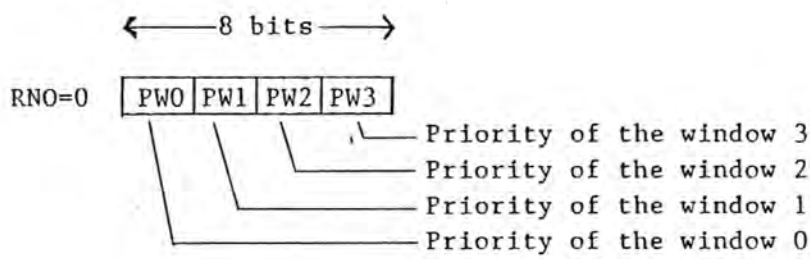
°WDC registers

(1) RNO register (I/O address 110H)
Register number (0 - 12) is set.

| x x x x | RNO |

RNO=0-12

(2) Priority register (I/O address 112H)
Priority is set to window.



°The priority 3 among all has the highest priority. (Be careful as it is an opposite to those of BASIC.)
°All priority must be different each other.
°The window function is not effective when all priorities are set to 0 and the address from the GDC is directly sent out.

°Window register (I/O address 112H)
VMA*1 and VDS*2 are set to window.

RNO	8 bits		
1	VMA0L	Bias address, low	For window 0
2	VMA0H	Bias address, high	
3	x x x x x VDS0	VRAM data select	
4	VMA1L	Bias address, low	For window 1
5	VMA1H	Bias address, high	
6	x x x x x VDS1	VRAM data select	
7	VMA2L	Bias address, low	For window 2
8	VMA2H	Bias address, high	
9	x x x x x VDS2	VRAM data select	
10	VMA3L	Bias address, low	For window 3
11	VMA3H	Bias address, high	
12	x x x x x VDS3	VRAM data select	

Fig.15-3

°Register setup
The priority register and the window register must be set after writing each register number to RNO register. Since the RNO register increments by one automatically each time written, only the first RNO may be written.

*1 VMA: See the paragraph discussing VMA.
*2 VDS: See the paragraph discussing VDS.

[Fx] To set the window register for the windows 1 and 2:

I/O address		
110H	x x x x 0 1 0 0	←RNO is set for VMA1L.
112H	VMA1L	←VMA and VDS are set in succession.
	VMA1H	
	x x x x x VDS1	
	VMA2L	
	VMA2H	
112H	x x x x x VDS2	

Fig.15-4

°Priority

As discussed previously, priority is used to determine the priority order of the window display; the value 0 to 3 must be set in registers. When windows are overlaid, the layout of windows can be set upside down in a flicker of moment by changing the priority.

[Ex]

PW0	PW1	PW2	PW3
0 0	0 1	1 0	1 1

PW0	PW1	PW2	PW3
0 0	1 1	0 1	1 0

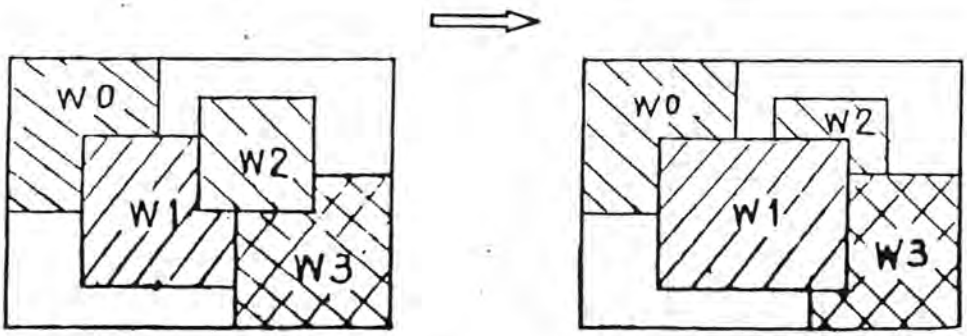
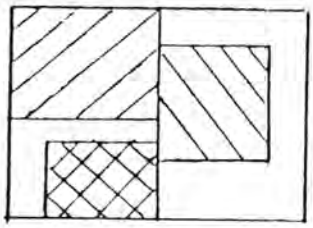


Fig.15-5

Except the following, different priority values must be given.

NOTE-1:
When only one window was set to mapping RAM*1, it does not matter even if the same value other than 0 is set for all.

NOTE-2:
If windows are not overlaid as in the figure right, it does not matter even if the same value other than 0 is set for all.



NOTE-3:
When all priority registers are set to 0, it disables the window function so that the address from the GDC is directly sent out. In this event, there is a need of setting VDS accordingly.

*1 Refer to the section Mapping RAM.

°VMA

VMA is the bias value which makes the window area set to the respective display area.

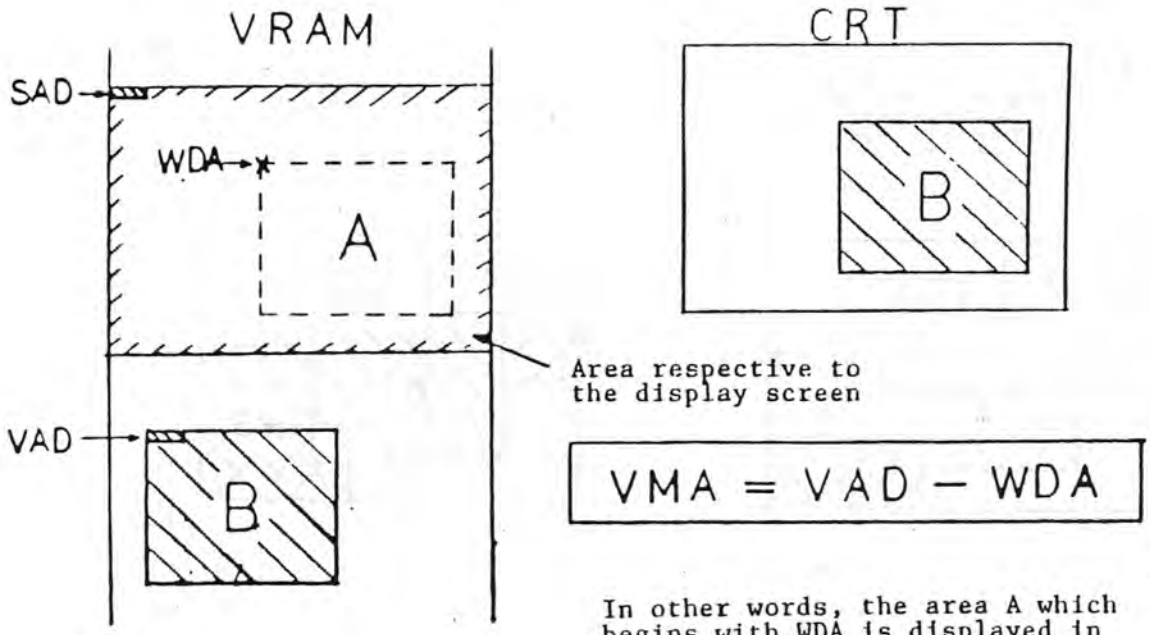
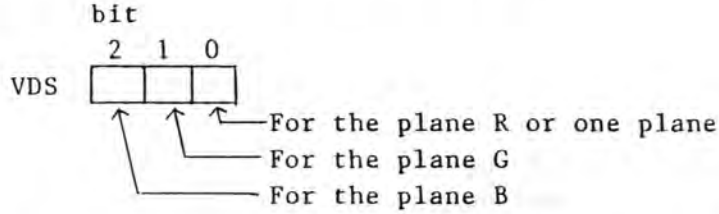


Fig.15-6

°VDS

VDS controls the VRAM plane output.



As shown above, VDS has three bits for each window which are used to perform any plane display or overlaid display of two or three planes.

[Ex]

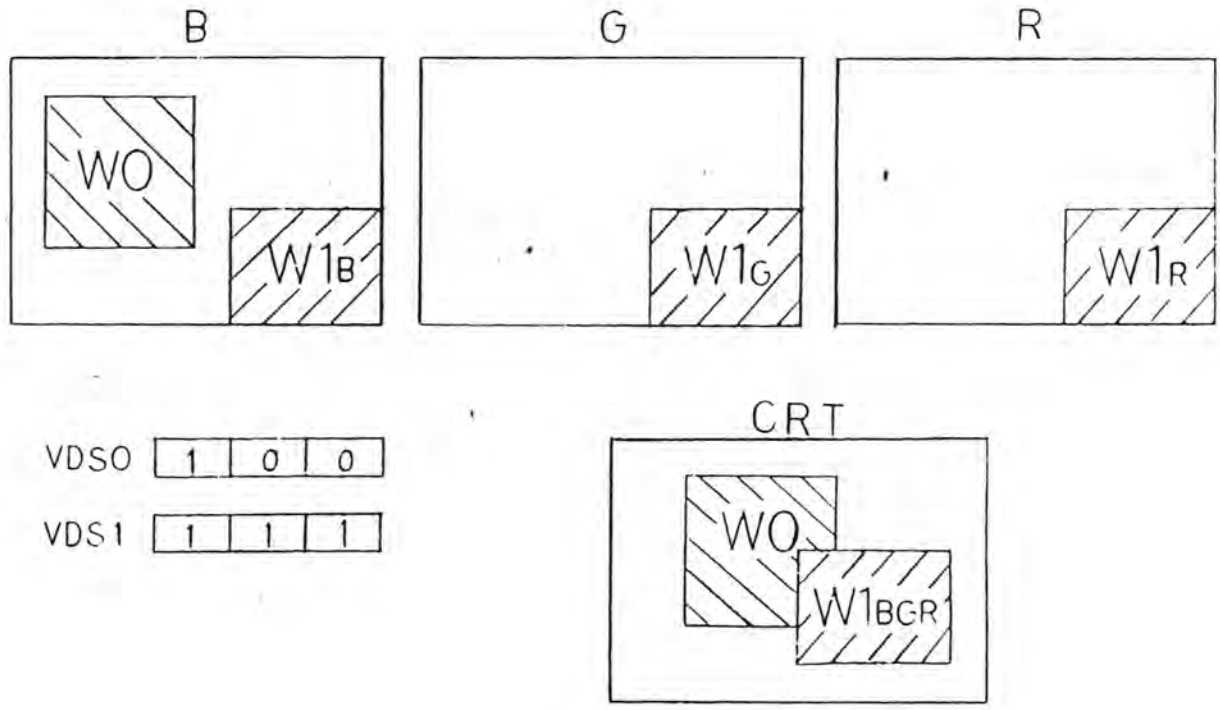
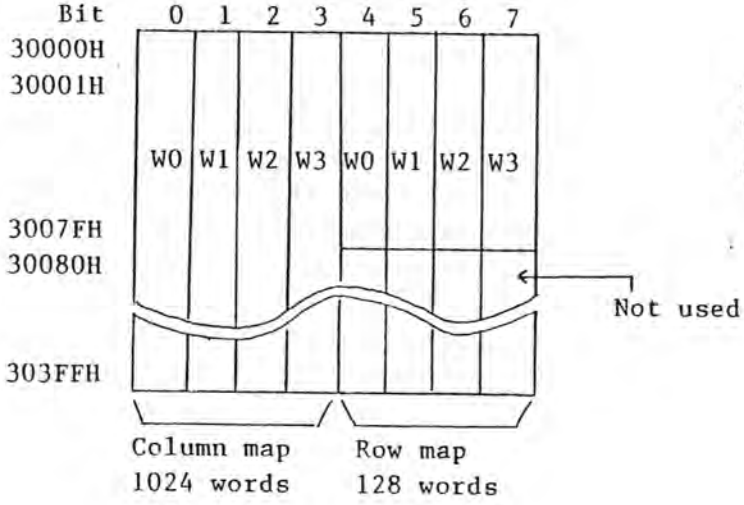


Fig.15-7

When 000 is set to three VDS bits, the background color corresponding to that window is displayed instead of the VRAM data in the window area.

°Mapping RAM

The mapping RAM controls the location and area of window in the display screen area.



NOTE:
The mapping RAM cannot be accessed from the CPU.

Fig.15-8

The mapping RAM exists on the GDC memory map as shown in Fig.15-8.
It has to corresponds to the display screen when the mapping RAM is used (Fig.15-9).

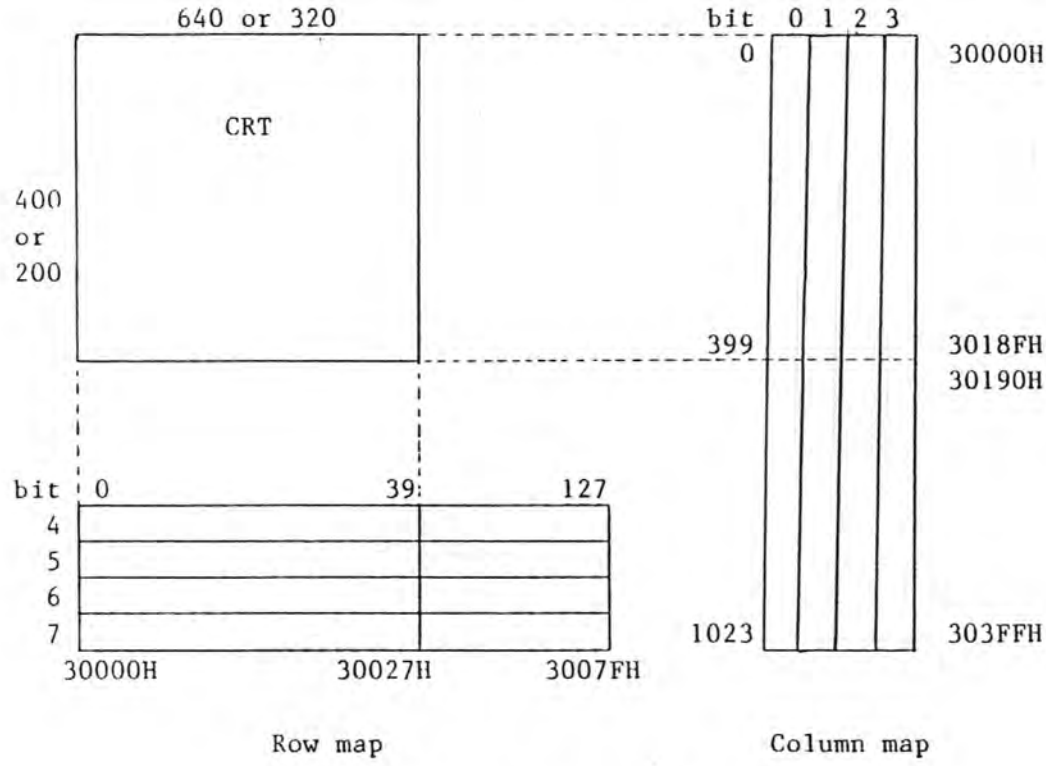


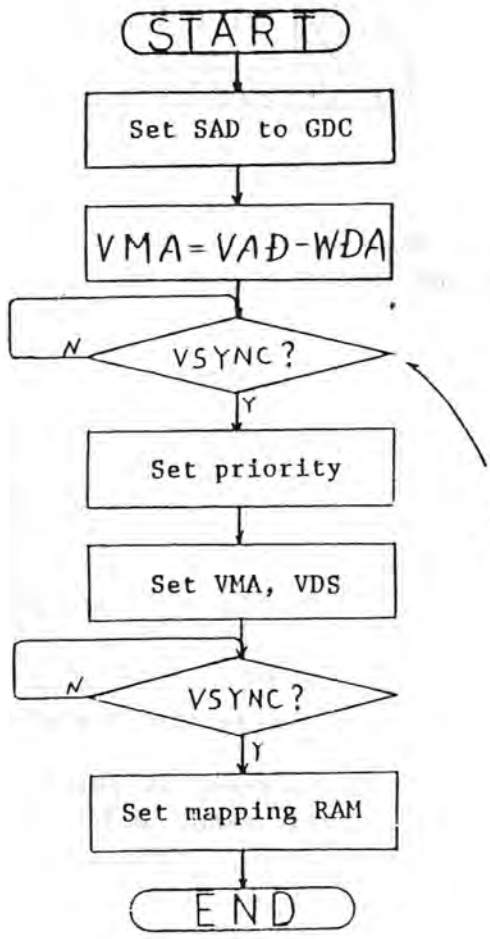
Fig.15-8 Mapping RAM assignment

°For the row map at the time of 320x400 and 320x200 dots mode, only even addresses are effective. The left margin of the display screen is the address 0 and the one that follows is the address 2.

°As one bit of the column map corresponds to ½ dot of the display when displaying under the 200-raster mode for the MZ1D13, MZ1D14, and MZ1D18, the window may be specified in an increment of ½ dot for the horizontal direction.

°WDC programming

Write to the WDC and the mapping RAM is limited only to the vertical flyback time. Whereas, one window must be programmed at a time in a single vertical flyback time to set four windows. Special attention must be paid to the program timing for the mapping RAM.



VMA, VDS, and priority values should be provided before the VSYNC check and they should be set in succession at VSYNC.

As VSYNC is with IRQ of the master (8259A), this interrupt may be used.

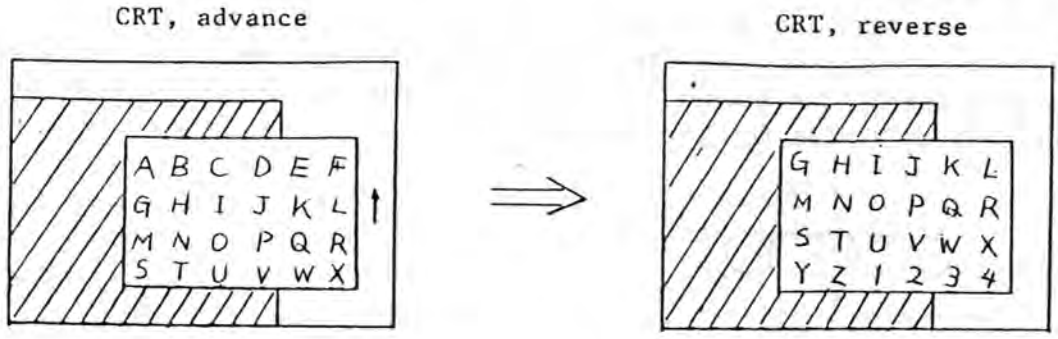
Priority, VMA, and VDS may not be programmed one at a time necessarily; they may be set altogether, if possible. However, the mapping RAM should preferably be programmed for a window one at a time during the vertical flyback time in order to prevent distortion in the display.

°Use of the WDC

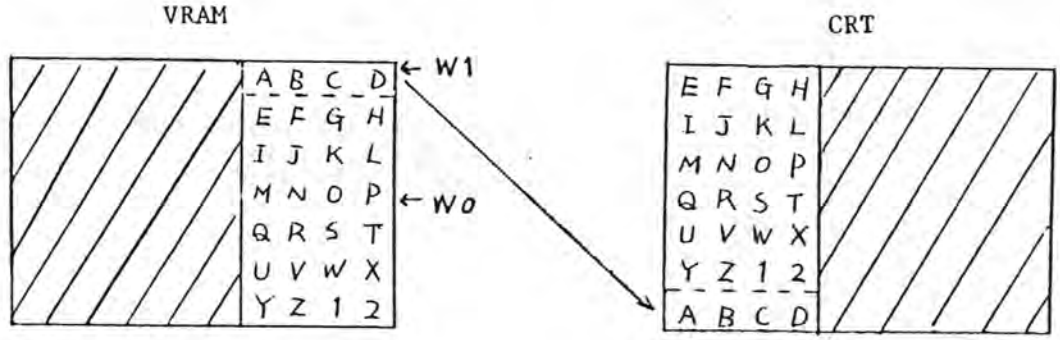
°Window overlay must be done by changing the priority.

°Relocation of the window must be done by changing the mapping RAM along with VMA.

°Scroll inside the window



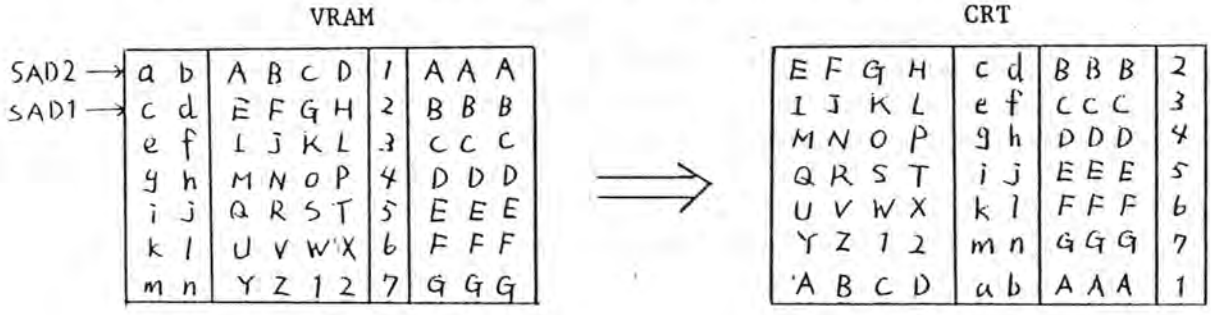
°Scroll can be attained by a change in VMA.
°Scrolling stops when it reaches the end (one window in use).



Or a single line revision

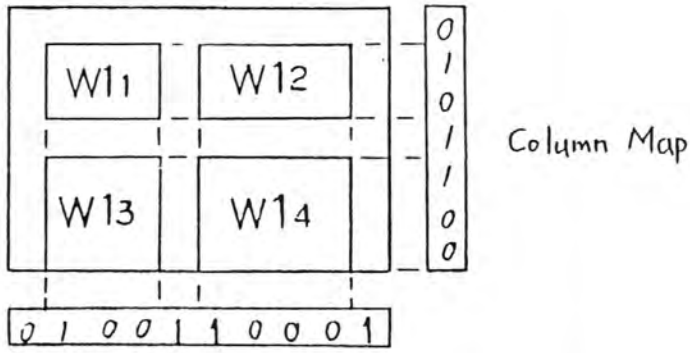
*When two windows are used in a part of the screen, it permits scrolling from the bottom end to the top end of the VRAM, which looks as if scrolling within one window. In such an occasion, the following screen setup and scroll may be possible.

(i) Two windows scrolling in different directions.
(ii) One window scrolling and two windows not scrolling.



*When the display is divided vertically as shown above, each window can be scrolled in the same direction at the same time by changing SAD1 and 2, without changing VMA.

°Others



As shown above, it is possible to have multiple number of windows in one window area of the mapping RAM. But, any desired area may not be specified as the window set in this manner is on the corresponding location on the VRAM as it is addressed by the same VMA.

WDC initialization

The WDC needs the following prior to sending of the START command.

1) All clear of the mapping RAM.
2) Setup of the mapping RAM, priority, VMA, and VDS for the screen to be displayed first.

Mapping RAM

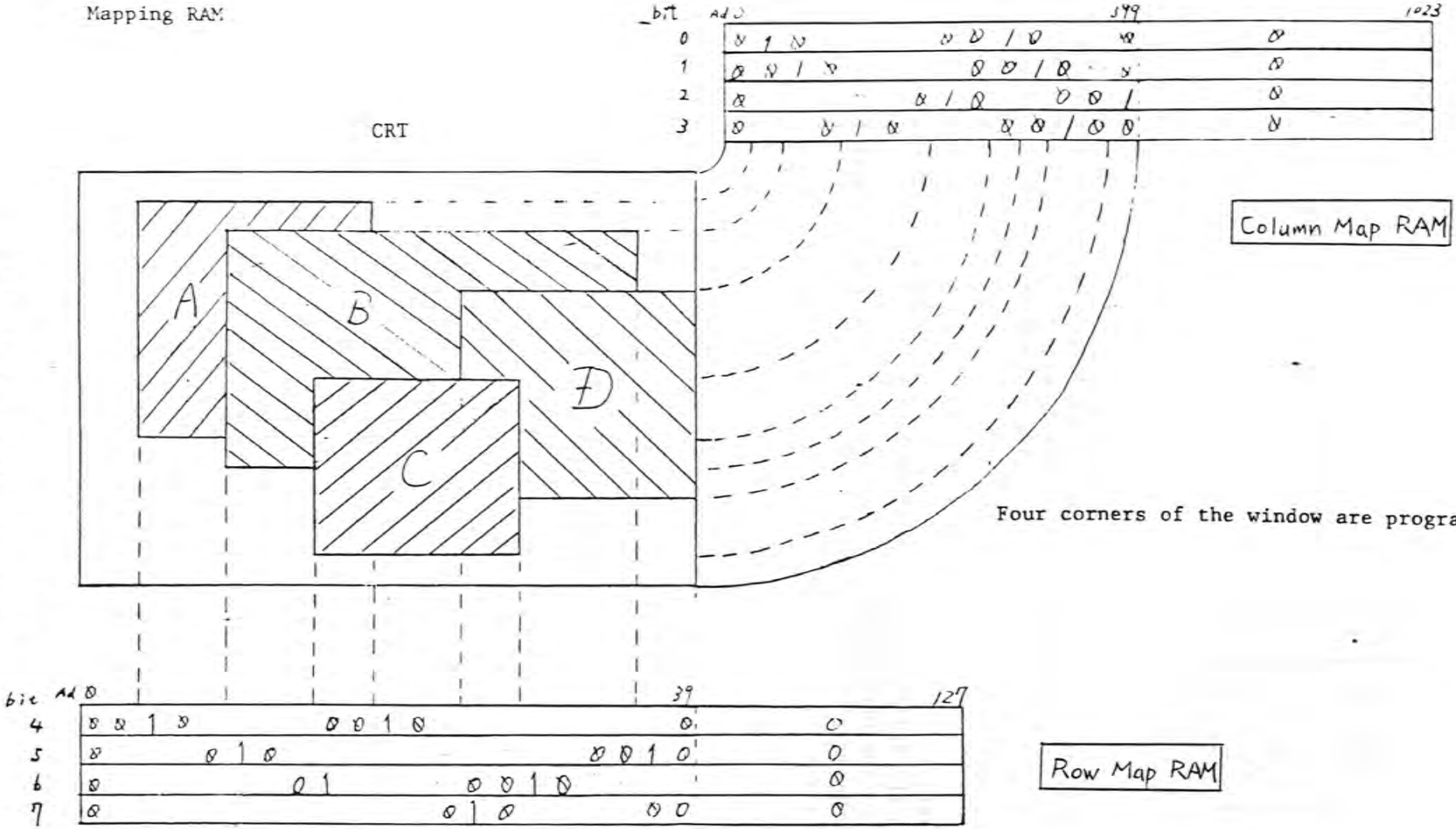


Fig.15-9 Use of the mapping RAM

°As shown above, the mapping information must be written after dividing it into the horizontal component and vertical component.

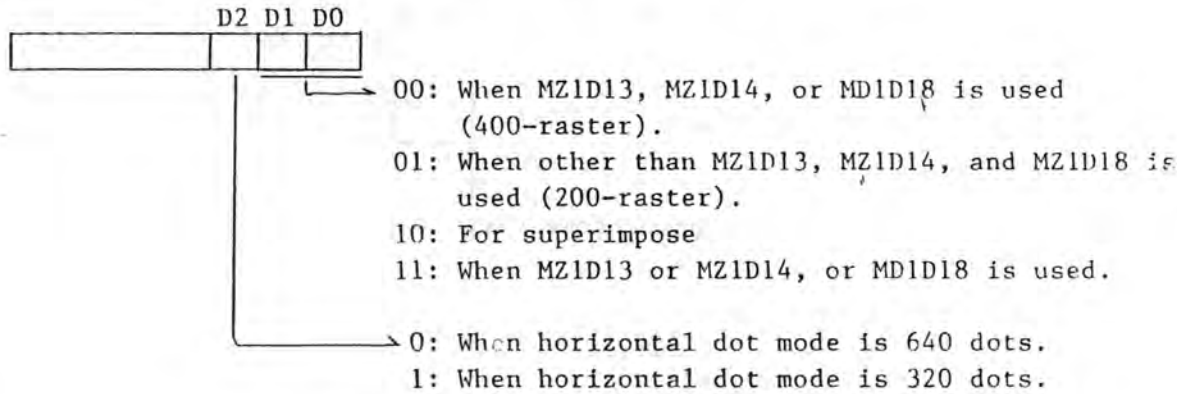
°Only 16 points must be programmed for setting four windows since one bit corresponds to one window and only the revised portions are written.

°The mapping RAM must be written using the graphic function of the GDC (single dot graphic).

°VDC1, VDC2

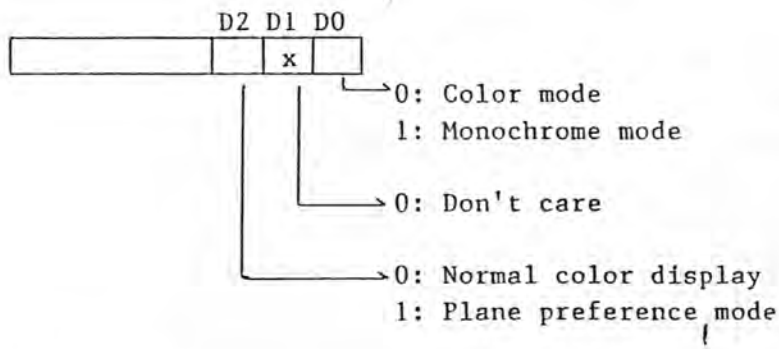
The VDC1 is the LSI which generates various timings and the VDC2 synthesizes display signal. Internal registers of these chips are write permitted.

°Resolution select register (I/O address 130H)



The resolution must be selected using the SYNC command of the GDC and the address 130H.

°Mode select register (I/O address 120H)



NOTE:
D2 must be programmed 0 in the case of the monochrome mode.

As the block diagram of the VDC2 is shown in Fig.15-10, D0 of the address 120H is the select signal for the last selector. Since planes, 0 - 2, are ANDed with VDS0 - 2, it has to be determined in the monochrome mode with which plane should it be ORed to display.

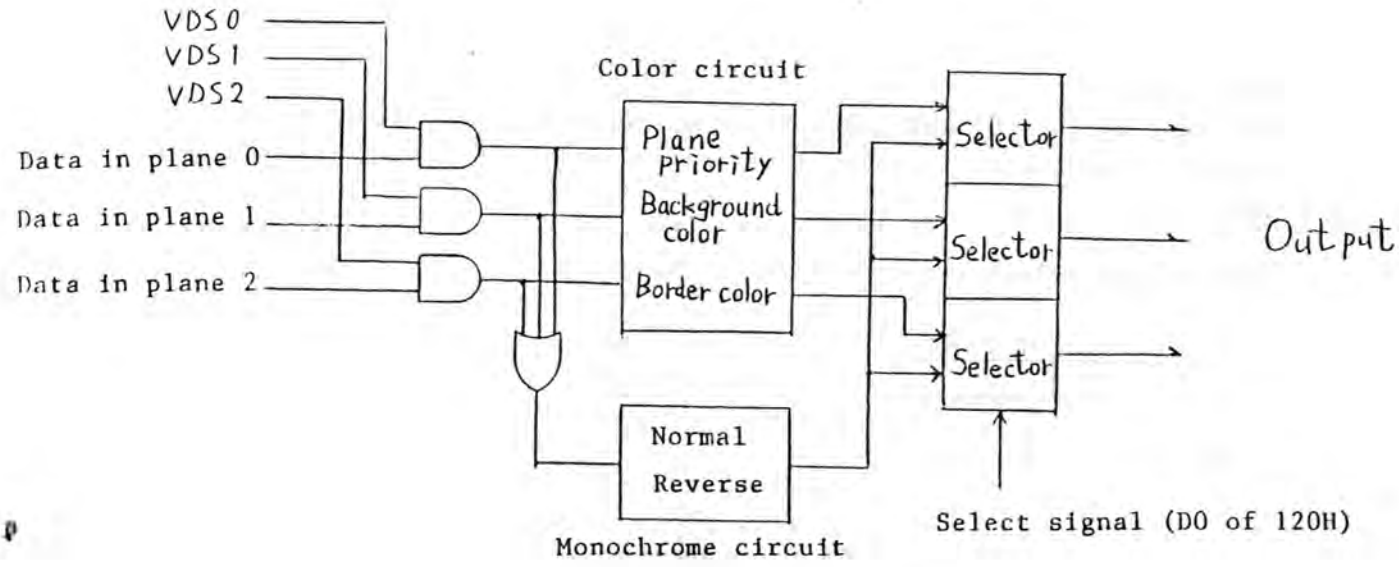


Fig.15-10 VDC internal

°Plane priority register (I/O address 122H)
Only when D2 of the I/O address 120H is 1, the display data are converted as in Table 15-5 by the value given to 122H.

Table 15-5

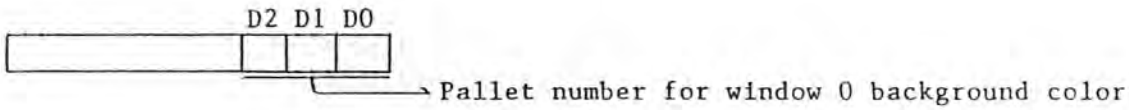
Value in 122H / Before change	After change: 0	1	2	3	4 ~ 7
0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0
0 0 1	0 0 1	0 0 1	0 0 1	0 0 1	0 0 1
0 1 0	0 1 0	0 1 0	0 1 0	0 1 0	0 1 0
0 1 1	0 1 1	0 1 1	0 1 1	0 1 1	0 1 1
1 0 0	0 0 0	1 0 0	1 0 0	1 0 0	1 0 0
1 0 1	0 0 1	0 0 1	1 0 0	1 0 0	1 0 0
1 1 0	0 1 0	0 1 0	0 1 0	1 0 0	1 0 0
1 1 1	0 1 1	0 1 1	0 1 1	0 1 1	1 0 0

Plane 2 Plane 1 Plane 0

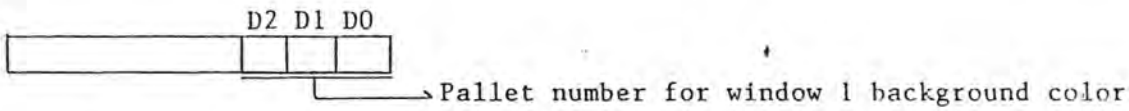
Priority order is given for four kinds of data composed of the plane 2 data, plane 1, and plane 0. The data of plane 2 would not be obtained if 0 was set when there is a data in the plane 2, as it is lower in its priority order than the four kinds of data composed of plane 1 and plane 0.
As the value is increased, it makes the plane 2 priority changed higher. Giving the value of 4 - 7 will make it higher in its priority than any of four kind data composed of the plane 1 and plane 0, so that data of plane 1 and plane 0 are not obtained.

°Background color register (I/O address 124H - 12AH)
Pallet number must be given to the background color of each window. Background color is given to the all zero area of the display data. Background color is displayed when planes 0 through 2 are all zero, VDS0 through VDS 2 are all zero, and the display data after converted in the priority mode are all zero.

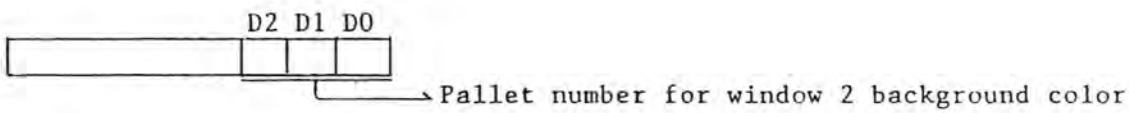
°124H



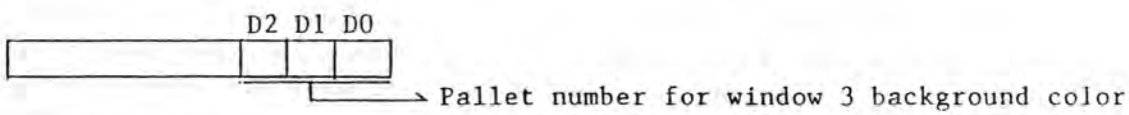
°126H



°128H

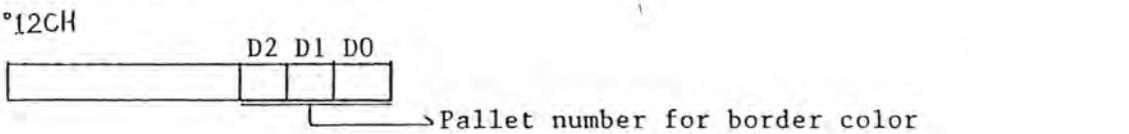


°12AH



°Border color register (I/O address 12CH)
Specifies pallet number of border color. Border color is the color outside the window.

°12CH

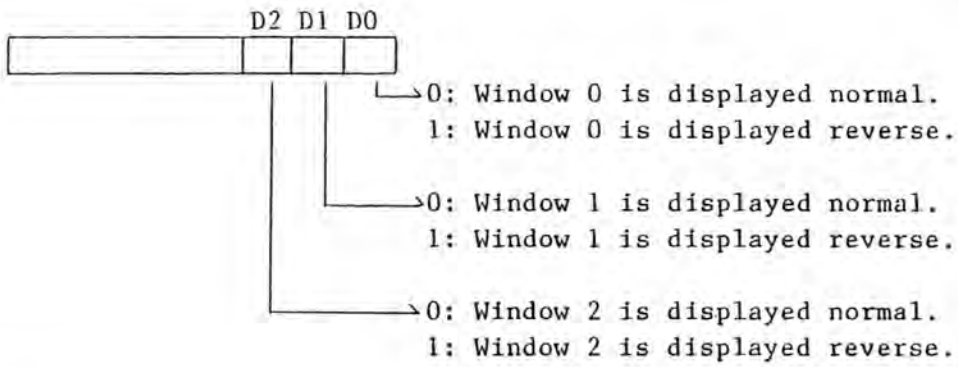


NOTE:
As a correct border color may not be produced when the MZ1D13, MZ1D14, or MZ1D18 is in use due to restriction to the CRT, it has to be programmed so as to produce black color.

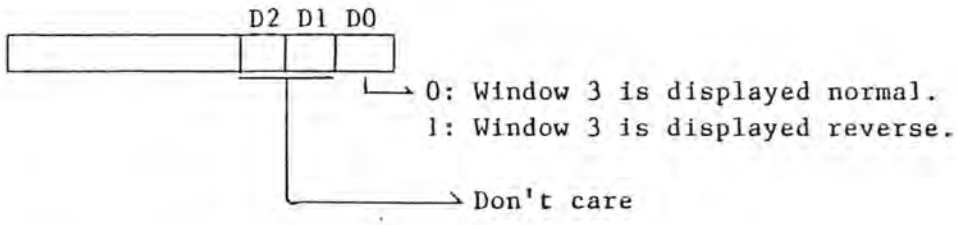
°Monochrome mode

Under the monochrome mode, different significance is given to 12CH and 12AH, which requires to select normal or reverse for the window.

°12CH



°12AH

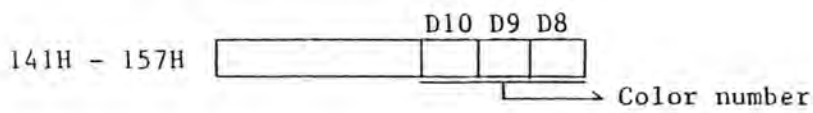


°Pallet register (LS670)

Colors displayed on the video screen and tones on the green video display depend on the presets set in the pallet register. As data written in the video RAM are read to be displayed at the same time from planes 0, 1, and 2, it may constitute a number 0 to 7, if they are assumed to be three digits binary number having the plane 0 for LSB and plane 2 for MSB, which is used to be the pallet number. What color be displayed by a pallet number depends on the color number set in the pallet register which is discussed next.

I/O address

141H: Color number for the pallet number 0
143H: Color number for the pallet number 1
145H: Color number for the pallet number 2
147H: Color number for the pallet number 3
151H: Color number for the pallet number 4
153H: Color number for the pallet number 5
155H: Color number for the pallet number 6
157H: Color number for the pallet number 7



Color number corresponds to the color (tone in the case of the monochrome CRT) in Table 15-6.

Color number	Color	Monochrome Brightness
0	Black	Black
1	Blue	(7)
2	Red	(6)
3	Magenta	(5)
4	Green	(4)
5	Cyan	(3)
6	Yellow	(2)
7	White	(1)

Brightness: (1) ⟶ (7)
Bright Dark

NOTE:
Since correct display is not assured for the MZ1D13, MZ1D14, and MZ1D18 due to restriction by the CRT, it has to be so programmed as to obtain color in the border portion.

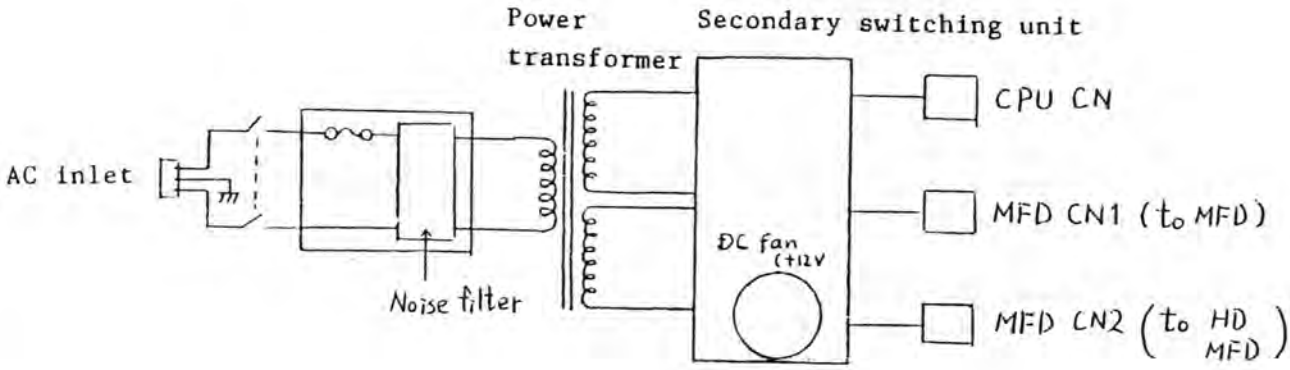
°Monochrome CRT tone display
As seen in the color number list above, tone display is enabled with the monochrome CRT (composite video input) is connected.

*Composite video input
Video signal (tone) coexists with the sync (vertical, horizontal) signal on the same signal line.

16. Power supply unit

Two kinds of power supply units are used for the MZ-5500/5600 series which differ in current capacity.

Model	Circuit type	VCC(+5V)	VDD(+12V)	VGG(-12V)	Alarm signal
MZ-5511 MZ-5521	Transformer + secondary switching type	9.2A	1.1A	0.15A	Yes
MZ-5631 MZ-5641 MZ-5645	Transformer + secondary switching type	10.8A	3.9A	0.15A	Yes



°Connector pin location

CPU CN

Pin No.	Signal name	Wire color
1	-12V	Blue
2	+12V	Yellow
3	+5V	Red
4	+5V	Red
5	ALARM	Orange
6	GND	Black
7	GND	Black
9	GND	Black

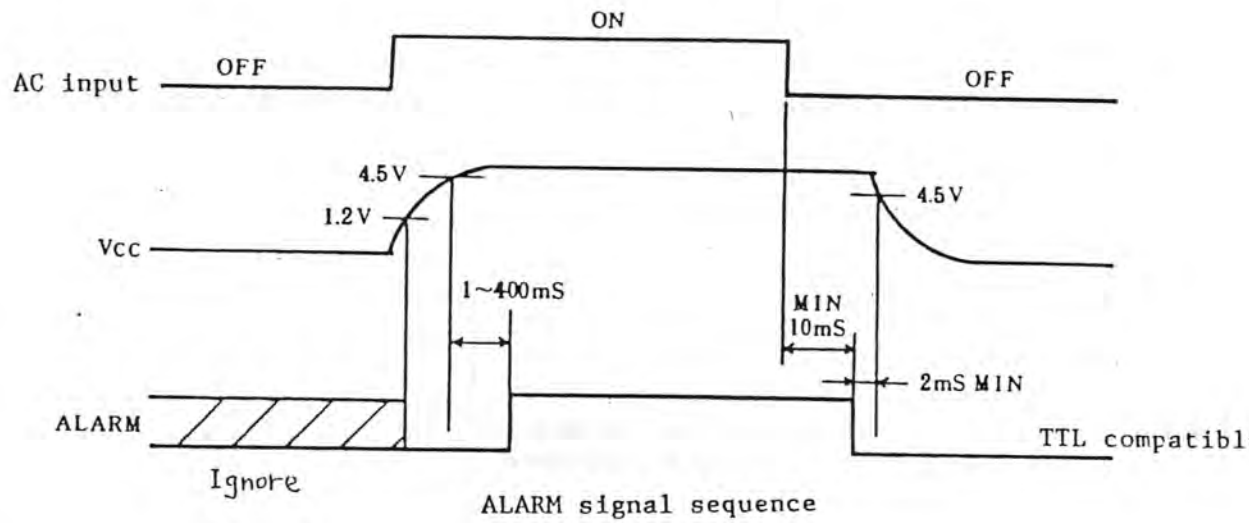
MFD CN1, 2

Pin No.	Signal name	Wire color
1	+12V	Yellow
2	GND	Black
3	GND	Black
4	+5V	Yellow

*The signal ground (SG) shares the line with the frame ground (FG).

°Alarm signal

Both types of the power supply units have the ALARM signal by which an abnormal condition in the DC output is detected as caused by a source supply failure or quick on/off of the power switch or when the CPU runswild or subjected to abnormal action. With this signal, immediate reset is applied to the CPU. The signal is an open collector output and pulled up to VCC level using a 2.2Kohms resistance. The ALARM signal is issued in the following sequence:



ALARM signal sequence

°Overcurrent protection

Both types have the overcurrent protection for VCC (+5V) and VDD (+12V) lines so that the output can be turned off when a short circuit is met or an abnormal load is added. However, the power supply unit may sometimes not recover its normal function immediately after removal of the cause. In such event, turn the power switch off, wait for 30 to 40 seconds, then turn power on. If power is not supplied on even after this, there may be a possible opening of the fuse or a trouble.

As no overcurrent protection is done to VGG (-12V), care must be exercised not to short the line. If shorted incidentally, it may burn out the fuse resistor or damage the output stage transistor.

17. 8087 Coprocessor option

The 8087 numerical data processor handles arithmetical operation of numeric data of various types and it has the capability to handle transcendental functions.

°Almost all signal lines are connected parallel with the 8086 CPU in view of the hardware. It does not require any special interface and has capacity to expand the CPU registers.
In view of software, the processing capacity of the CPU is largely increased as if the CPU commands are expanded.

°The 8087 NDP has eight 80-bit registers as shown in Fig.1 and its configuration is as shown in Fig.2. Almost all commands of the 8087 (data transfer, arithmetic operation, comparison) are executed with the register ST (0) or between ST (0) and other register ST (0 - 7) or the memory.

°There are seven kinds of data formats that can be handled (Fig.3), but they are converted into the format when fetched inside the 8087 before being stored (Fig.2).

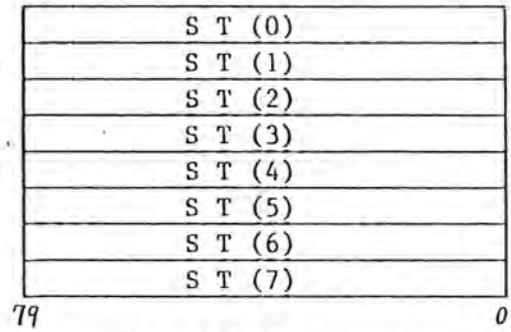


Fig.1 8087 registers

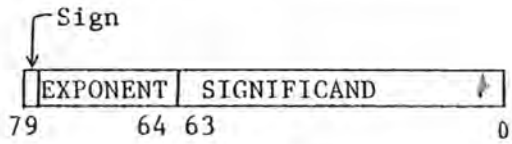


Fig.2 8087 register structure

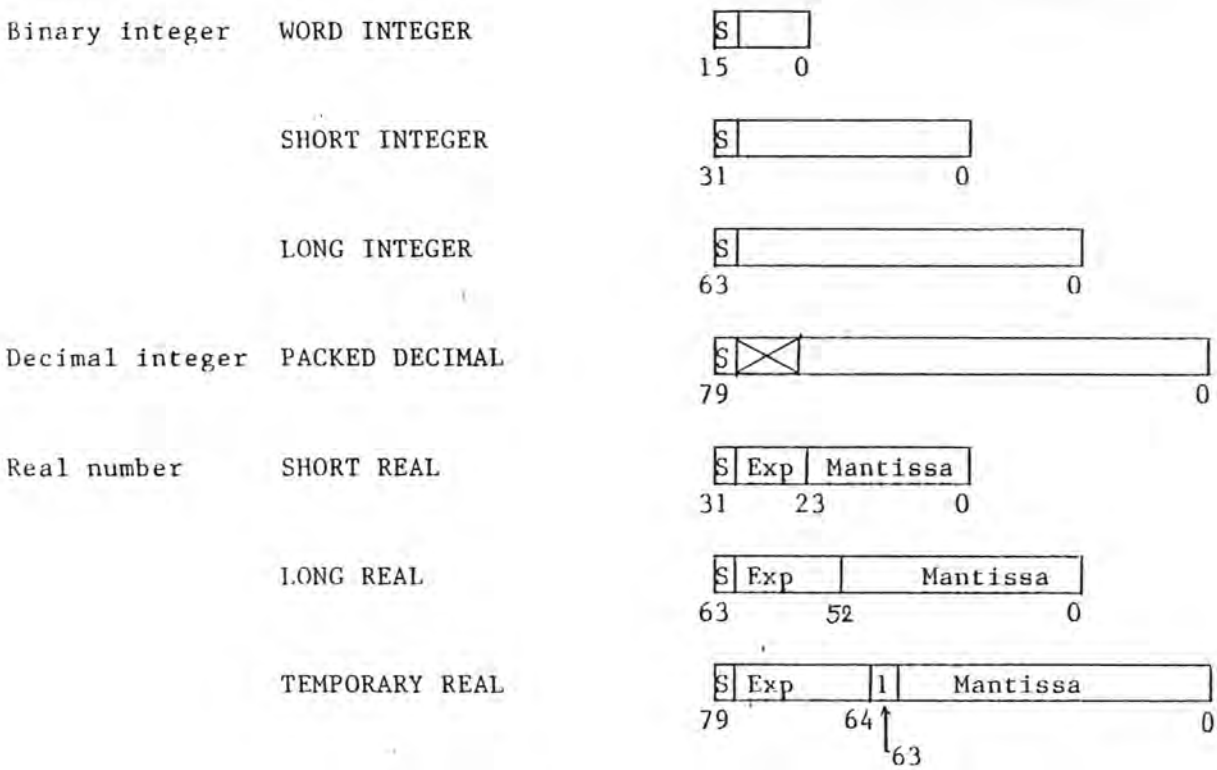


Fig.3 8087 data format

Complement of 2 is used to represent binary integer of 16 bits, 32 bits, or 64 bits, the most significant bit being a sign bit.
A BCD 18 digits are used to represent decimal integer, the most significant bit being a sign bit, and when the number becomes negative, only the sign is changed with rest of figure not affected. All bits of the most significant byte except the sign bit are disregarded when loaded and treated as 0 when stored.
Real number is represented in either of 32 bits, 64 bits, or 80 bits, having a sign bit, exponential bits, and mantissa bits. The true value of the mantissa can be obtained in the following manner, assuming the exponent as E and mantissa as F.

$$(-1)^S \cdot (2^{(E-BIAS)}) \cdot (1.F)$$

BIAS = 7FH (short real number)
3FFH (long real number)
3FFFH (temporary real number)

A negative real number is simply attached with a negative sign to the real number. The exponential part is provided for easier data comparison and has been added with the above mentioned bias. The following is an example to compare.

+ 5	00000101	BIAS →	10000100
-40	11011000	+7FH	01010111
+10	00001010	BIAS →	10001001
+21	00010101	+7FH	10010100
- 7	11111001	BIAS →	01111000
-11	11110101	+7FH	01110100

If not biased, it needs to distinguish comparisons between the same signs and different signs. But, when biased, comparison can be done with a first different bit by making comparison from high order bit, similar as the unsigned binary integer.
As the integer part is 1 for the mantissa, the maximum effective digits are maintained for a number smaller than 1. Table 1 shows an example how the real number 178.125 (decimal) is stored when represented in a form of short word length real number by the 8087.

Decimal	178.125		
Exponential type decimal	1.78125E2		
Exponential type binary	1.0110010001E111		
Exponential type binary, biased	1.0110010001E10000110		
8087 short word real number	Sign 0	Biased exp 10000110	01100100010000000000000

°The following shows the action of the 8086 CPU and the 8087 NDP when the next program is executed.

```
        CSEG
 1      ORG  100H
 2      MOV  AX,2000H
 3      MOV  DS,
 4      MOV  BX,0
 5      MOV  BP,2
 6      MOV  SI,4
 7      MOV  AX,1
 8      MOV  [BX],AX
 9      MOV  AX,2
10      MOV  DS:[BP],AX
11      MOV  AX,0
12      MOV  DS:[SI],AX
13  ;
14      (WAIT)
15      FINIT
16      (WAIT)
17      FILD [BX]
18      (WAIT)
19      FIADD DS:[BP]
20      (WAIT)
21      FIST DS:[SI]
22      WAIT
23  ;
24      MOV  DX,DS:[SI]
25      AND  DX,0FH
26      ADD  DX,30H
27      MOV  CL,2
28      INT 224
29
30      XOR  CX,CX
31      XOR  DX,DX
32      INT 224
33      END
```

This program adds the contents in 20000H with the contents of 20002H and the result is stored in 20004H using the 8087.

	Command	8086	8087
1		Memory address	Commands fetched are all
}		1 to 20000H.	disregarded.
		2 to 20002H.	
12		0 to 20004H.	
14	WAIT	Test pin is checked. Advances to a next step, if 0 (8087 being not busy).	At not busy state. WAIT command disregarded.
15	FINIT	Disregarded as it is a NDP command.	Executes the same function as hardware reset.
16	WAIT	Similar as 14, it waits until the 8087 turns not busy (8 clocks at a maximum).	In busy state while the reset is being carried out.
17	FILD [BX]	The EU does nothing as it is a NDP command. Because the NDP needs to refer the memory, the BIU creates the physical address from DS and BX and dummy read cycle is executed. →	The address is stored in the data pointer inside the NDP during the dummy cycle the CPU executes. ↓ $\overline{RQ}$ pulse is issued to the CPU to request for the bus privilege.
		Upon receiving of $\overline{RQ}$, $\overline{GT}$ pulse is sent out to release the bus for use, → if satisfactory.	Memory read cycle is executed from the address implied by the data pointer to push the data in ST(0). The data in ST(n) is stored in ST(n+1), then.
		An integer type data are ⟹ automatically converted into the real type temporarily and stored.	*If the command is the long real load command, four memory cycles are needed. ↓
		Goes into a next bus cycle. ←	Release pulse is returned to the CPU to open the bus free.
18	WAIT	Similar as 14.	Similar as 14.
19	FIADD DS:[BX]	Similar as 17.	Though similar as 17, addition of ST(0) with the data is stored in ST(0), instead of storing the data in ST(0).
20	WAIT	Similar as 14.	Similar as 14.