SHARP SERVICE MANUAL

CODE：00ZMZ5600HIFE

10MB/20MB NEW HARD DISK INTERFACE For MODEL MZ1F10/MZ5600A

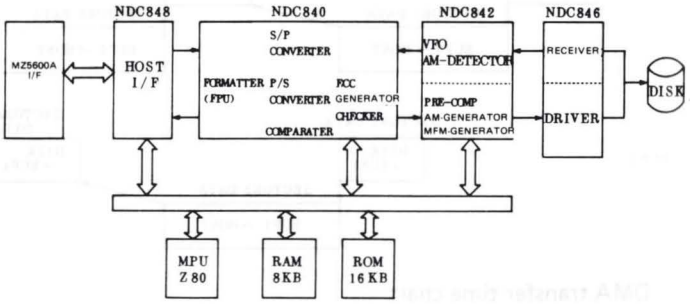
CONTENTS

SHARP CORPORATION

1. GENERAL

DUNTK1517 ACZZ is constructed with four exclusive LSIs, CPU Z-80 and others.

The description here is mainly on the LSIs.



2. HOST INTERFACE

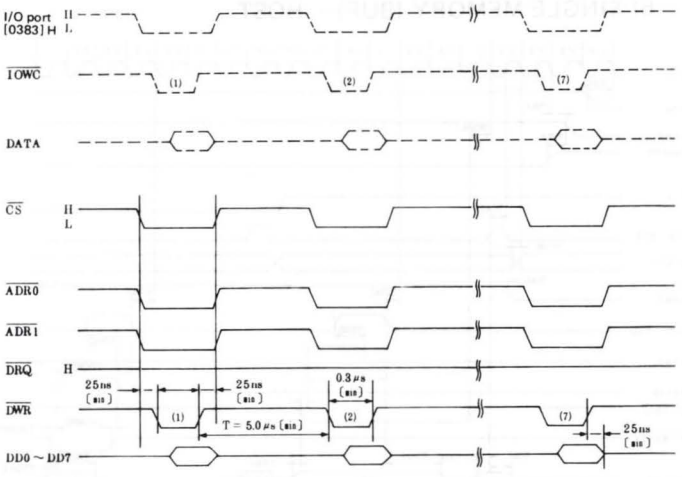
NDC-848 is an LSI device for the NCL host interface. NDC-848 can be easily conncted with the host and can construct a disk controller with NDC-840 (HDC) and others.

Commands and Data Write from the host are set in the internal register of NDC-848 and are transferred to RAM by DMA of NDC-840.

Status and Data Read are set by DMA in the register of NDC848 and are read by the host.

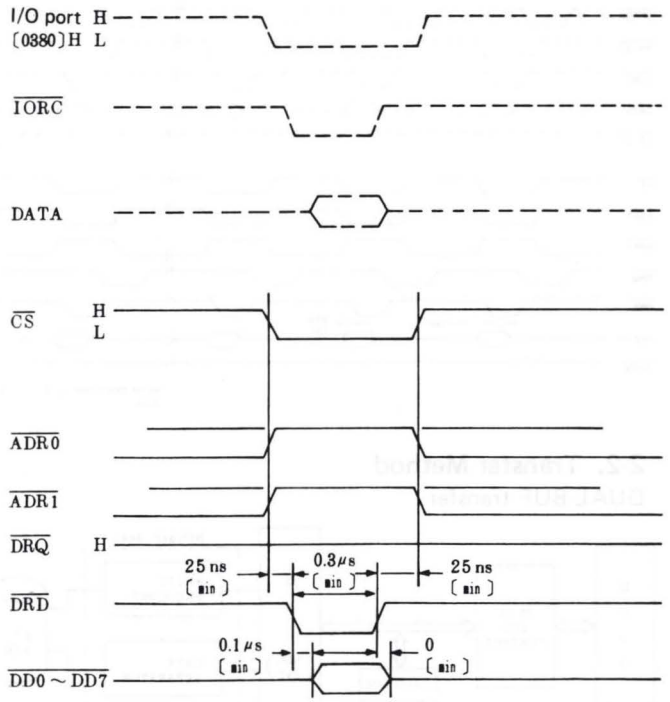
2-1. Main Operation Time Chart

(1) COMMAND SET



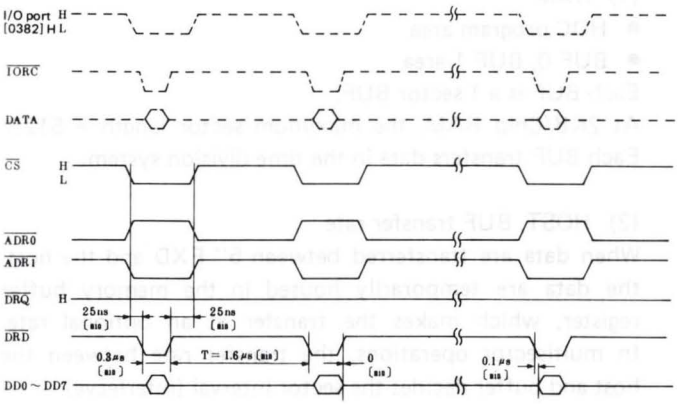
note: – – – – – host signals
——— internal signals

(2) STATUS READ

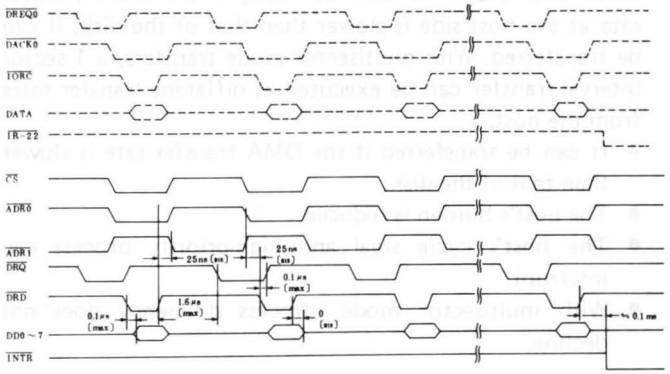


note: – – – – – host signals
——— internal signals

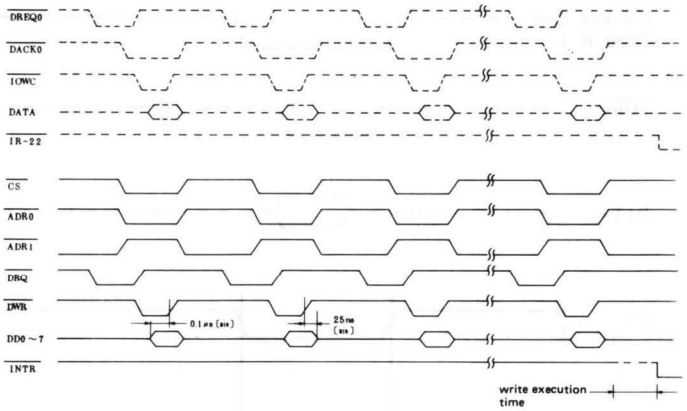
(3) RESULT READ

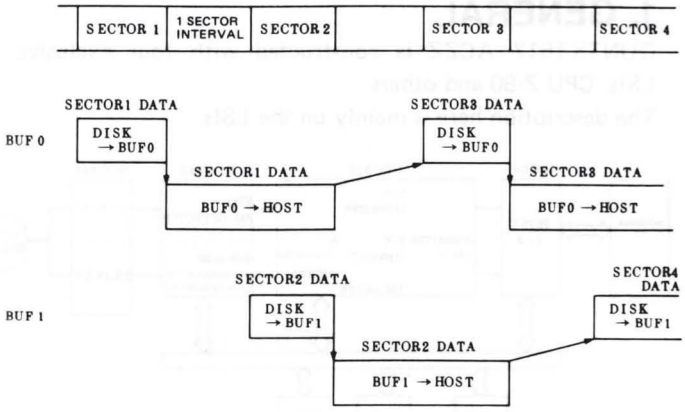


(4) DATA READ (DMA)



(5) DATA WRITE (DMA)

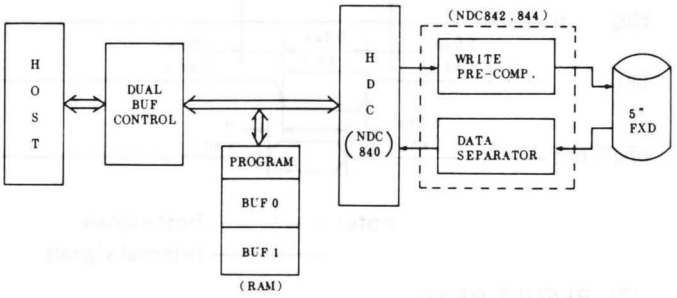




DMA transfer time chart

2-2. Transfer Method

DUAL-BUF transfer



(1) RAM

- HDC program area
- BUF 0, BUF 1 area

Each BUF is a 1 sector BUF.

At 2KB/Chip RAM, the maximum sector length = 512B.

Each BUF transfers data in the time division system.

(2) HOST, BUF transfer rate

When data are transferred between 5" FXD and the host, the data are temporarily housed in the memory buffer register, which makes the transfer at an optional rate. In multisector operations, the transfer rate between the host and buffer decides the sector interval (interleave).

(3) DUAL-BUF

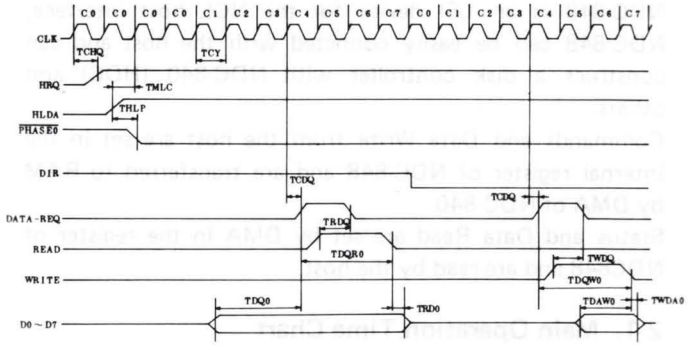
When DUAL-BUF is used as HDC, if the DMA transfer rate at the host side is slower than that of the disk, it can be transferred. With multisector mode transfers, a 1 sector interval-transfer can be executed at different transfer rates from the host.

- It can be transferred if the DMA transfer rate is slower than that of the disk.
- The host's burden is reduced.
- The host's cycle steal and high-priority process can interrupt.
- With multisector mode, process dificiency does not decline.

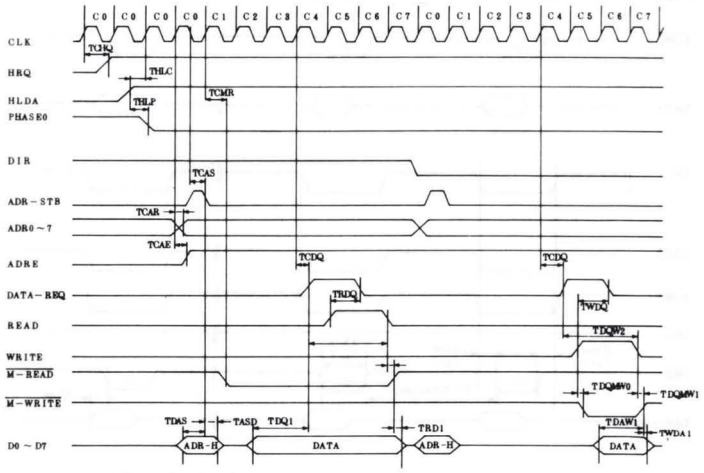
(e.g.) Read Data (disk → host)

disk transfer rate	5Mbit/s (1.6μs/byte)
host transfer rate	3.2μs/byte

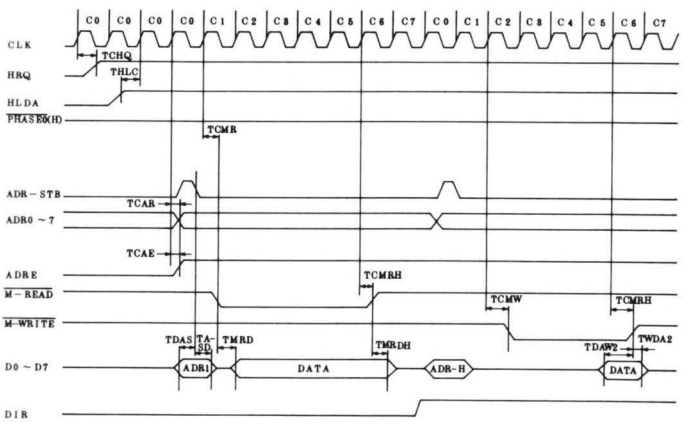
a) SINGLE MODE, DISK – HOST



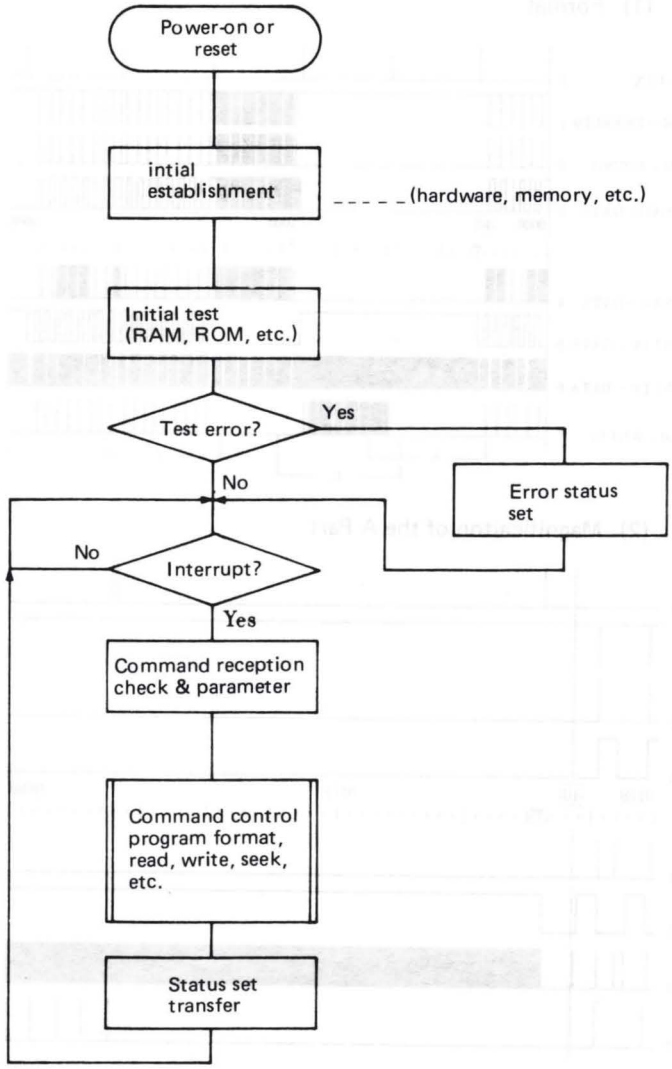
b) SINGLE MEMORY (BUF) – HOST



c) SINGLE MEMORY (BUF) – DISK

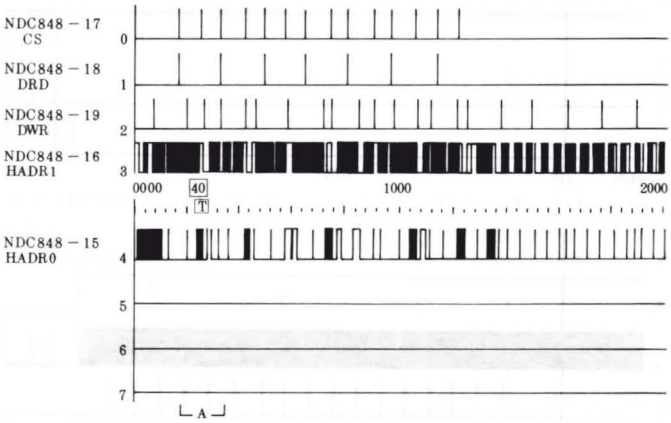


2-3. Basic Operations General Flow Chart

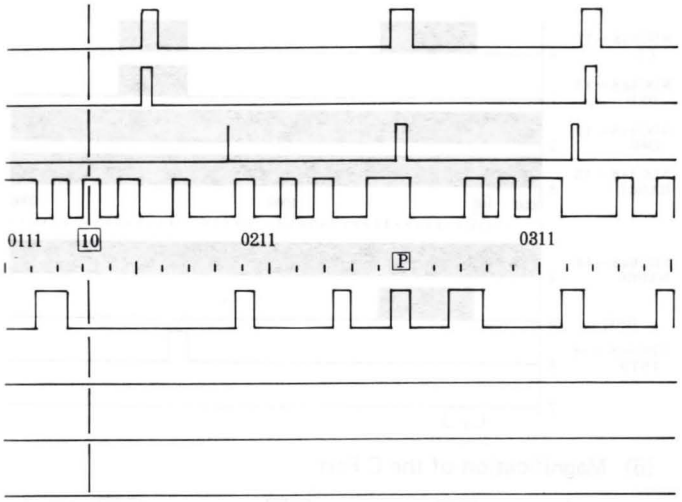


2-3-1. Timing

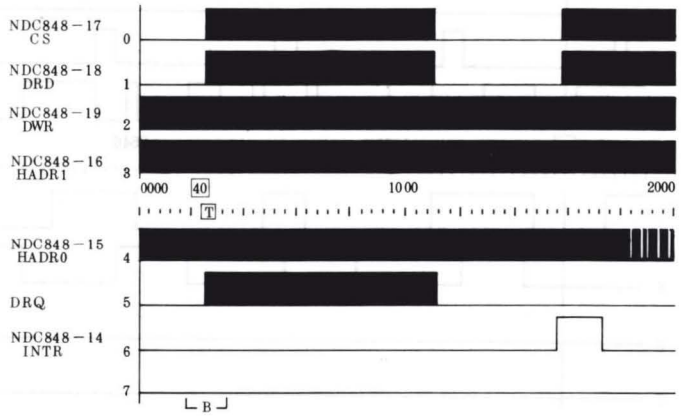
(1) Command Transfer



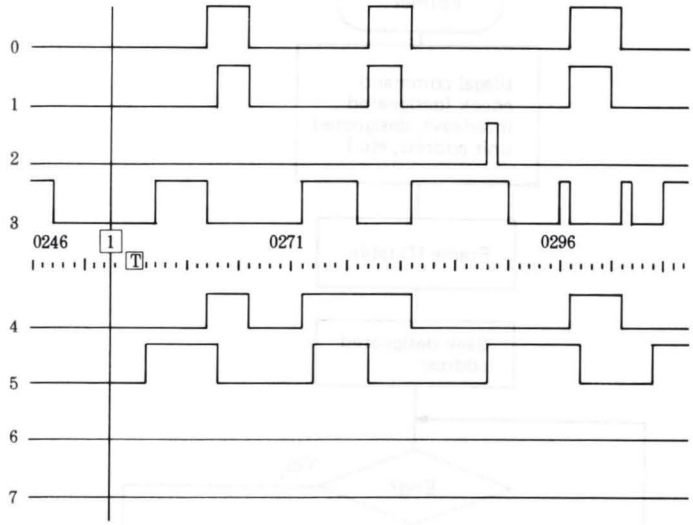
(2) Magnification of the A Part



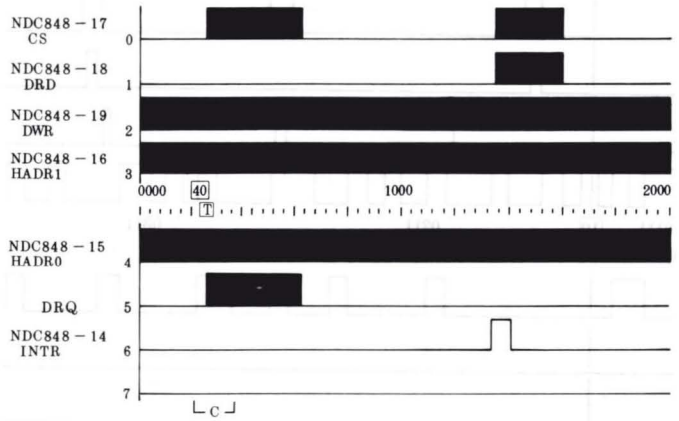
(3) Data Read



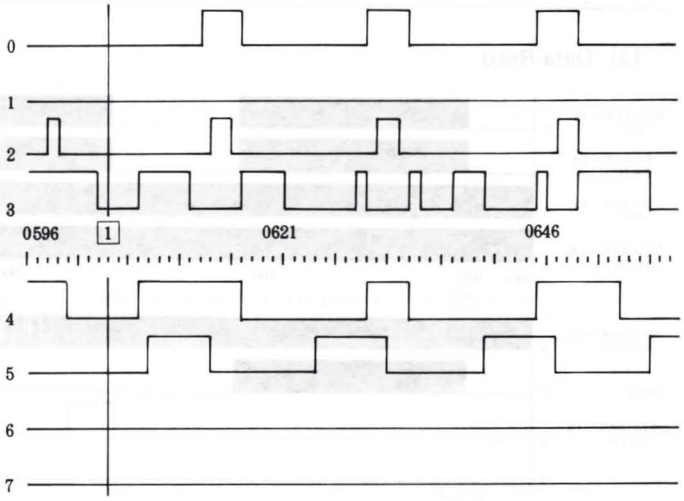
(4) Magnification of the B Part



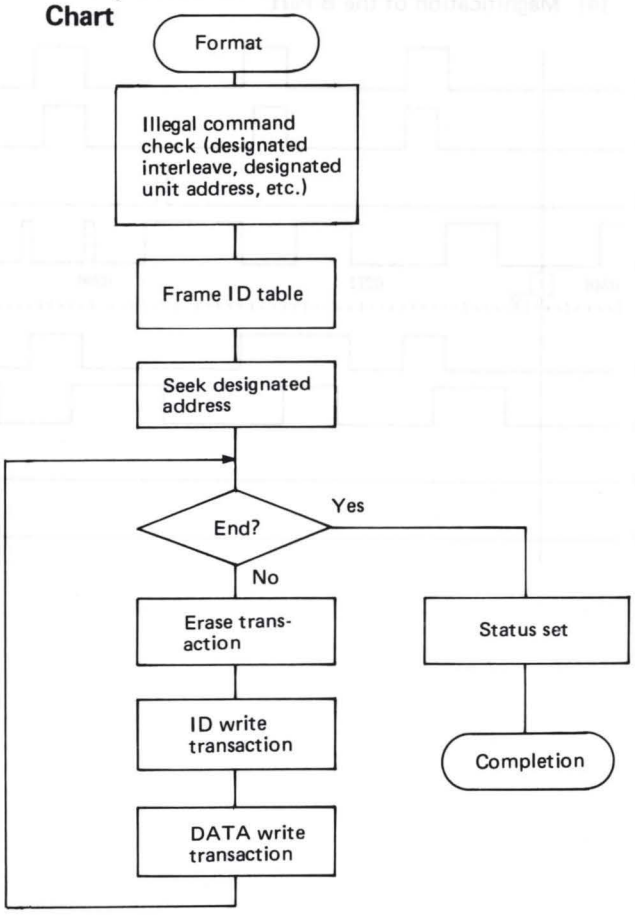
(5) Data Write



(6) Magnification of the C Part

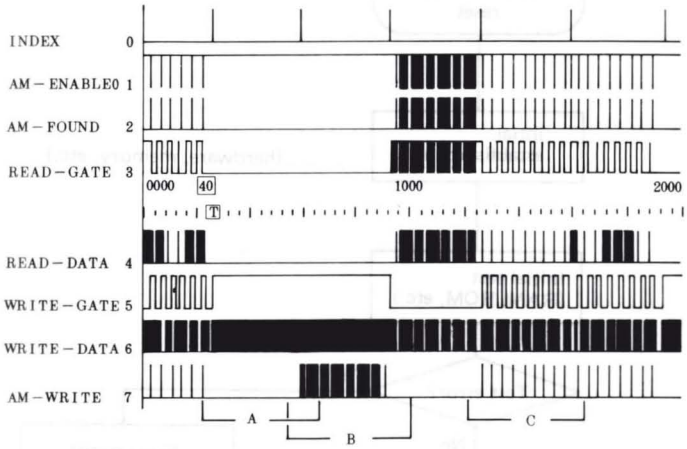


2-4. A Prepresentative Command General Flow Chart

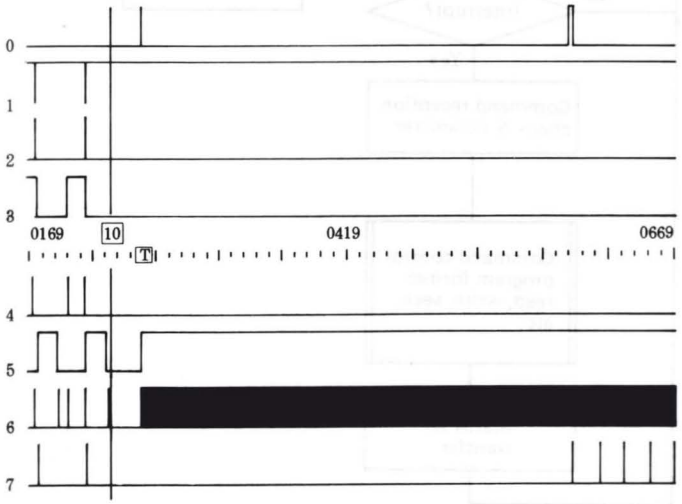


2-4-1. Timing

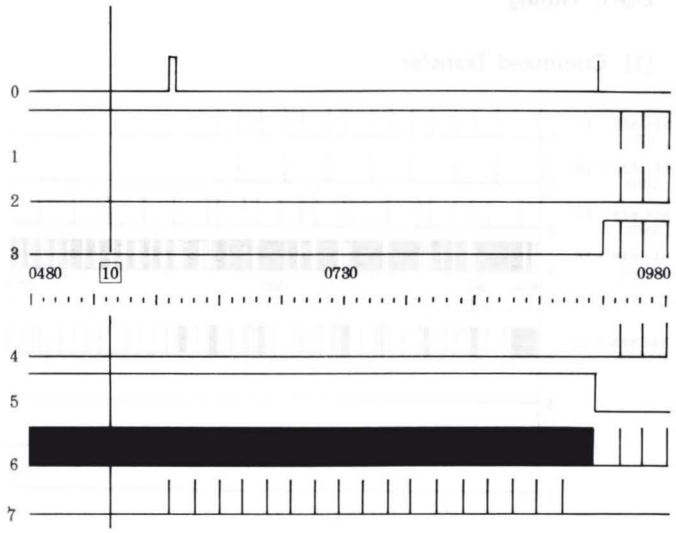
(1) Format



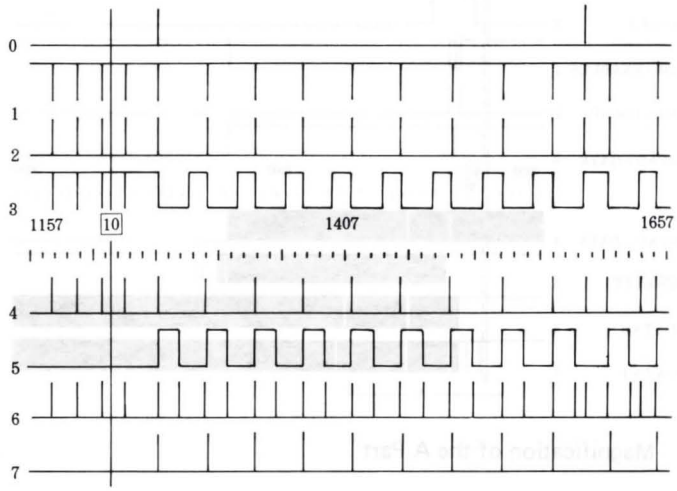
(2) Magnificaiton of the A Part



(3) Magnification of the B Part



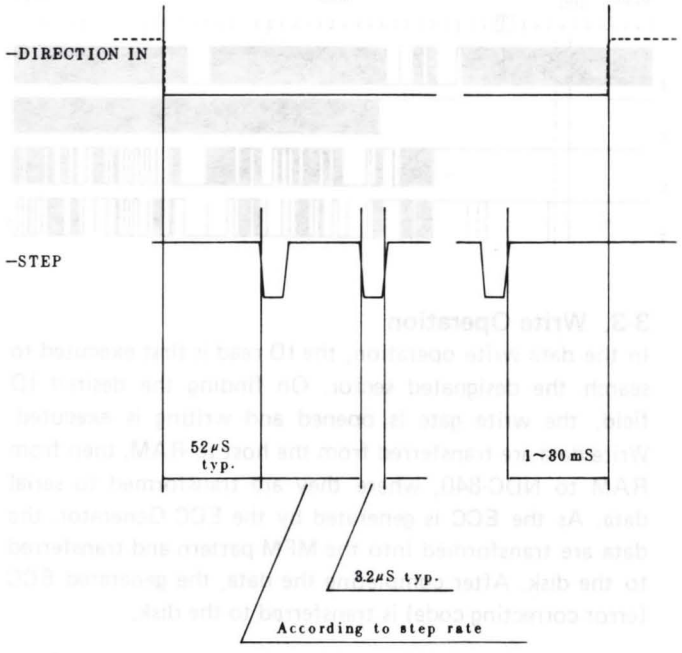
(4) Magnification of the C Part

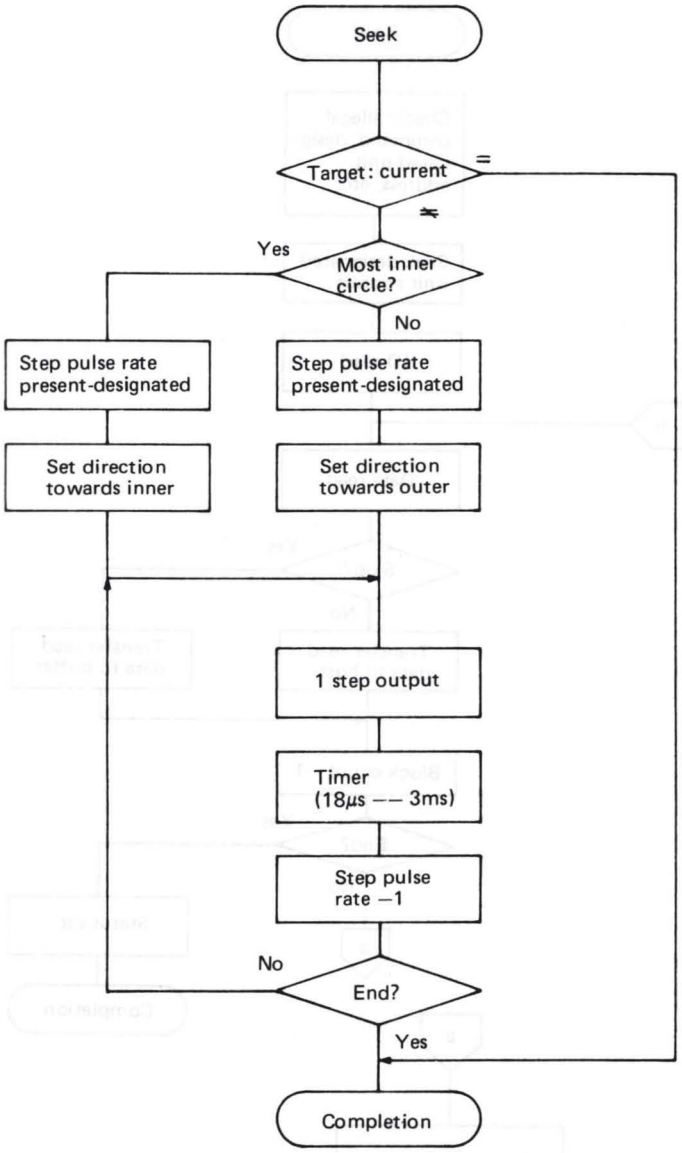


3. BASIC OPERATION

3-1. Seek Operation

The step for seeking is generated by FPU (NDC 840). The step rate is designated by a command from the host.





3-2. Read Operation

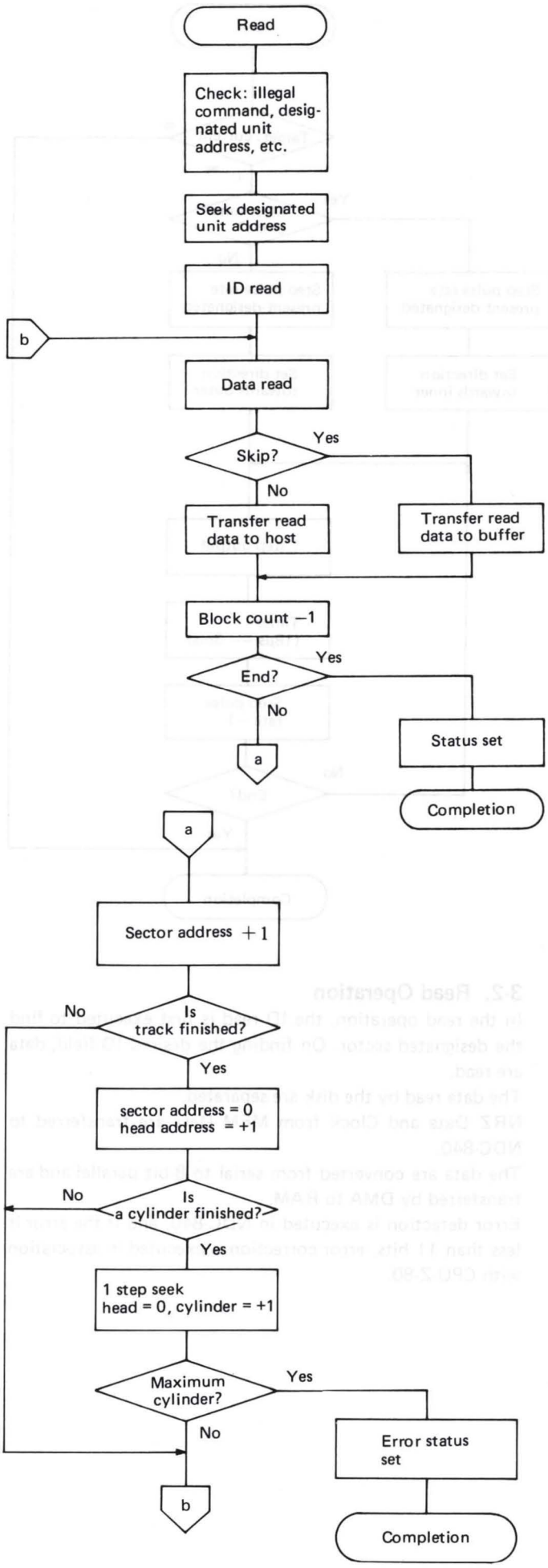
In the read operation, the ID read is first executed to find the designated sector. On finding the desired ID field, data are read.

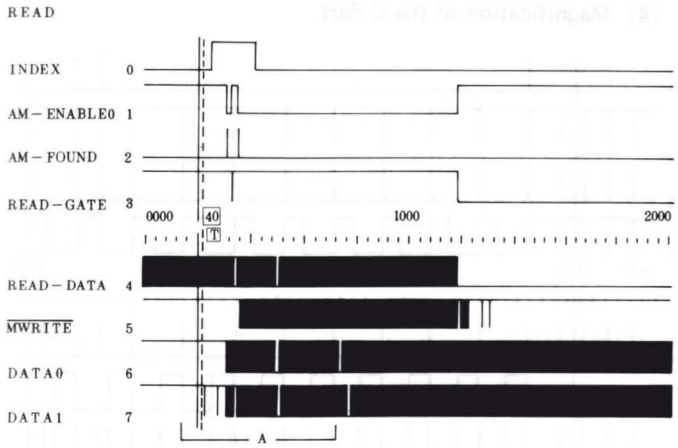
The data read by the disk are separated.

NRZ Data and Clock from MFM Data are transferred to NDC-840.

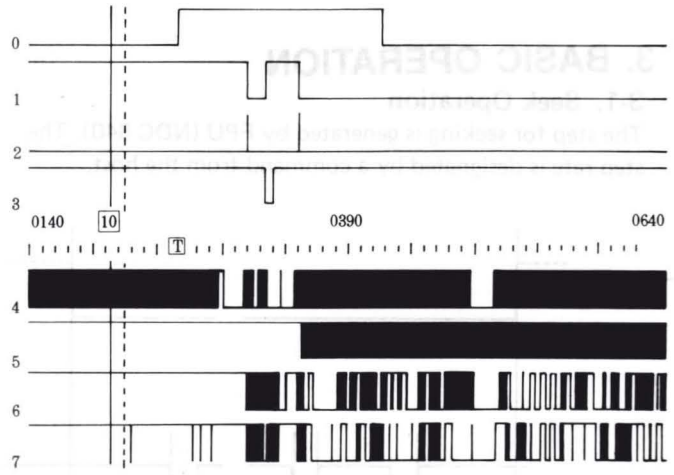
The data are converted from serial to 8-bit parallel and are transferred by DMA to RAM.

Error detection is executed in NDC-840, and if the error is less than 11 bits, error correction is executed in association with CPU-Z-80.



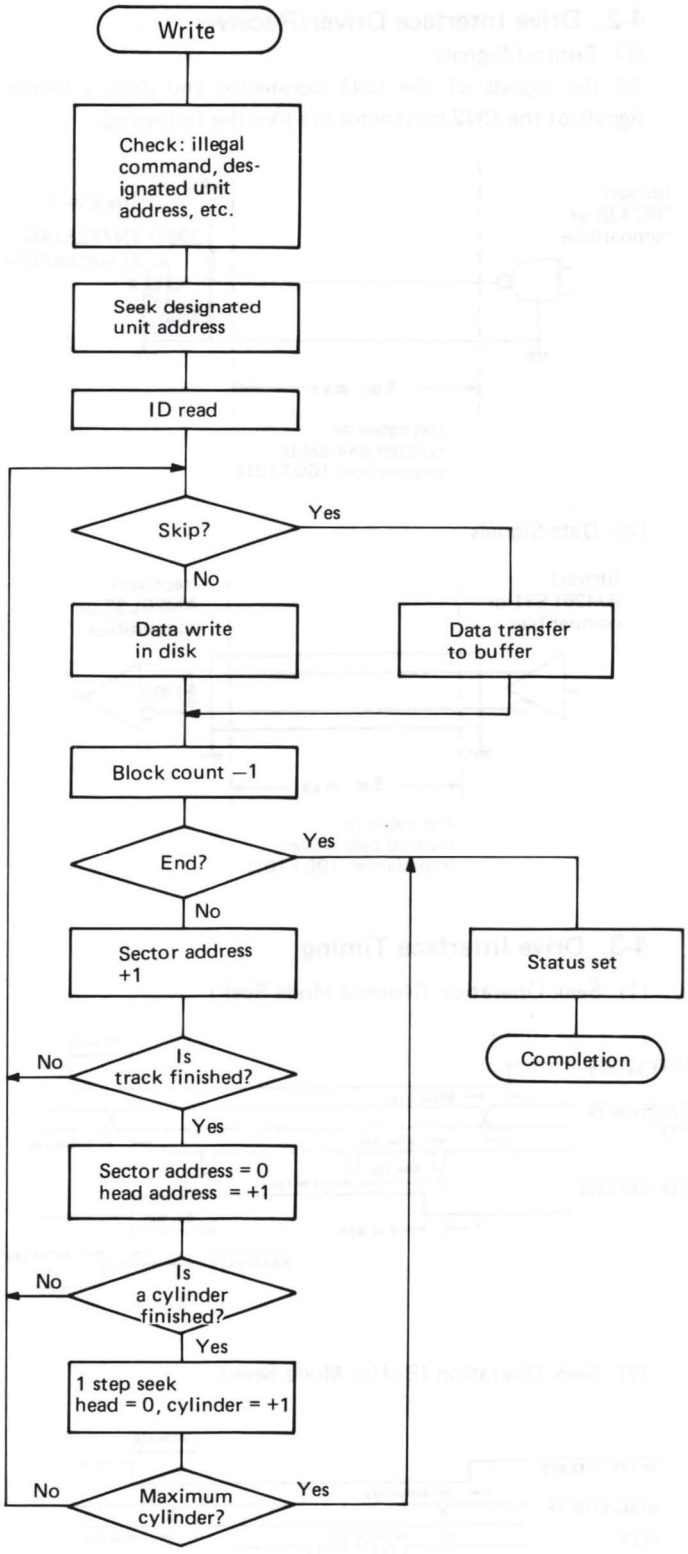


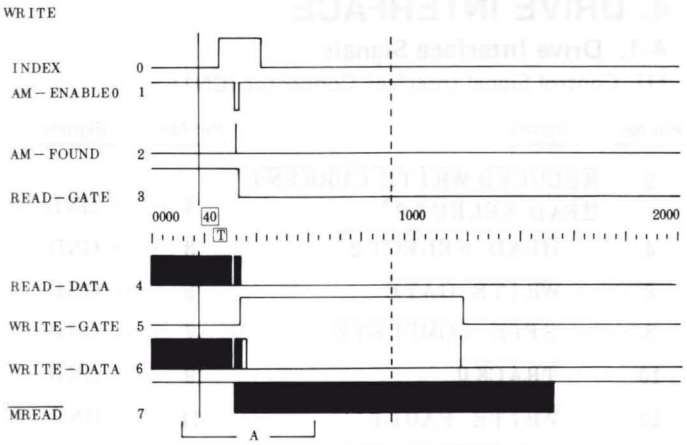
Magnification of the A Part



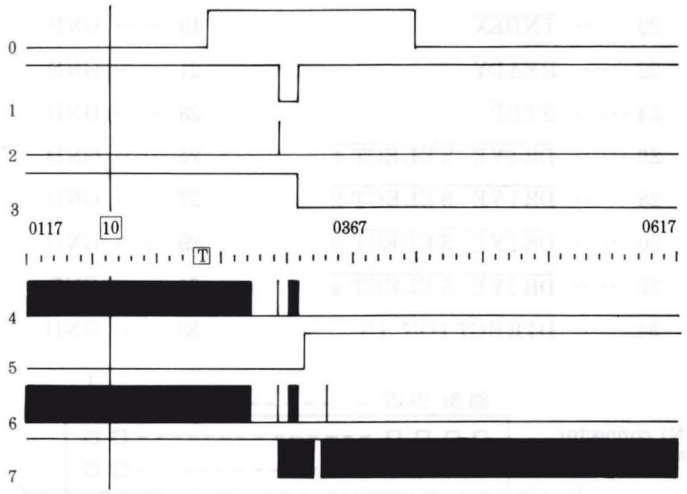
3-3. Write Operation

In the data write operation, the ID read is first executed to search the designated sector. On finding the desired ID field, the write gate is opened and writing is executed. Write data are transferred from the host to RAM, then from RAM to NDC-840, where they are transformed to serial data. As the ECC is generated by the ECC Generator, the data are transformed into the MFM pattern and transferred to the disk. After completing the data, the generated ECC (error correcting code) is transferred to the disk.





Magnification of the A Part

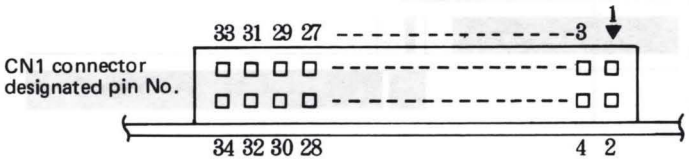


4. DRIVE INTERFACE

4-1. Drive Interface Signals

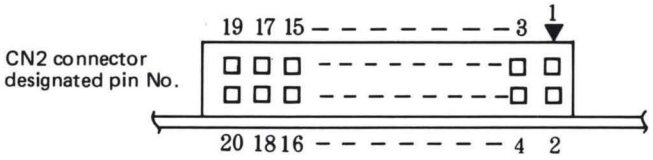
(1) Control Signal Interface Connector (CN1)

Pin No.	signals	Pin No.	Signals
2	$\overline{\text{REDUCED WRITE CURRENT/ HEAD SELECT 2}^3}$	1	GND
4	$\overline{\text{HEAD SELECT 2}^2}$	3	GND
6	$\overline{\text{WRITE GATE}}$	5	GND
8	$\overline{\text{SEEK COMPLETE}}$	7	GND
10	$\overline{\text{TRACK 0}}$	9	GND
12	$\overline{\text{WRITE FAULT}}$	11	GND
14	$\overline{\text{HEAD SELECT 2}^0}$	13	GND
16	RESERVED	15	GND
18	$\overline{\text{HEAD SELECT 2}^1}$	17	GND
20	$\overline{\text{INDEX}}$	19	GND
22	$\overline{\text{READY}}$	21	GND
24	$\overline{\text{STEP}}$	23	GND
26	$\overline{\text{DRIVE SELECT 1}}$	25	GND
28	$\overline{\text{DRIVE SELECT 2}}$	27	GND
30	$\overline{\text{DRIVE SELECT 3}}$	29	GND
32	$\overline{\text{DRIVE SELECT 4}}$	31	GND
34	$\overline{\text{DIRECTION IN}}$	33	GND



(2) Data Signal Interface Connector (CN2)

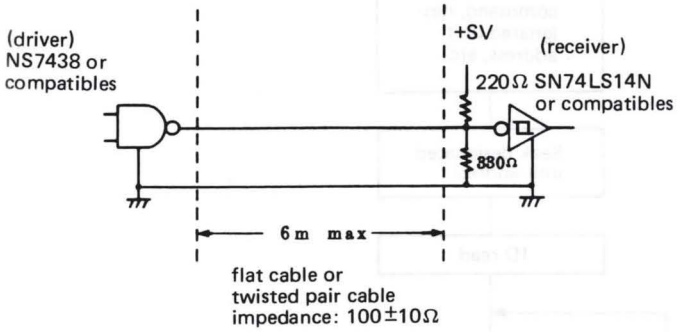
Pin No.	Signals	Pin No.	Signals
2	GND	1	$\overline{\text{DRIVE SELECTED}}$
4	GND	3	RESERVED
6	GND	5	SPARE
8	GND	7	RESERVED
10	SPARE	9	SPARE
12	GND	11	GND
14	–MFM WRITE DATA	13	+MFM WRITE DATA
16	GND	15	GND
18	–MFM READ DATA	17	+MFM READ DATA
20	GND	19	GND



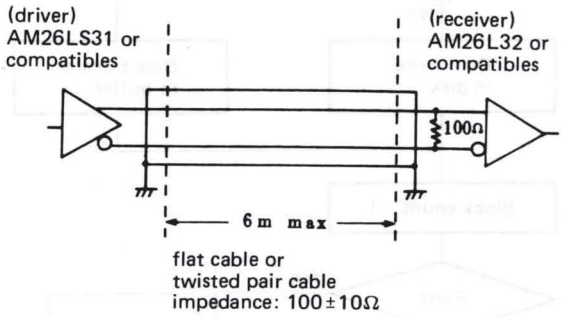
4-2. Drive Interface Driver/Receiver

(1) Control Signals

All the signals of the CN1 connector and drive selected signals of the CN2 connector are like the following.

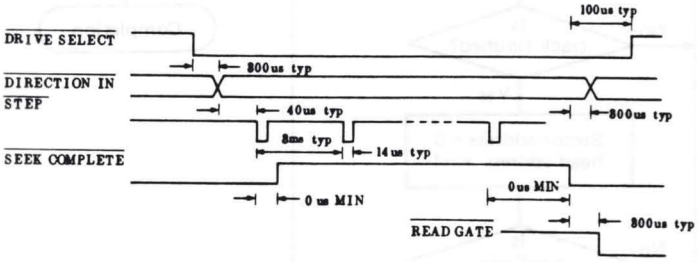


(2) Data Signals

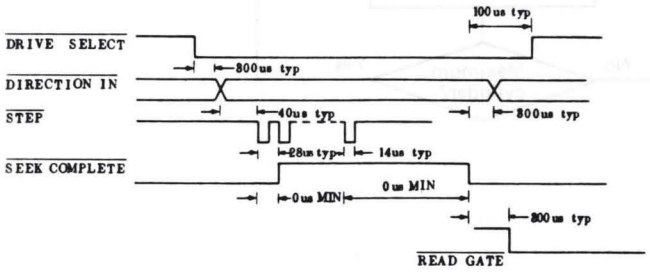


4-3. Drive Interface Timing

(1) Seek Operation (Normal Mode Seek)



(2) Seek Operation (Buffer Mode Seek)



4-4. Description of the Drive Interface Signals

4-4-1. Control Signals

(1) $\overline{\text{REDUCED WRITE CURRENT}}$ CONT ⟶ When this signal is Low, the Write current is reduced. Low occursat inner cylinder than 128.

(2) $\overline{\text{HEAD SELECT}}$ $2^0 \sim 2^2$ CONT ⟶ Head address is designated by a combination of three binary bits.

(3) $\overline{\text{WRITE GATE}}$ CONT ⟶ When this signal is Low, the Write data are written in the drive.

(4) $\overline{\text{SEEK COMPLETE}}$ CONT ⟶ When this signal is Low, it indicates the Seek operation has been completed. Read/Write operations are executed only on $\overline{\text{READY}}$ and this signal is Low.

(5) $\overline{\text{TRACK0}}$ CONT ⟶ When this signal is Low, it indicates the drive head is in the outermost cylinder. With the REZERO command, REV Seek is executed until this signals is detected.
When the power is on, the controller does not issue $\overline{\text{DRDY}}$ until this signal is detected.

(6) $\overline{\text{WRITE FALUT}}$ CONT ⟶ This indicates there was an abnormal condition in the drive.
When this signal is Low, the Read/Write operations are not executed.

(7) $\overline{\text{INDEX}}$ CONT ⟶ A pulse output once per rotation, indicating the beginning of the data track.

(8) $\overline{\text{READY}}$ CONT ⟶ This indicates the drive has reached the normal rotation speed.
Seek/Read/Write operations are executed only when this signal is Low.

(9) $\overline{\text{STEP}}$ CONT ⟶ This is a pulse signal to seek the head.
Seeking is made one cylinder per one pulse.
By selecting the jumper plug on the board, the following two ways of seeking are made available.
1. Normal mode Seek: Seeking is made per every pulse.
2. Buffer mode Seek: High-speed seeking is done by the high-speed pulse.

(10) $\overline{\text{DRIVE SELECT 1} \sim 4}$ CONT ⟶ With this signal, several drives connected to the controller are selected.
For this controller, a maximum of two drives are connectable.
This signal is kept High and in the De-Select condition except in Seek/Read/Write operations.

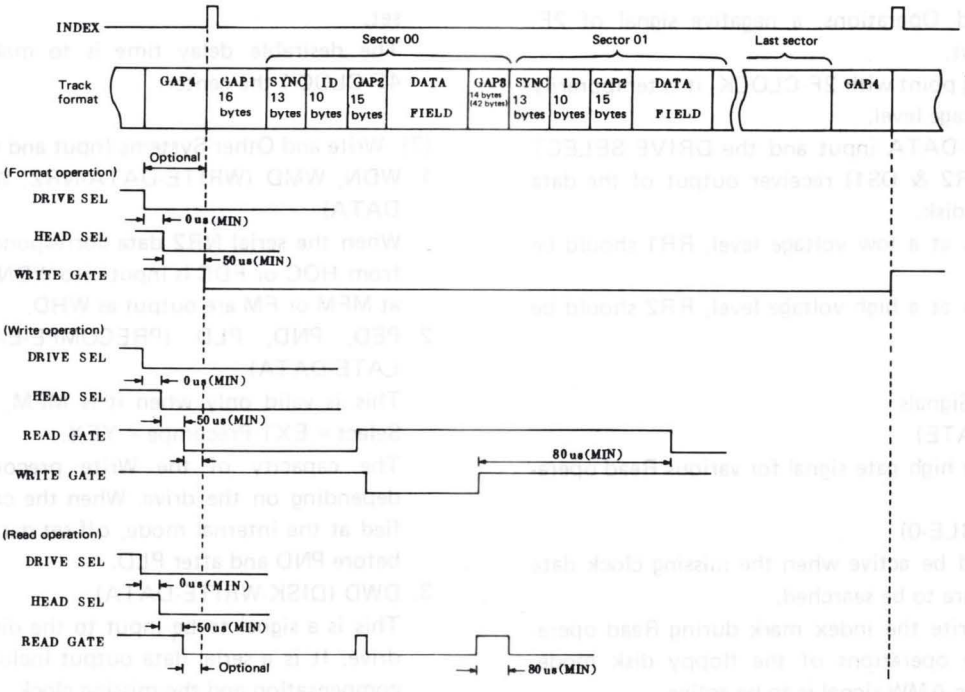
(11) $\overline{\text{DIRECTION IN}}$ CONT ⟶ This signal, which designates the head seeking direction has:,
forward (inward) direction at Low;
reverse (outward) direction at High;

(12) $\overline{\text{DRIVE}}$ CONT ⟵ A signal to indicate the drive designated by the $\overline{\text{Drive Select 1} \sim 4}$ is selected.

4-4-2. Data Signals

(1) ±MFM WRITE DATA CONT ⟶ This is a data signal to write in the drive. It is sent as a differential signal.

(2) ±MFM READ DATA CONT ⟵ This is a data signal to read from the drive. It is sent as a differential signal.



5. ENCODER/DECODER, DATA SEPARATOR

5-1. General

NDC-842 was developed to further simplify the connection of the hard disk drive and controller. It has the same advantages as T1 NDC10 (MB15546) and is enabled to connect with a 5-inch disk drive and floppy disk drive.

5-2. Features

1. VFO data separating function.
2. Built-in domestic PLL circuit, phase comparator for NDC-844 and 847.
3. Copes with double density (MFM) and single density (FM) record system.
4. Missing data detecting function.
5. Double density (MFM) write compensation support.
6. DC5V single power supply.

5-3. Operations of NDC842

(1) Reset Input

1. RST Input
   This active high input clears all the registers including the mode register and initializes this chip.

(2) Clock Input

1. 4FC (4F-CLOCK)
   This is a basic clock used for internal controls and the write circuit; a half circle of this clock is output as 2F-CLOCK.
2. VCK (VCO-CLOCK)
   This generates the output clock in the VCO circuit. In Read operations, the clock generated from this clock is output as the Read-Clock.

(3) Clock Output

1. 2FC (2F-CLOCK)
   This outputs a half cycle of 4F-CLOCK.
2. RCK (READ-CLOCK)
   This outputs the clock generated from VCO-CLOCK in Read operations, the and the Read-Data is correspondingly output.
   Except in Read Operations, a negative signal of 2F-CLOCK is output.
   At the switching point with 2F-CLOCK, it is temporarily set at a high voltage level.
   Input the RAW-DATA input and the DRIVE SELECT signal (RR1, RR2 & DS1) receiver output of the data is sent from the disk.
   - When DS1 is at a low voltage level, RR1 should be selected.
   - When DS1 is at a high voltage level, RR2 should be selected.

(4) Read Control Signals

1. RGT (READ-GATE)
   This is an active high gate signal for various Read operations.
2. AE0 (AM-ENABLE-0)
   Active – should be active when the missing clock data (address mark) are to be searched.
   It enables to write the index mark during Read operations and Write operations of the floppy disk mode. For the latter the AMW signal is to be active.

(5) Write Control Signals

1. WGT (WRITE-BATE)
   This is an active high gate signal for various Write operations.
2. AMW (AM-WRITE)
   Active – this should be active when data (address mark) including the missing clock are to be written. For writing the index mark of the floppy, AE1 is also necessary.

(6) Read and Other Systems Input and Output

1. RDM (RAW-DATA-M)
   An active low input signal is necessary to recognize the internal sink field. It is a gate signal for the bit counter of the raw-data.
   Therefore, when 00 is used as the synchronized field, a control signal is necessary which becomes a low voltage level upon the detection of the 1F cycle pattern at MFM and 2F cycle pattern at FM.
2. DD0, DD1, DD2 (DELAY-DATA-0, 1, 2)
   The reading edge in all cases is the rise time.
   The raw-data selected by the DS1 signal is basically output to DD0. DD0 maintains a high voltage level except at DD1 input.
   - DD1 corrects the width of raw-data, which inputs pulse delayed as much as the data width.
     e.g.: for 5Mbit/s Disk Drive
     10 ~ 25ns delay
   - DD2 is a signal to be input into the built-in phase comparator. Half of the 4F-CLOCK cycle delay from DD0 is desirable.
3. RSE, RSN, RSL (READ-STROBE-E, N, L)
   The reading edge in all cases is the rise time.
   These are the strobes to be input into the internal data separator through the same gate.
   The reading margin is different between the inner and the outer of the media for some disk drives, therefore it is established to be used for error recovering by inputting off-set data before and after RSN to make it possible to select each strobe depending on the mode set.
   The desirable delay time is to make a half cycle of 4F-CLOCK the center.

(7) Write and Other Systems Input and Output

1. WDN, WMD (WRITE-DATA-NRZ, WRITE-MODIFIED-DATA)
   When the serial NR2 data corresponding to ZF-CLOCK from HOC or FDC is input into WDN, the data modified at MFM or FM are output as WHD.
2. PED, PND, PLD (PRECOMPE-EARLY, NORMAL, LATE-DATA)
   This is valid only when it is MFM, and the Precompe Select = EXT Precompe = YEX.
   The capacity of the Write precompensation differs depending on the drive. When the capacity is not satisfied at the internal mode, off-set data PED will be input before PND and after PLD.
3. DWD (DISK-WRITE-DATA)
   This is a signal to be input to the disk interface output drive. It is a serial data output including the Write precompensation and the missing clock.

(8) Write Precompensation Detecting Pattern

The precompensation bit pattern is shown below.

The pattern shows the 3rd bit timing, monitored by the 4-bit shift register.

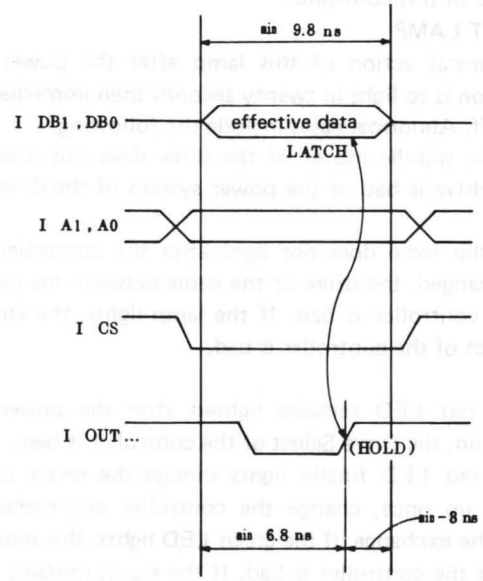
	bit pattern	precompensation
0	0 0 0 0	NORMAL CLOCK
1	0 0 0 1	EARLY CLOCK
2	0 0 1 0	NORMAL DATA
3	0 0 1 1	LATE DATA
4	0 1 0 0	
5	0 1 0 1	
6	0 1 1 0	EARLY DATA
7	0 1 1 1	NORMAL DATA
8	1 0 0 0	LATE CLOCK
9	1 0 0 1	NORMAL CLOCK
A	1 0 1 0	NORMAL DATA
B	1 0 1 1	LATE DATA
C	1 1 0 0	
D	1 1 0 1	
E	1 1 1 0	EARLY DATA
F	1 1 1 1	NORMAL DATA

*The data are effective at MFM.

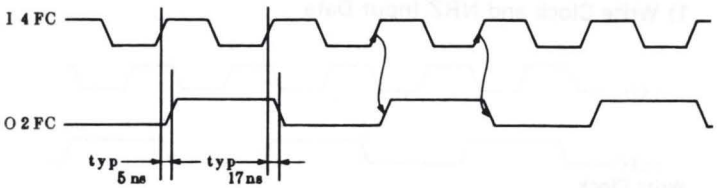
When the precompensation select is internal, precompensation is added.

5-4. Timing

(1) Mode Set Input

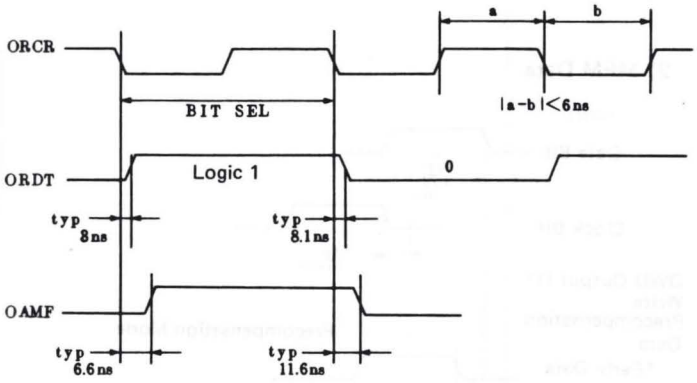


(2) 4F-Clock Input and 2F Clock Output

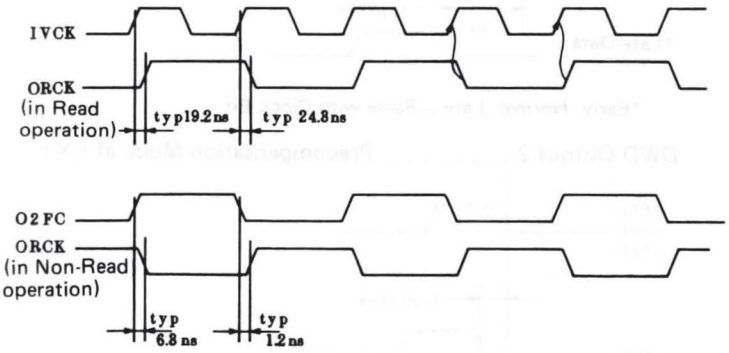


(3) Read Input/Output

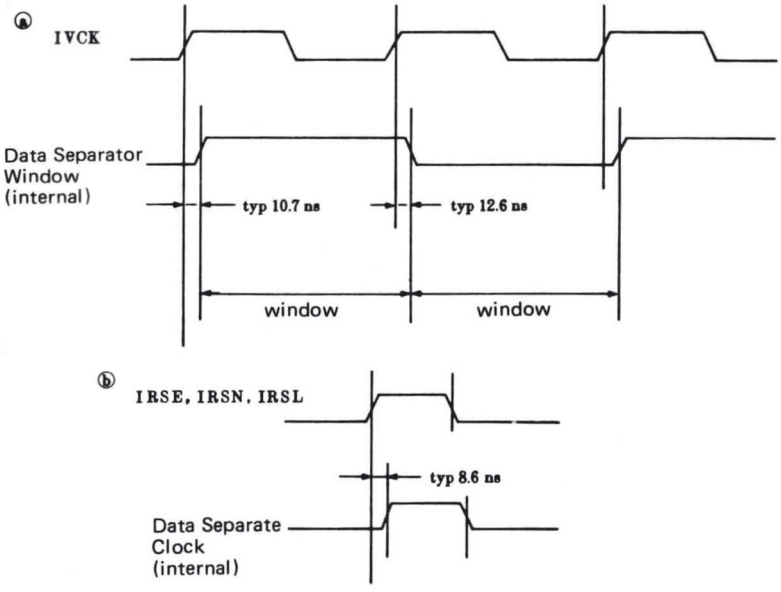
1) Read Clock and NRZ Output Data



2) Read Clock (in Read operation/Non-Read operation)

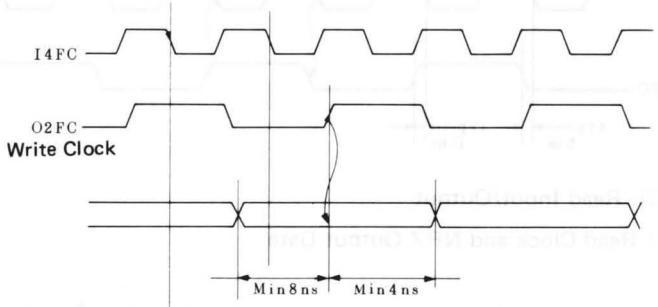


3) IVCKとリードストローブ(IRSE, IRSN, IRSL)

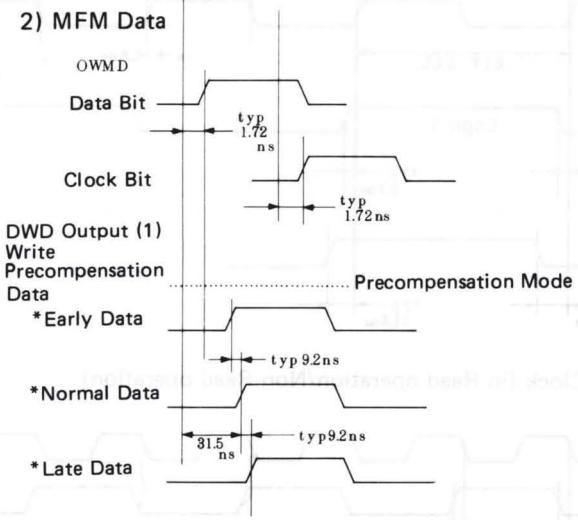


(4) Write Input/Output

1) Write Clock and NRZ Input Data

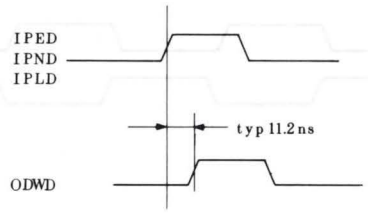


2) MFM Data



*Early, Normal, Late – Same with Clock Bit

DWD Output 2 . . . . . Precompensation Mode at EXT



6. MAINTENANCE (Trouble-shooting)

6-1. Genral

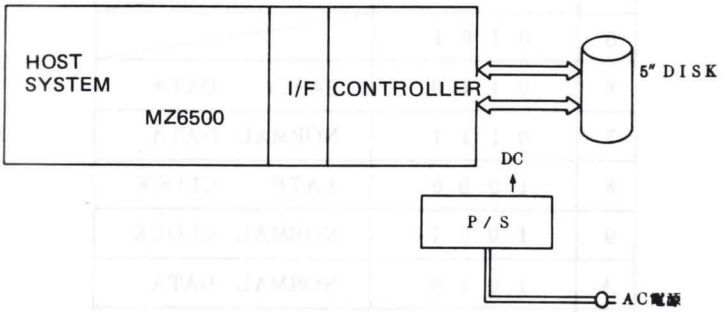
Trouble analysis of the NDC5801 Hard Disk Controller is described, sequence by sequence.

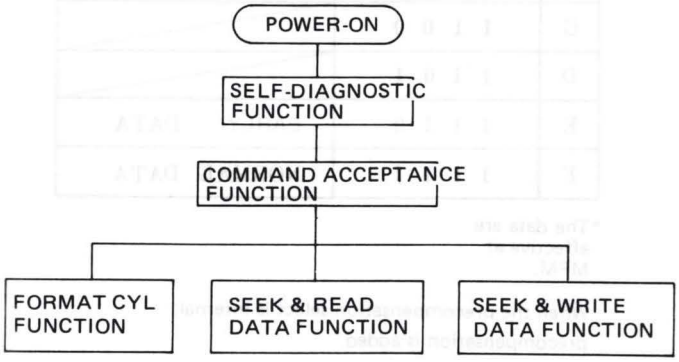
6-2. Tools

The tools necessary for trouble analysis are the following.

(1) Host system (MZ-6500)
(2) Troubled 5" Disk and NDC5801 controller
(3) Oscilloscope
(4) Test program

6-3. Structure





6-4-2. Self-Diagnostic Function

This function works with the power on. A judgement of good or bad is shown with the SELECT LAMP of the drive and the LED of this controller.

(1) SELECT LAMP

The normal action of this lamp after the power is furned on is to light in twenty seconds then immediately go off. Abnormal cases include the following.

- If the spindle motor of the dirve does not rotate, the drive is bad or the power system of the drive is bad.
- IIf the lamp does not light after the controller is exchanged, the drive or the cable between the dirve and controller is bad. If the lamp lights, the Drive Select of the controller is bad.

(2) LED

If the red LED remains lighted after the power is turned on, the Dirve Select of the controller is bad.

If the red LED finally lights though the green LED lighted up once, change the controller and recheck. After the exchange, if the green LED lights, this indicates that the controller is bad. If the status remains the same, then the drive or the periphery is bad.

6-4-3. Basic Operations of the Controller

To check if the self-diagnosis is executing normally after the controller is turned on or reset:

(1) If the red LED remains lighted after the power is on or reset.

① Confirm if the MPU Z-80 39PIN READ signal is output after eset.

② MPU Z-80 39PIN CLK is normal or 2.5MHz.

- 26LS31 (5F) is bad.
- 74LS74 (5C) is bad.
- NDC842 (7G) is bad.
- OSC (6G) is bad. 10MHz

③ Is the RESET signal at High?

- TL7700 (&B) and the peripheral circuit are bad.
- RESET from the host and the circuit are bad.
- NDC848 is bad.

(2) If the red LED remains lighted after the green LED lights with the power on or reset,

① Change the controller and reconfirm.

- If the green LED lights after the change, this indicates that the controller is bad.
- If the status remains the same, then the drive or the periphery is bad.

6-4-4. Operation Check with the Self-Diagnostic Switch

(1) Read Test

- RD (SW3) switch is ON.
- ST (SW1) switch is ON.

① If the NG lamp does not light unitl 15 minutes after the switch is on,

- It can be judged that the Read system is normal.

② The NG lamp lights:

a) Confirm NDC847 (8G) Pin 2, 13–5V.

- TL497 (8B) is bad.
- Peripheral circuit of TL497 is bad.

b) Confirm NDC847 (8G) Pin 8+0.5V±2.0V

- NDC847 is bad.

c) Confirm the REad data from the disk.

- NDC842 (7G) is bad.
- NDC840 (4E) is bad.
- NDC846 (4G) is bad.
- 74LS123 (8H) is bad.
- 26LS32 (5E) is bad.
- NDC847 (8G) is bad.

d) 74LS123 (8H) Pin 12:

- Confirm Low level at 260ns÷30ns.

(2) Write Test

- RW (SW4) switch is ON.
- ST (SW1) switch is ON.

① If the NG lamp does not light until 15 minutes after the switch is on,

- It can be judged that both the Read and Write systems are normal.

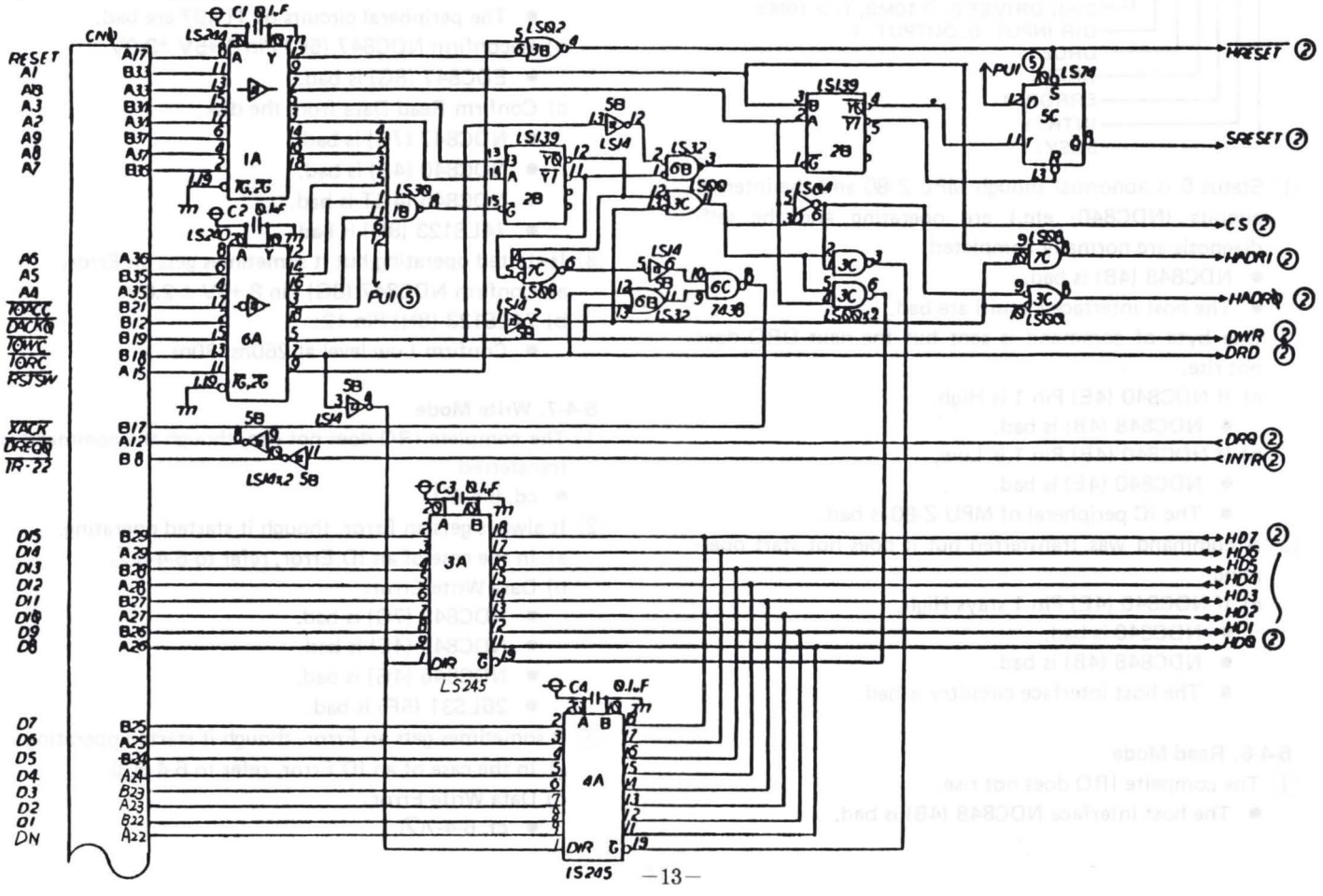
② The NG lamp lights:

a) If the Read system is normal, it can be judged that the Write system is abnormal.

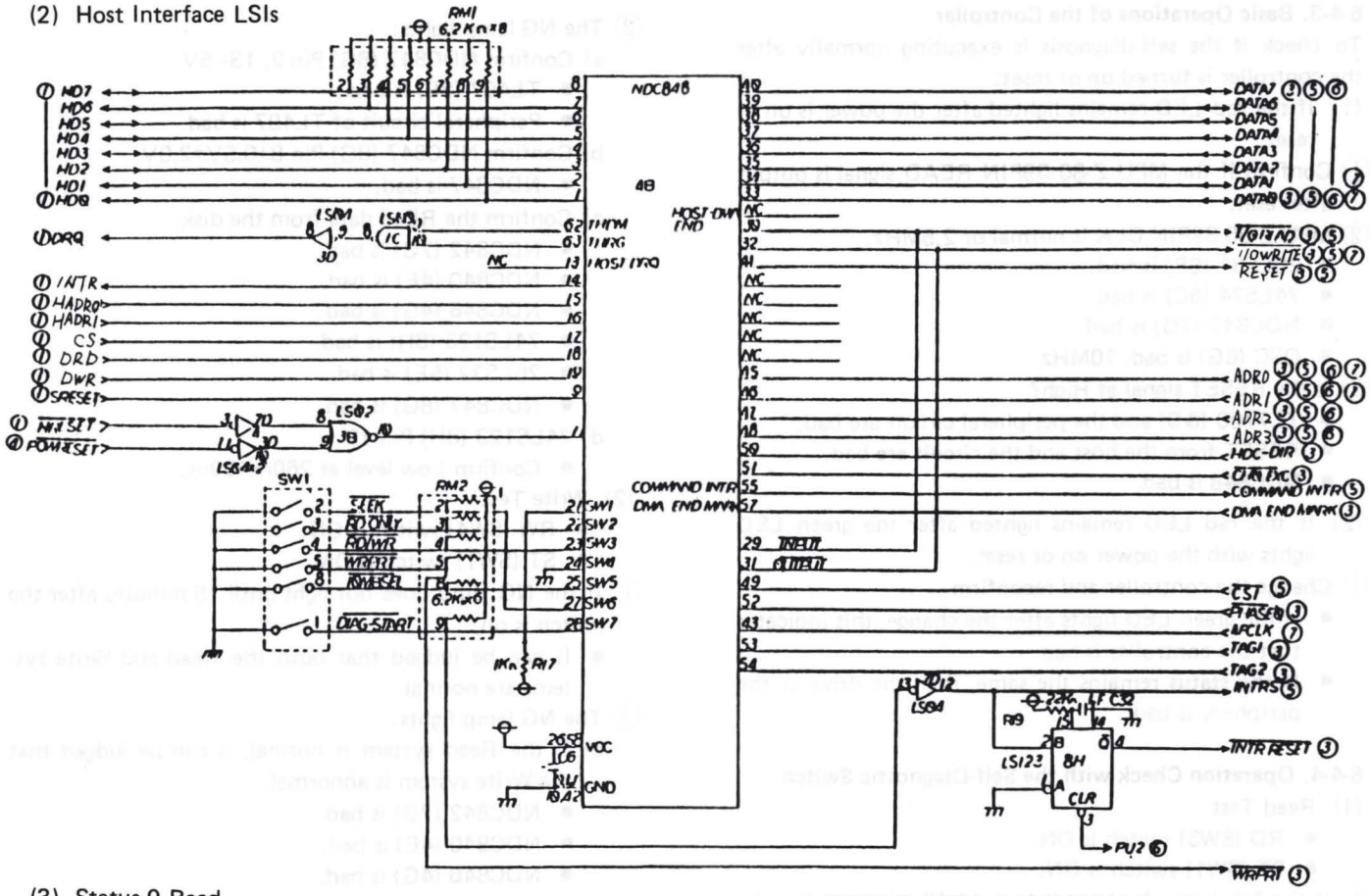
- NDC842 (7G) is bad.
- NDC840 (4E) is bad.
- NDC846 (4G) is bad.
- 74LS38 (6C) is bad.
- 26LS31 (5F) is bad.

6-4-5. Impossibility of Command Acceptance

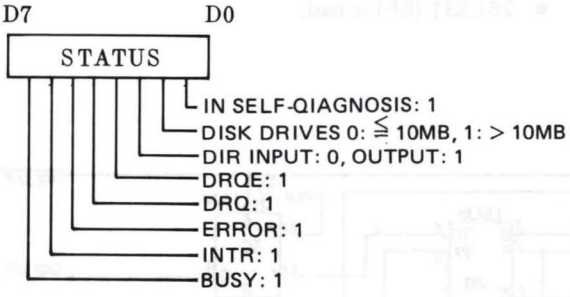
(1) Host Interface Circuits



(2) Host Interface LSIs



(3) Status 0 Read



① Status 0 is abnormal though MPL Z-80 and the internal circuits (NDC840- etc.) are operating and the self-diagnosis are normally completed.
- NDC848 (4B) is bad.
- The host interface circuiti are bad.

② One byte of command is sent but the next DRQ does not rise.
a) If NDC840 (4E) Pin 1 is High,
- NDC848 (4B) is bad.

b) If NDC840 (4B) Pin 1 is Low,
- NDC840 (4E) is bad.
- The IC peripheral of MPU Z-80 is bad.

③ A command was transferred but it does not start operating.
a) If NDC840 (4E) Pin 1 stays High,
- NDC840 is bad.
- NDC848 (4B) is bad.
- The host interface circuitry is bad.

6-4-6. Read Mode

① The compelte IRQ does not rise.
- The host interface NDC848 (4B) is bad.
- NDC840 (4E) is bad (DMA).

② It started operating but it always gets an Error.
Reconfirm Itesm:
a) Recoefirm NDC847 (8G) Pin 2, 13–5V.
- TL497 (8B) is bad.
- The peripheral circuits of TL497 are bad.

b) Reconfirm NDC847 (5G) Pin 8 +5V ±2.0V.
- EDC847 (8G) is bad.

c) Confirm Read Data from the disk.
- NDC847 (7G) is bad.
- NDC840 (4E) is bad.
- NDC846 (4GT is bad.
- 74LS123 (8H) is bad.

③ It started operating but it sometimes gets an Error.
a) Confirm NDC847 (8G) Pin 8 +5V ± 2.0V.
b) 74LS123 (8H) Pin 12:
- Confirm Low level at 260ns±30ns.

6-4-7. Write Mode

① The complete IRQ does not rise, though the command is transferred.
- cd. 6-4-6①

② It always gets an Error, though it started operating.
a) In the case of an ID Error, refer to 6-4-6②
b) Data Write Error:
- NDC842 (7G) is bad.
- NDC840 (4E) is bad.
- NDC846 (4G) is bad.
- 26LS31 (5F) is bad.

③ It sometimes gets an Error, though it started operating.
a) In the case of an ID Error, refer to 6-4-6③
b) Data Write Error:
- cf. 6-4-7②

7. EXPLANATION OF LSI

7-1. NDC840

1) GENERAL

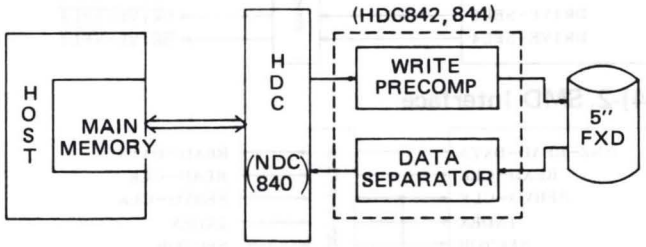
NDC840 is a highly integrated one-chip Hard Disk Controller (HDC). This high-speed controller uses a dual buffer. A DMA controller is built in HDC.

FEATURES

- Transfer Rate between HDC and a Hard Disk Drive (HDD) — 20 Mbits/s
- Buffer — Dual buffer available
- DMA — DMA controller in HDC
- Transfer Rate between Host and HDC — DMA dual = 2.3MB/s (max)
- Data check, Correction — CRC or ECC (11 bit burst correction)
- Drive I/F — SMD I/F or Floppy I/F
- Data Bus — 8-bit timign signal bidirection
- Dynamic Memory — Refresh timing signal bidirection
- Power Supply — +5VDC

2) APPLICATIONS

2)-1. Main Memory Direct Transfer



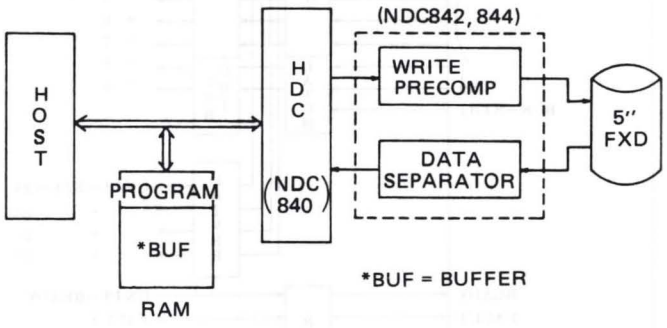
Main Memory

When a Main-Memory cycle time can follow up a disk transfer rate, data can be transferred directly into the Main Memory.

(1) Main-Memory cycle time (Byte Transfer)

$$\frac{10^6}{\text{Disk Transfer Rate (bit/s)}} \times 8 \text{ Memory Cycle Time } (\mu s)$$

2)-2. Single-Buffer Transfer



(1) RAM

HDC PROGRAM area

BUF: 1 SECTOR or 1 TRACK BUF

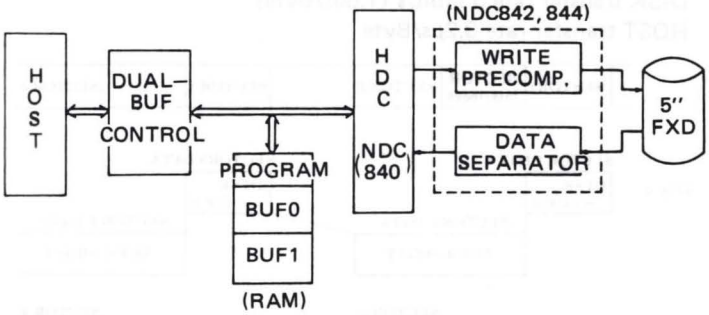
(2) HOST, BUF Transfer Rate

When data are transferred between the 5" FXD and host, data shall be accomdated temporarily in a buffer register. Transfers can be executed at any transfer rate.

(3) BUF area

A buffer area can be allocated as one area of Main Memory.

2)-3. DUAL-BUF Transfer



(1) RAM

HDC PROGRAM area

BUF 0, BUF 1 area

Either BUF is a 1 SECTOR BUF.

2KB/CHIP RAM – maximum SECTOR length = 512 Bytes

A buffer transfers data in time-sharing.

(2) HOST, BUF Transfer Rate

When data are transferred between the 5" FXD and host, data shall be accomodated temporarily in a buffer register. Transfers can be executed at any transfer rate.

In multisectors, transfer rates of the host and buffer determine sector interleaves.

3) TRANSFER MODES

3)-1. Single Buffer

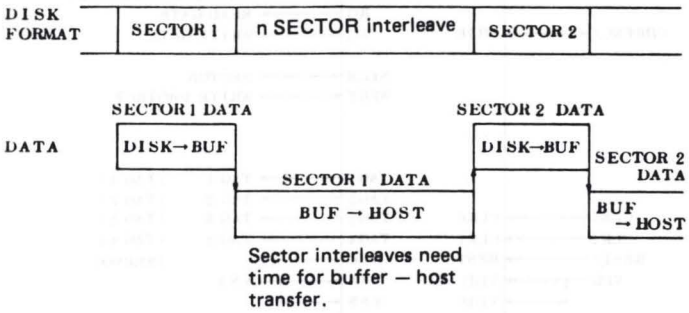
DMA shall be transferred regardless of the disk transfer rate.

The hardware of the host shall become Japanese.

Host cycle-steal and prior interruption.

In a multi-sector mode, process efficiency decreases.

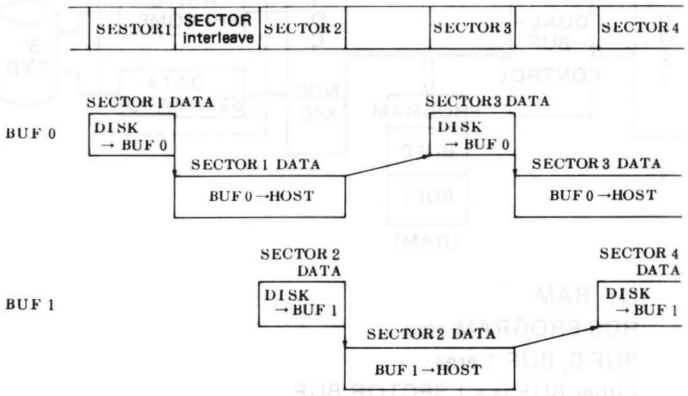
(e.g.) READ DATA (DISK → HOST)



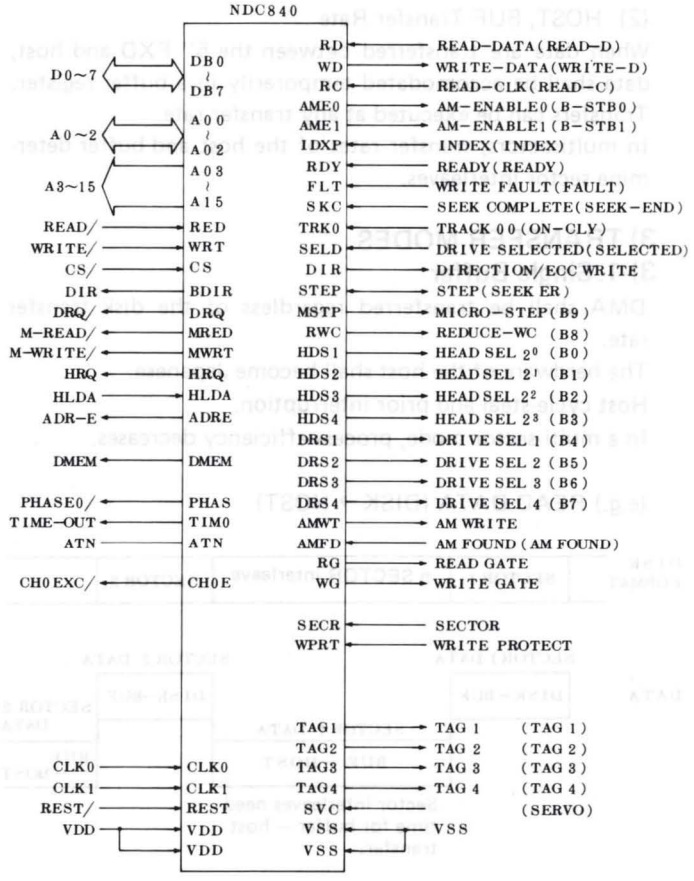
3)-2. Dual Buffer

DMA shall be transferred regardless of the disk transfer rate.
The hardware of the host shall become Japanese.
Host cycle-steal and prior interruption.
In a multi-sector mode, process efficiency decreases.

(e.g.) READ DATA (DISK → HOST)
DISK transfer rate 5 Mbit/s (1.6us/Byte)
HOST transfer rate 3.2μs/Byte

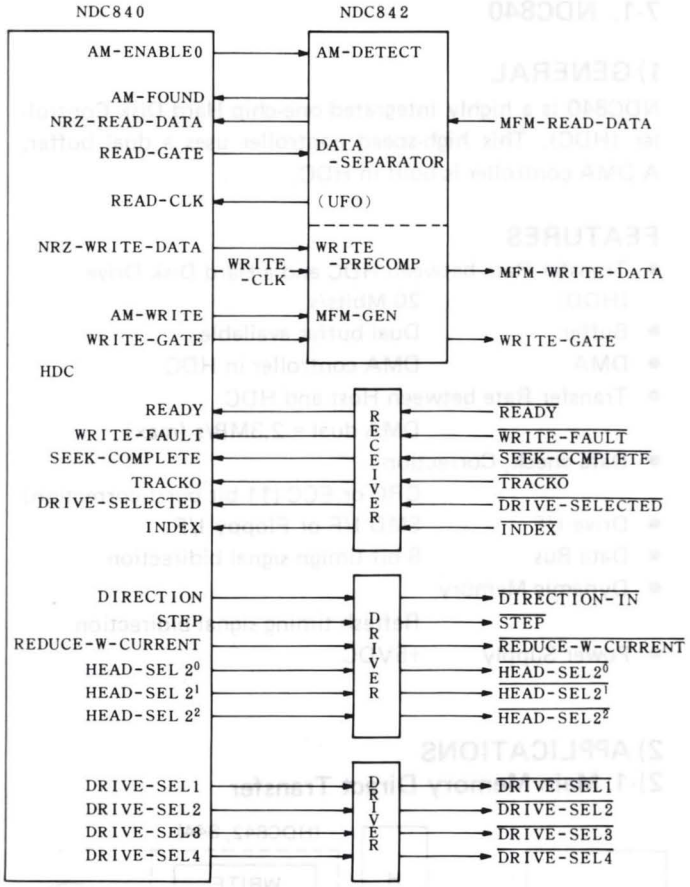


4) INTERFACE SINGNALS

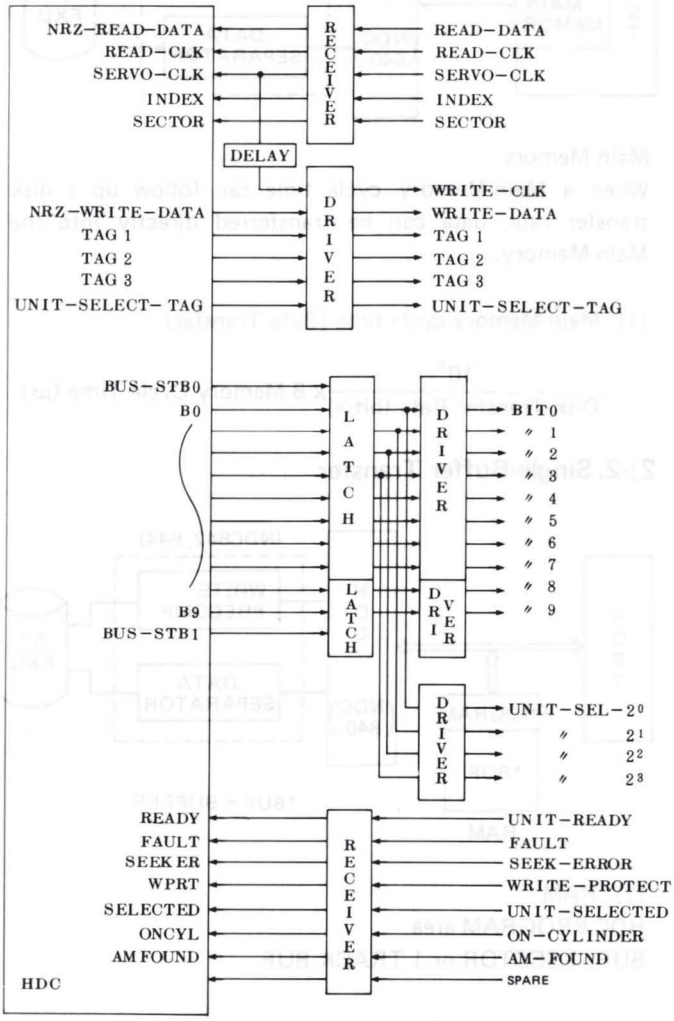


* Signals in parentheses are used for SMD I/F.

4)-1. Floppy Interface



4)-2. SMD Interface



5) DESCRIPTION OF SIGNALS

5)-1. Host I/F Signals

(1) DATA-BUS (D0 ~ D7)
8-bit bidirectional data bus is in a tristate.
Data are transferred between CPU and the host.

(2) $\overline{\text{READ}}$
This active low signal is used to take parameters such as data, status, DMA address, BYTE counter and mode from HDC.

(3) $\overline{\text{WRITE}}$
This active low signal is used to load parameters such as data, DMA address, BYTE counter and mode.

(4) $\overline{\text{CS}}$ (CHIP SELECT)
This is low signal which makes READ/WRITE of HDC parameters and STATUS READ effective and directs ADR0 ~ ADR2 from CPU to HDC.

(5) DIR (DIRECTION)
It indicates data-bus directions.
"H": HDC (DISK or BUF) → HOST
"L": HDC (DISK or BUF) ← HOST
When DMA channel 0 is in execution, this signals is output by the READ/WRITE modes as follows:
READ mode : HDC → HOST
WRITE mode : HDC ← HOST
When DMA is not being executed the direction is HDC ← HOST.

(6) DATA-REQ
When DMA channel 0 is excuted, this output signal requests the host for data. By this signal, the host activates I/O mode and the DMA controller of CPU. When DMA signal 0 is designated to the I/O mode, this signal makes a handshake with the Read and Write signals.

(7) ADR0 ~ ADR2
ADR0 ~ ADR2 are bidirectional. Unless DMA is executed, these bits address internal registers. In DMA execution, these three bits are tristate signals which output three lower bits of the 16-bits memory address.

(8) ADR3 ~ ADR15
This signal outputs 13 bits from the 2nd to the 7th bit of Memory Address generated by HDC in DMA execution.

(9) $\overline{\text{M-READ}}$ (MEMORY-READ)
This active low tristate output is used to read data from an addressed memory in the DMA read-cycle. When a DMA channel is designated the to the I/O mode, this signal is output handshaking with READ or WRITE. This signal is also used as a program load timing in format programming.

(10) $\overline{\text{M-WRITE}}$ (MEMORY-WRITE)
This active low tristate output is used to write data into an addressed memory in the DMA write cycle. When a DMA channel is designated to the I/O mode, this signal is output by handshaking with READ or WRITE.

(11) ADRE
This indicates that HDC is executing DMA and reading commands and that the addresses from HDC are effective.

(12) HRQ
This is an output signal which requests a control over a system bus.

(13) HLDA
This signal answers to HRQ and indicates that HDC has a control over a system bus.

(14) $\overline{\text{PHASE 0}}$
This indicates a $\overline{\text{DMA}}$ transfer mode.
ADRE = H PHASE 0 = L
HOST ↔ DISK
HOST ↔ MEMORY (BUF) } DMA MODE REG.

ADRE = H $\overline{\text{PHASE 0}}$ = L
MEMORY (BUF) ⟷ DISK: DMA MODE REG.

(15) DMEM
This signal turns "H" with a DMA channel termination and turns "L" by a INTER reset command.

(16) CLK 0, 1 (CLOCK 0, 1)
This is a clock input signal to make an internal timing in HDC.
CLK 0 = DMA CONTROLLER CLOCK
CLK 1 = DISK CONTROLLER CLOCK

(17) $\overline{\text{RESET}}$
This is a synchronized input used to clear an internal register and control line.

(18) ATN
This stops READ/WRITE. READ/WRITE operations continue until a write gate turns off.

5)-2. SMD Interface

5)-2-1. Unidirectional Signals

(1) NRZ-READ-DATA
This signal is the data of NRZ.

(2) READ-CLK
Synchronized with Read-Data, this signal is output from a disk drive when reading.

(3) SERVO-CLK
This signal is phase-locked to the data recorded on a servo-track, and is always the output from a disk drive.

(4) INDEX
A pulse generated once in a revolution which indicates the start of a track.

(5) SECTOR
This is a signal used to get a sector timing when reading data.

(6) NRZ-WRITE-DATA
Synchronized with Write Clock, these NRZ data are output to a disk drive.

(7) TAG 1 (CYLINDER SELECT)
This is a strobe signal to select a cylinder address on bus bit 0 ~ 9. A disk drive seeks for a cylinder address on a bus strobed by TAG 1.

(8) TAG 2 (HEAD SELECT)
This signal selects a head by designating bus bit 0 ~ 2.

(9) TAG 3 (CONTROL SELECT)
When this signal is gated, the following operations are enabled.

a) WRITE GATE (BIT 0)
This signal enables a Write operation.

b) READ GATE (BIT 1)
This signal enables a Read operation.

c) SERVO OFFSET PLUS (BIT 2)
When this signal is active, it makes an inner offset of head from a normal on-track position.

d) SERVO OFFSET MINUS (BIT 3)
When this signal is active, it makes an outer offset of head from a normal on-track position.

e) FAULT CLEAR (BIT 4)
This clears a fault status of a selected drive.

f) AM ENABLE (BIT 5)
- Write
  When this signal is active in an active Write Gate, a DC erase area is written by synchronizing with this signal.
- Read
  When this signal is active in an active Read Gate, an Address Mark Found signal is output after an Address Mark has been detected.

g) RTZ (BIT 6)
This signal moves a head to Cylinder "0", Head "0".

h) DATA STROBE EARLY (BIT 7)
When this signal is active, data of the PLO Data Separator in a disk drive are strobed earlier.

i) DATA STROBE LATE (BIT 8)
When this signal is active, data of the PLO Data Separator in a disk drive are the strobed late.

(10) UNIT-SELECT-TAG
This is a drive-select gate signal and samples Unit-Sel $2^0 \sim 2^3$.

5)-2-2. Bidirectional Signals

5)-2-2-1. Output Signals
B0 ~ B9 are latched in an outer latch area and used as bus bit 0 ~ 9 or Unit-Sel $2^0 \sim 2^3$)

(1) UNIT-SEL $2^0 \sim 2^3$ (UNIT-SELECT $2^0 \sim 2^3$)
This is a signal used to select a drive unit and sampled by Unit-Select-Tag.

(2) BUS-BIT 0 ~ 9
This signal has different meanings depending on the selection of TAG 1 ~ 3.

BUS	TAG1 (CYLINDER SELECT)	TAG2 (HEAD SELECT)	TAG3 (CONTROL SELECT)
BIT0	1	1	WRITE GATE
1	2	2	READ GATE
2	4	4	SERVO OFFSET PLUS
3	8	8	SERVO OFFSET MINUS
4	16	8	FAULT CLEAR
5	32		AM ENABLE
6	64		RTZ
7	128		DATA STROBE EARLY
8	256		DATA STROBE LATE
9	512		

5)-2-2-2. Input Signals

(1) UNIT-READY
This indicates that disks reach a rated revolution and heads are on a recording zone. When a drive is in fault, this signal shall be inhibited.

(2) FAULT
This indicates that a selected drive is in fault.

(3) SEEK-ERROR
This indicates that a seek error is found.

(4) WRITE-PROTECT
This indicates that a write-circuit of a disk drive is in a status of Write Protect.

(5) UNIT-SELECTED
This indicates that a drive designated by Unit-Select $2^0 \sim 2^3$ and Unit-Select-Tag is selected.

(6) ON-CYLINDER
This indicates that the heads are positioned on the tracks.

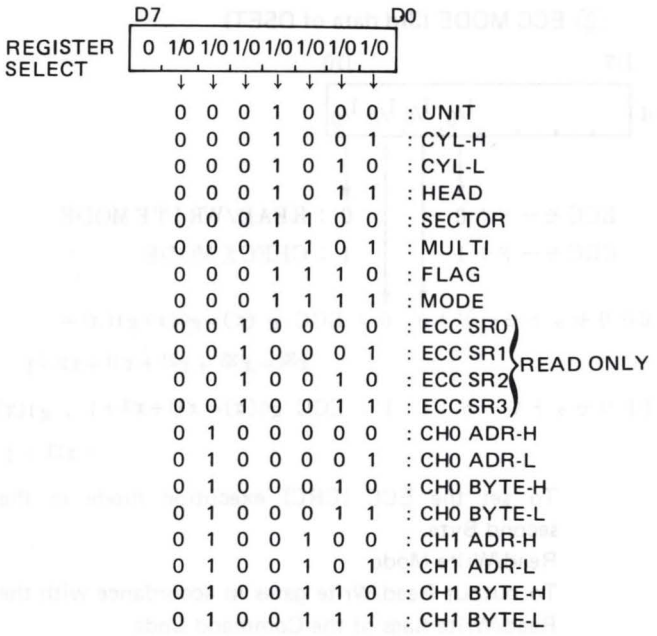
(7) AM-FOUND (ADDRESS MARK FOUND)
AM FOUND is output when Read Gate and AM Enable are active, and a disk drive detects Address Mark.

6) HDS STATUS AND REGISTER

HDC Statsu and Register are shown below:

CS	ADR 2	ADR 1	ADR 0	READ	WRITE
1	0	0	0	INTR STATUS	RW/SEEK START
1	0	0	1	READ/WRITE ERROR STATUS	INTR RESET
1	0	1	0	DISK STATUS	DMA START
1	0	1	1	———	REGISTER SELECT
1	1	0	0	REGISTER READ	REGISTER WRITE
1	1	0	1	PC-H	PC-H
1	1	1	1	———	FPU RESET
0	X	X	X	DMA TRANSFER	DMA TRANSFER

The Read/Write Status and Register shall not be executed during an HDC operation. However Read is enabled in a Zero Search Command execution. To Read/Write, each register shall be executed by designating a register at Resigter Select.



(1) INTR STATUS

This indicates the result at the completion of Seek and Read/Write operations.

NO.	BIT STATUS	Description
D7	READY	HDC is ready.
D6	COMMAND INTR	INTR 0 signal. Interruption generated by the HDC command.
D5	END INTR	INTR signal to indicate a completion.
D4	SEEK END	This indicates an interruption by a seek completion.
D3	READ/WRITE END	This indicates an interruption of the Read/Write completion.
D2	ERROR	HDC operation ends up in Error.
D1	NOT READY	Device is not ready.
D0	DEVICE CHECK	This indicates reception of a fault signal. In a floppy drive, this indicates that it was not able to detect Track 0 within a specified time after Restore.

(2) ERROR STATUS

In a Read/Write execution, any error are shown in Error Status.

NO.	BIT STATUS	Description
D7	LOST DATA	Transfer rates of CPU and HDC cannot follow a disk drive and HDC.
D6	CRC ERROR	CRC or ECC Error is found.
D5	RECORD NOT FOUND	ID is not found.
D4	–	–
D3	DRIVE CHECK	Receives a fault signal from a drive.
D2	NOT READY	A drive is not ready.
D1	COMMAND ERROR	Read Flag and Write Flag are set at a time.
D0	FLAG ERROR	The Flag byte of ID is cncountered.

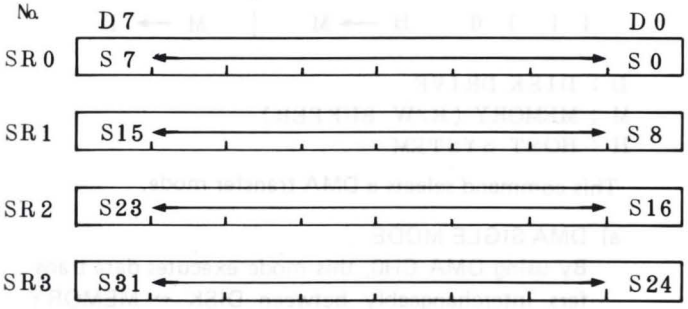
(3) DISK STATUS

Disk Status shows a signal received from a disk drive.

BIT NO.	SMD I/F	FLOPPY TYPE I/F
D7	UNIT READY	READY
D6	UNIT SELECTED	DRIVE SELECTED
D5	WRITE PROTECTED	0
D4	FAULT	WRITE FAULT
D3	SEEK END	SEEK COMPLETE
D2	ON CYLINDER	TRACK 00
D1	SEEK ERROR	IDAM FOUND
D0	(AM FOUND)	DATA AM FOUND

(4) ECC SYNDROME REGISTER (32 BIT)

The following data can be read in accordance with Syndrome Register No. (SR0 ~ 3).



(5) SECTOR (8 BIT)

Accomodation register – Sector No. in Read/Write.

(6) CYLINDER – H, L (12 BIT)

Accommodation register – Cylinder No. in Read/Write/Seek execution.

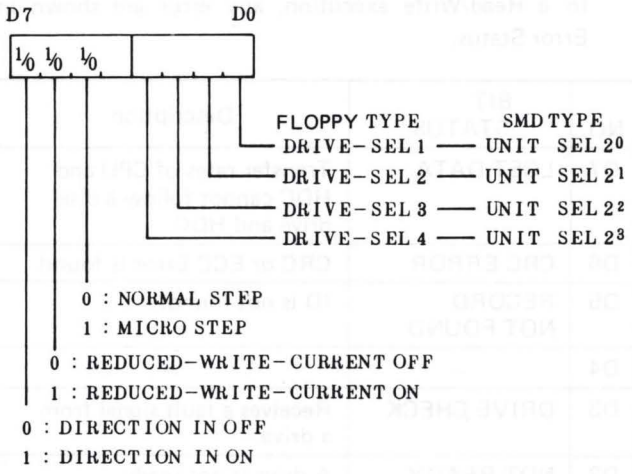
SMD I/F : SEEK CYLINDER

FLOPPY TYPE I/F : STEP (0001) H ~ (0FFF) H

(7) HEAD (8 BIT)

Accommodation register – Head No. in Read/Write.

(8) UNIT (8 BIT)



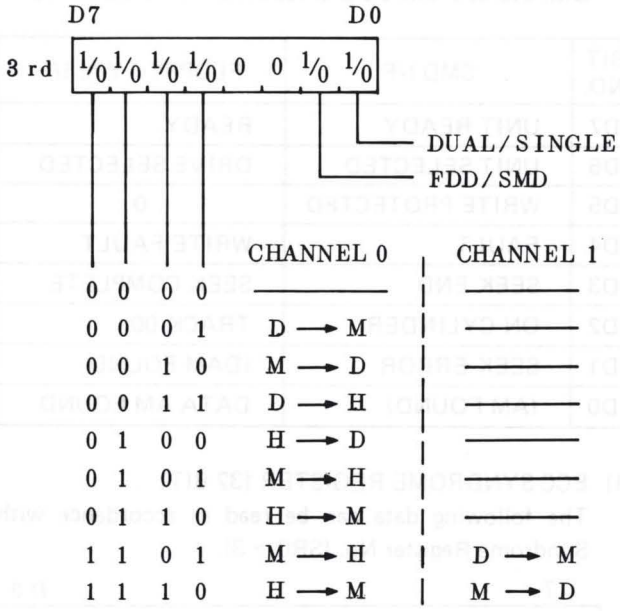
(9) FLAG (8 BIT)

A register to accomodata a flag content allocated in ID used to check ID.

(10) MODE

① DMA MODE (3rd data of DSET and data of DMA mode set)

To select an HDC execution mode



	CHANNEL 0	CHANNEL 1
0 0 0 0	———	———
0 0 0 1	D → M	———
0 0 1 0	M → D	———
0 0 1 1	D → H	———
0 1 0 0	H → D	———
0 1 0 1	M → H	———
0 1 1 0	H → M	———
1 1 0 1	M → H	D → M
1 1 1 0	H → M	M → D

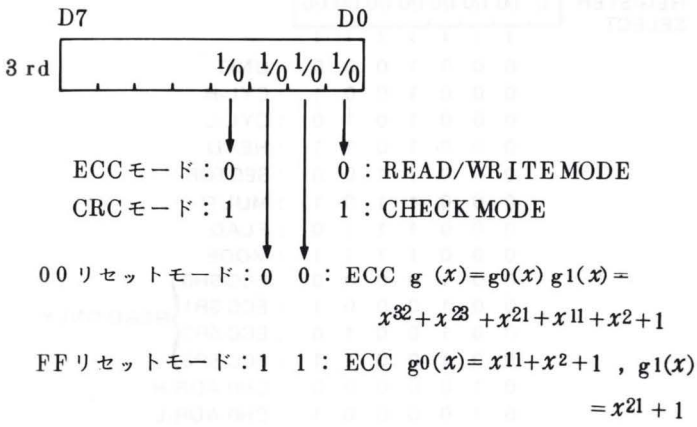
D : DISK DRIVE
M : MEMORY (R/W BUFFER)
H : HOST SYSTEM

This command selects a DMA transfer mode.

a) DMA SIGLE MODE
By using DMA CH0, this mode executes data transfers interchangeably between DISK ↔ MEMORY and MEMORY ↔ HOST.

b) DMA DUAL MODE
Parallel processing: CH 0 for HOST ↔ MEMORY
CH 1 for DISK ↔ MEMORY

② ECC MODE (3rd data of DSET)



To set the ECC (CRC) execution mode in the second Byte.
Read/Write Mode
To output Read/Write gates in accordance with the Read/Write flags of the Command Code.
Check Mode
To not output Read/Write gates by ignoring the Read/Write flags of the Command Code.

(11) CH0 ADR (16 BIT)

ADR REG. of DMA CH 0 in H.L. 16 bits.

(12) CH0 BYTE (16 BIT)

H.L. 16-bit Regster to indicate and select a number of transfer bytes of DMA CH 0. (Sets 2 complements)

(13) CH1 ADR (16 BIT)

ADR REG. of DMA CH1 1 in H.L. 16 bits.

(14) CH1 BYTE (12 BIT)

H.L. 12-bits Register to indicate and select a number of transfer bytes of DMA CH1. (Sets 2 complements)

(15) SEEK/RW START

Starts HDC and excutes an HDC micro-program in a specified program counter (PC).

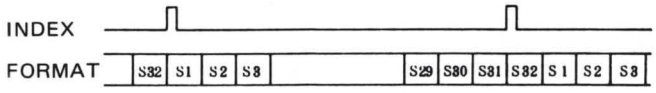
(16) PC H.L (16 BIT)

16-bit program counter for an HDC micro-program. Program to be executed shall be ready in an outer memory before execution. (Program-execution area: 4KB/page, within a page)

(17) MULTI SECTOR (8 BIT)

Selects a sector number to be excuted by a RW START command, a selectable area shall be on the same track. If selected on tracks of more than two, RECORD NOT FOUND comes up. Sectors selected by Multi Sector Reg. shall be executed with the initial sector selected by sector Reg.

(e.g.)



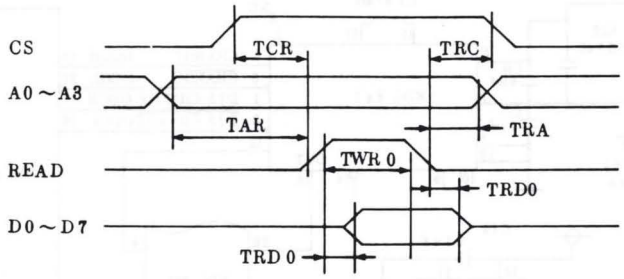
a) Executable
SECTOR REG. : 29
MULTI SECTOR : 4

b) Record Not Found Error
SECTOR REG. : 29
MULTI SECTOR : 5

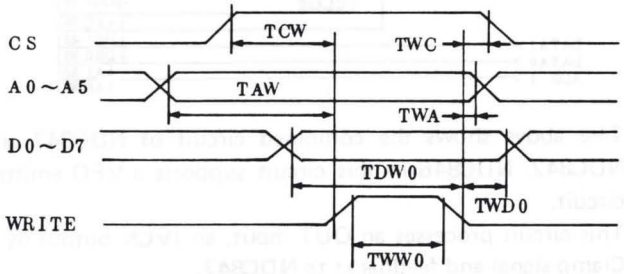
7) TIMING CONDITIONS

7)-1. HOST I/F

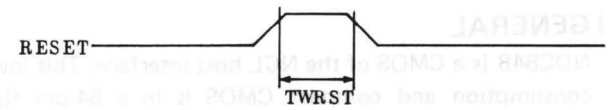
(1) Status, Register Read



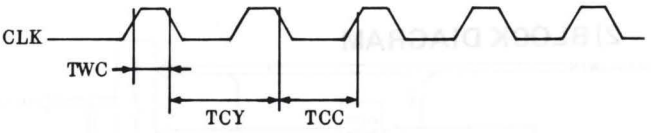
(2) Parameter, Register Write



(3) RESET

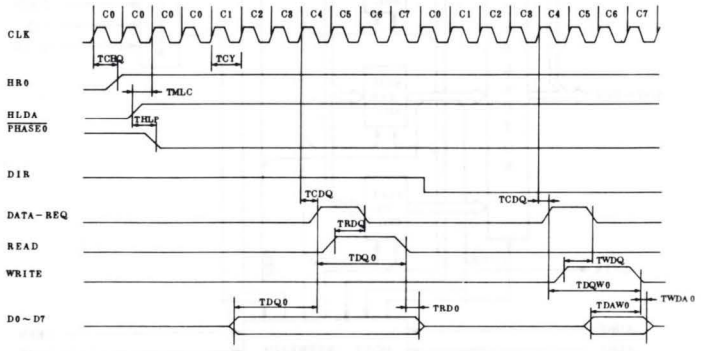


(4) CLK

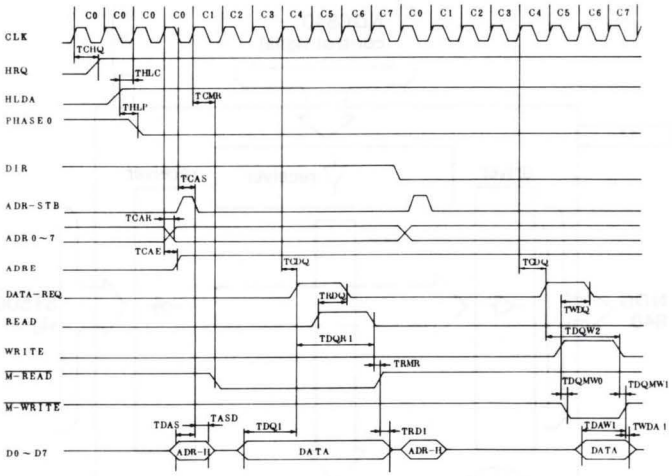


(5) DMA Transfer

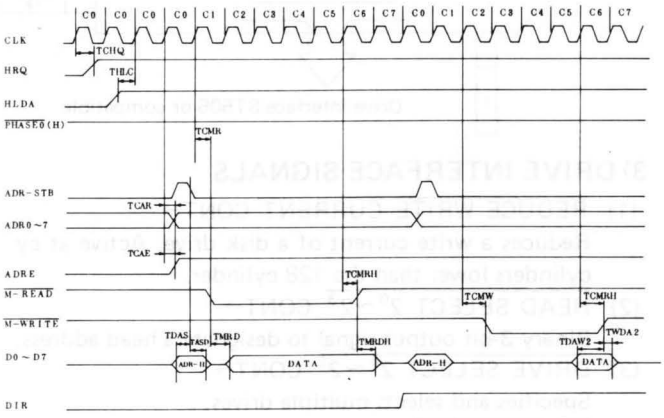
a) SINGLE MODE, DISK←→HOST



b) SINGLE MEMORY (BUF)←→HOST



c) SINGLE MEMORY (BUF)←→DISK



7)-2. NDC846

1) GENERAL

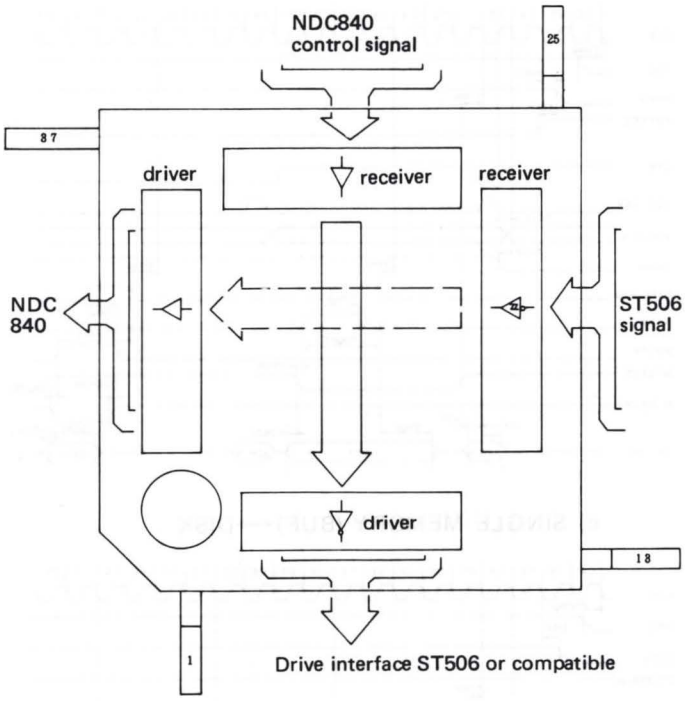
NDC846 is a hard disk drive interface for ST506 or compatible.

2) PIN ASSIGNMENTS AND POSITIONS

(1) Pin Assignments

Pin No.	I/O	Pin NAME	Pin No.	I/O	Pin NAME	Pin No.	I/O	Pin NAME	Pin No.	I/O	Pin NAME
1	O	INDEX	13	O	$\overline{DS-2}$	25	I	$\overline{INDEX}$	37	I	DS-2
2	O	VCO CLK	14	O	$\overline{DIR\ IN}$	26	I	$\overline{CLMP}$	38	I	DIR
3		NC	15	O	$\overline{STEP}$	27		NC	39	I	STEP
4	O	$\overline{VC1}$	16	O	$\overline{MSTP}$	28	I	VC1	40	I	$\overline{MSTP}$
5	O	$\overline{F1}$	17	O	$\overline{W-GT}$	29	I	F1	41	I	W-GT
6	O	$\overline{RWC}$	18	O	$\overline{HS-2-3}$	30	I	RWC	42	I	HS-2-3
7		VCC	19		GND	31		VCC	43		GND
8	O	$\overline{HS-2-0}$	20	I	$\overline{D-SEL}$	32	I	HS-2-0	44	O	D-SEL
9	O	$\overline{HS-2-1}$	21	I	$\overline{SKCMP}$	33	I	HS-2-1	45	O	SKCMP
10	O	$\overline{HS-2-2}$	22	I	$\overline{TRK00}$	34	I	HS-2-2	46	O	TRK00
11		NC	23	I	$\overline{W-FLT}$	35		NC	47	O	W-FLT
12	O	$\overline{DS-1}$	24	I	$\overline{RDY}$	36	I	DS-1	48	O	RDY

BLOCK DIAGRAM



3) DRIVE INTERFACE SIGNALS

(1) $\overline{\text{REDUCE WRITE CURRENT}}$ CONT→
Reduces a write current of a disk drive. Active at cy cylinders lower than the 128 cylinder.

(2) $\overline{\text{HEAD SELECT}}$ $2^0 \sim 2^3$ CONT→
Binary 3-bit output signal to designate a head address.

(3) $\overline{\text{DRIVE SELECT}}$ $2^0 \sim 2^1$ CONT→
Specifies and selects multiple drives.

(4) $\overline{\text{DIRECTION IN}}$ CONT→
Designates a seek direction of a head. When low, the direction is inward. When high, the direction is outward.

(5) $\overline{\text{STEP}}$ CONT→
A pulse signal of a head seek --- one cylinder-per-pulse seek. A jumper plug on a board selects a normal mode seek or a buffer mode seek.

(6) $\overline{\text{MICRO STEP}}$ CONT→
Active low signal to designate a head movement.

(7) $\overline{\text{WRITE GATE}}$ CONT→
A drive-write control signal which enables a data write in active low.

(8) $\overline{\text{DRIVE SELECTED}}$ CONT←
An active low signal to indicate that a drive has been selected by DRIVE SELECT $2^0 \sim 2^1$.

(9) $\overline{\text{SEEK COMPLETE}}$ CONT←
When low, indicates a seek completion.

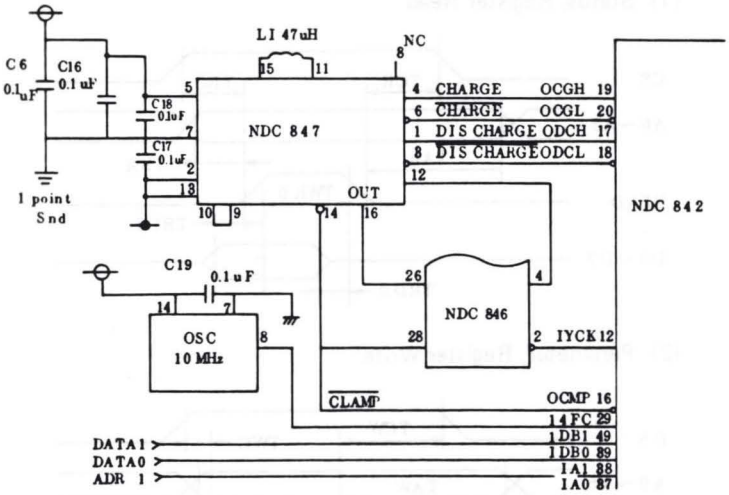
(10) $\overline{\text{TRACK 00}}$ CONT←
When low, indicates that a head is positioned at the outermost cylinder.

(11) $\overline{\text{WRITE FAULT}}$ CONT←
When low, indicates that a drive has an abnormality and Read/Write is not executed.

(12) $\overline{\text{READY}}$ CONT←
When low, indicates that a drive reaches a normal revolution.

(13) $\overline{\text{INDEX}}$ CONT←
A pulse per revolution indicates the start of a data track.

4) COMBINED CIRCUIT OF NDC847 AND NDC842



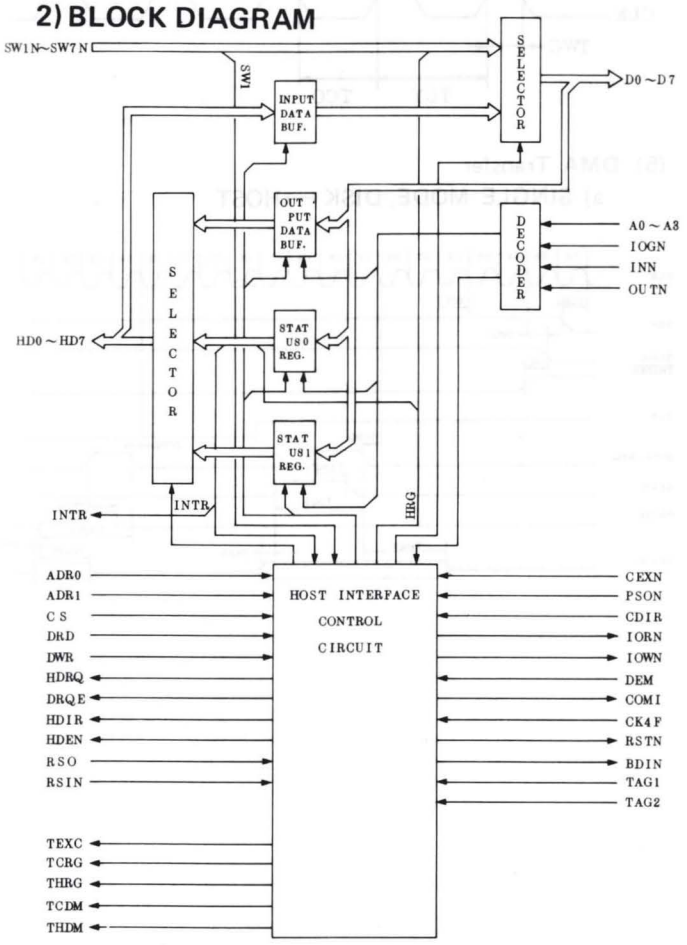
The above shows the combined circuit of NDC847 and NDC842. NDC846 in this circuit supports a VFO emitter circuit.
This circuit processes an OUT input, an IVCK output by a Clamp signal and feedbacks to NDC847.

7-3. NDC848

1) GENERAL

NDC848 is a CMOS of the NCL host interface. This low-consumption and compact CMOS is in a 64-pin flat package. This LSI can be directly connected to a hard disk controller (HDC840).

2) BLOCK DIAGRAM



注 HRG : Host Data Request Enable

3) PIN ASSIGNMENTS

3)-1. Host

(1) HD0–HD7 (Host Data Bus)
8-bit bidirectional data bus. Transfer lines of commands, status and Read/Write data.

(2) ADR0–ADR1 (Host Address)
Input pins to select a transfer register and buffer.

ADR1	ADR0	READ(DRD)	WRITE(DWR)
0	0	STATUS 0	
0	1	DATA	DATA
1	0	RESULT	
1	1	STATUS 1	COMMAND

(3) CS (Chip Select)
An input to enable a DRD input pin, DWR input pin, HDIR input pin, DRQE output pin and HDRQ output pin.

(4) DRD (Data Read)
Receives a strobe signal which puts status, and data of a Status Register and Output Data Buffer, into 8-bit bidirectional data bus HD0–HD7.

(5) DWR (Data Write)
Receives a host signal which sets data and commands on 8-bit bidirectional data bus HD0–HD7 into an input data buffer.

(6) HDRQ (Host Data Request)
When the Host DMA mode and Host Data Request Enable are set and CS is at an "H" level, this pin transmits an "H" level signal.

(7) DRQE (Data Request End)
When "H" is set at the fourth bit from LSB of Status 0 Register and CS is at an "H" level, this pin transmits an "H" level signal.

(8) HDIR (Host Direction)
When "H" is set at the third bit from LSB of Status 0 Register and the Host DMA mode is set at an "H" level of CS, this pin transmits and "H" level signal.

(9) INTR (Interrupt)
When "H" is set at the second bit from MSB of Status 0 Register, this pin transmits an "H" level signal.

(10) HDEN (Host DMA End*)
Transmits an "L" level signal, when Host DMA End is set.

(11) RS0 (Reset 0)
This schmidt trigger reset pin initializes an internal circuit and makes an RSTN pin transmit an "L" level signal.

(12) RS1N (Rest 1*)
This schmidt trigger reset pin initializes an internal circuit and makes an RSTN pin transmit an "L" level signal.

3)-2. HDC

(1) D0–D7 (Data Bus)
8-bit bidirectional data bus. Transfer lines of commands, status and Read/Write data.

(2) A0–A3 (Address)
Input pins to select a transfer register, buffer and mode.

A3	A2	A1	A0	INPUT (INN)	OUTPUT (OUTN)
0	0	0	0	Read Switch	
0	0	0	1		DMA Mode Set
0	0	1	0	Read Host Data	Status 1 Set
0	0	1	1		Host Data Request Set
0	1	0	0		HDC Data Request Set
0	1	0	1		Host DMA End Reset
0	1	1	0		HDC Data Set
0	1	1	1		Status 0 Set
1	0	0	0		Abort

(3) IOGN (IO Enable*)
An input pin to enable INN and OUTN input pins.

(4) INN (Input*)
Receives a strobe signal which transmits data of the Switch and Input Data Buffer to 8-bit bidirectional data bus D0–D7.

(5) OUTN (Output*)
Receives a strobe signal which sets data and status on 8-bit bidirectional data bus D0–D7 into an Output Data Buffer and Status Register. This pin also sets a mode and aborts.

(6) CEXN (Channel 0 Execution*)
Receives a strobe signal which transacts data between a Data Buffer and 8-bit bidirectional data bus D0–D7. This pin also transmits an "H" or "L" signal from IORN and IOWN pins.

(7) PSON (Phase 0*)
An input pin to enable a CEXN pin.

(8) CDIR (HDC Direction)
Designates a direction of data transfer. Used together with the CEXN and PSON pins.
CDIR "H" Output Data Buffer Data Bus D0–D7
CDIR "L" Input Data Buffer Data Bus D0–D7

(9) IORN (IO Read*)
Transmits an "L" level signal, when CDIR is "H" and Channel 0 Execution FF is set. Transmits an "H" level signal, when CDIR is "L". IORN is in a high impedance ("Z"), when Channel 0 Execution FF is reset.

(10) IOWN (IO Write*)
Transmits an "L" level signal, when CDIR is "L" and Channel 0 Execution FF is set. Transmits an "H" level signal, when CDIR is "H". IOWN is in a high impedance ("Z"), when Channel 0 Execution FF is set.

(11) DEM (DMA End Mark)
An input pin to enable Host DMA End.

(12) COMI (Command Interrupt)
Transmits an "H" level signal, when Input Data Buffer receives a command from 8-bit bidirectional data bus HD0–HD7.

(13) CK4F (4 Frequency Clock)
This 10 MHZ-clock input pin is used to complement a width of a Bus Direction signal.

(14) RSTN (Reset*)
Transmits an "L" level signal by receiving a reset signal from RS0 and RS1.

(15) BDIN (Bus Direction*)
Transmits an "L" level signal, when Status and Read data are transferred to 8-bit bidirectional data bus HD0–HD7.

(16) TAG1
An input pin to set Host Data Request Enable and reset Host DMA End.

(17) TAG2
An input pin to set HDC Data Request Enable and reset Host DMA End.

3)-3. Others

(1) SW1N–SW7N (Switch*)
An input pin for user's utility.

(2) TEXC (Test Channel 0 Execution)
This test output pin transmits an "H" level signal, when Channel 0 Execution FF is set.

(3) TCRG (Test HDC Data Request Enable)
This test output pin transmits an "H" level signal when HDC Data Request Enable is set.

(4) THRG (Test Host Data Request Enable)
This test output pin transmits an "H" level signal when Host Data Request Enable is set.

(5) TCDM (Test HDC DMA Mode)
This test output pin transmits an "H" level signal when HDC DMA Mode is set.

(6) THDM (Test Host DMA Mode)
This test output pin transmits an "H" level signal when Host DMA Mode is set.

(7) Vss (Ground)
A ground pin.

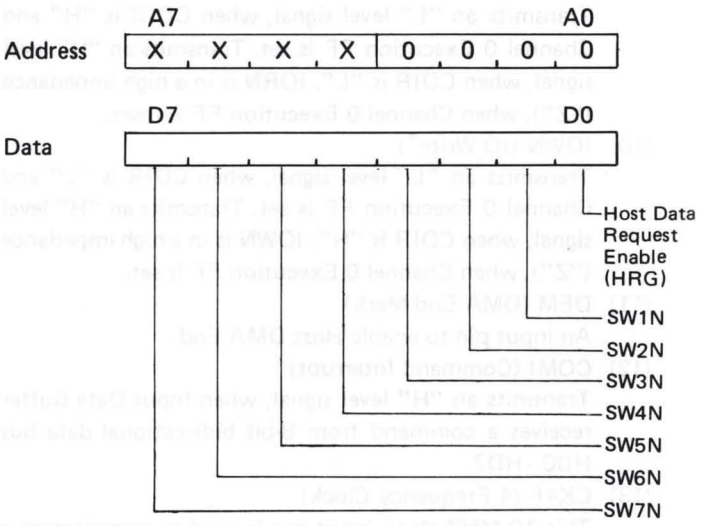
(8) VDD (Power Supply)
+5V power supply pin.

(9) N.C. (No Contact)
Not used.

4) HDC IO COMMANDS

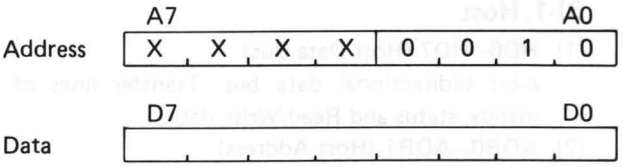
4)-1. Inputs

(1) Read Switch



When this command is executed, data of the Switch (SW1N–SW7N) and status of HRG are transferred to 8-bit bidirectional data bus D0–D7.

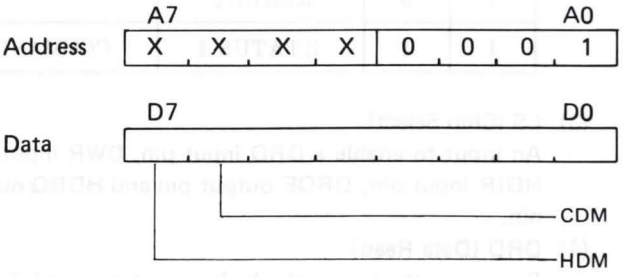
(2) Read Host Data



When this command is executed, data and commands of Input Data Buffer are transferred to 8-bit bidirectional data bus D0–D7.

4)-2. Outputs

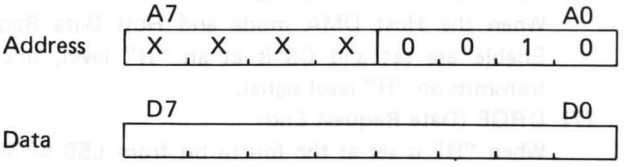
(1) DMA Mode Set



HDM1: Host DMA Mode
0: Host Program Mode
CDM1: HDC DMA Mode
0: HDC Program Mode

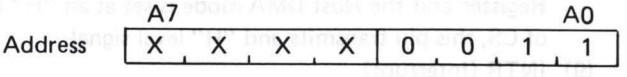
This command sets a DMA Program Mode. When HDM is 1 and SW1N is "L", a command cannot be received.

(2) Status 1 Set



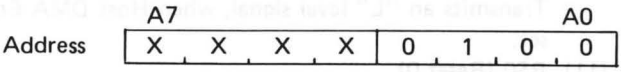
When this command is executed, status on 8-bit bidirectional data bus D0–D7 is set to Status 1 Register.

(3) Host Data Request Set



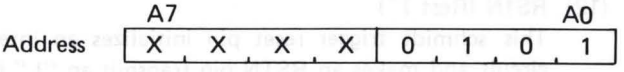
When this command is executed, Host Data Request Enable FF is set.

(4) HDC Data Request Set



When this command is executed, HDC Dat Request Enable FF is set.

(5) Host DMA End Reset



When tis command is executed, Host DMA End FF is set.

(6) HDC Data Set

	A7							A0
Address	X	X	X	X	0	1	1	0

	D7							D0
Data								

When this command is executed, data on 8-bit bidirectional data bus D0—D7 are set to Output Data Buffer.

(7) Status 0 Set

	A7							A0
Address	X	X	X	X	0	1	1	1

	D7							D0
Data								

When this command is executed, status on 8-bit bidirectional data bus D0—D7 is set to Status 0 Register.

(8) Abort

	A7							A0
Address	X	X	X	X	1	0	0	0

When this command is executed, the following Flip-Flops are reset:

* Channel 0 Execution
* HDC Data Request Enable
* Host Data Request Enable
* HDC DMA Mode
* Host DMA Mode
* Host DMA End
* Command Interrupt

7-4. NDC847

1) GENERAL

1)-1. Basic Concept

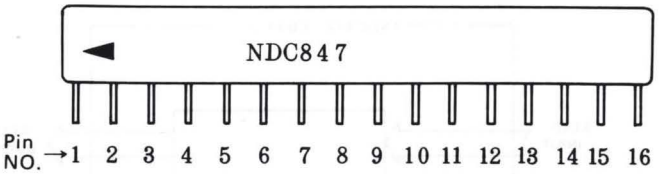
NDC847 is a hybrid IC of an analog PLL circuit.

1)-2. Features

(1) functions as data separator by being combined with NDC10-5 (MB113T119) or NDC842.
(2) has an internal linear circuit and receives a digital signal.
(3) compact and requires fewer parts in order to build circuit in comparison with a circuit using discrete parts.
(4) non-adjustable and reliable.
(5) functions as data transfer VCO of ST506, 5MBit/sec.
(6) 16-pin single-line IC and mountable as a regular IC.
(7) power supply: DC ±5V.

1)-3 Pin assignment

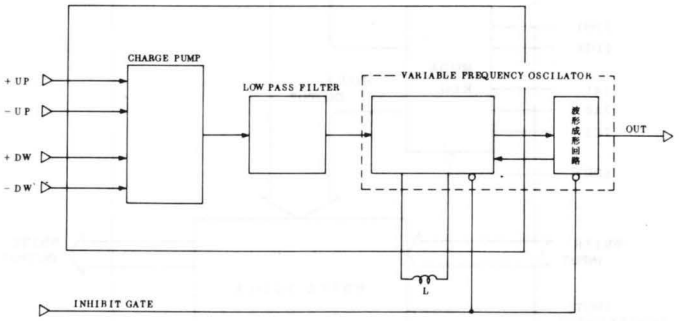
NO.	SYMBOL	NO.	SYMBOL
1	IN 3	9	KC0
2	VEE	10	K0 I
3	IN 4	11	L 2
4	IN 1	12	A
5	VCC	13	− B
6	IN 2	14	CMP
7	GND	15	L 1
8	T P	16	OUT



Single – 16pin, 2.54mm pitch

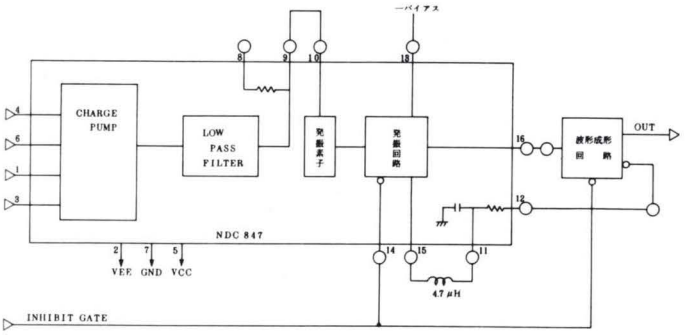
1)-4. Block Diagram

1)-4-1.



1. Basic Structure Diagram of NCL-type PLL Circuit

1)-4-2.



2. Structure of the connections of NDC847

2) OPERATIONS

NDC847 acts as a data separator for the ST506 Hard Disk Drive Interface by being combined with an NCL VFO data encoder/decoder.

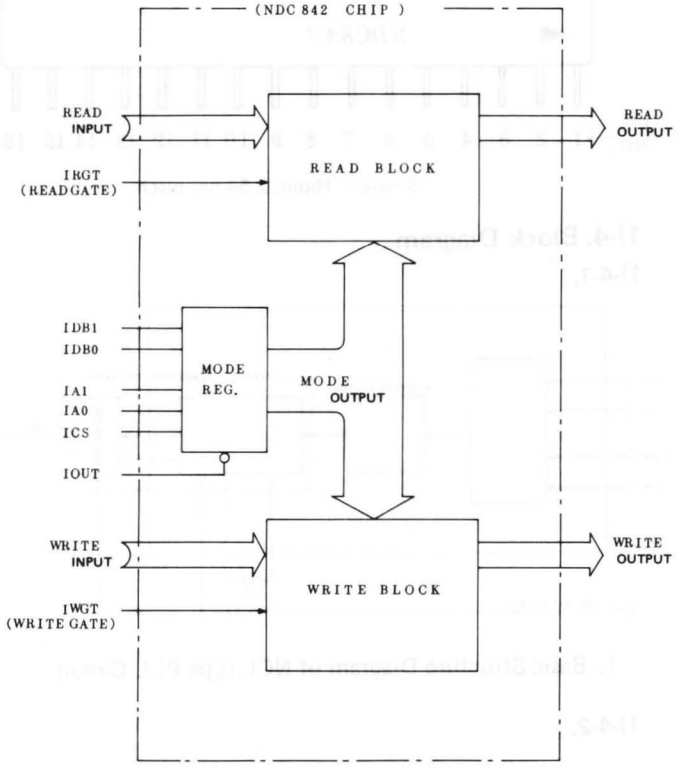
7-5. NDC842

1) PIN ASSIGNMENTS AND POSITIONS

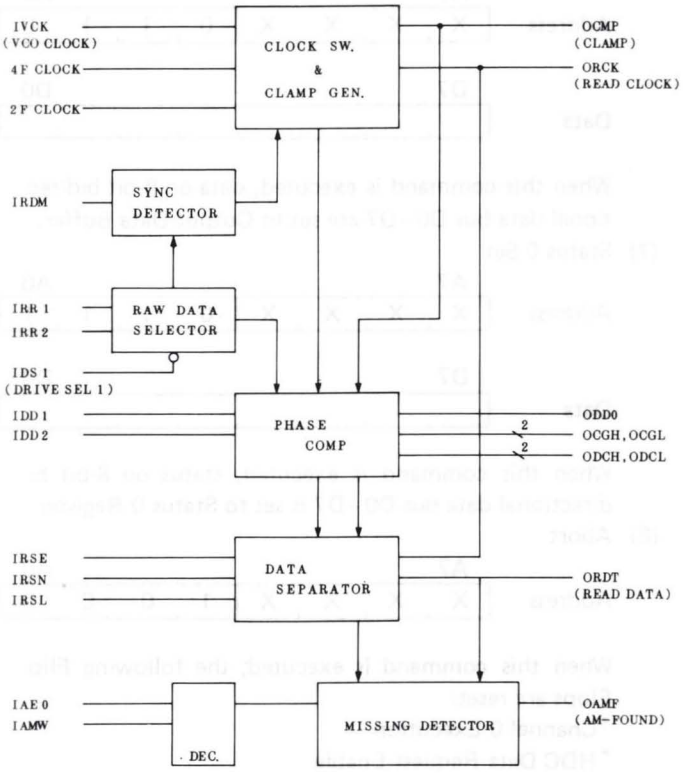
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	IRDM	11	GND	22	ODWD	32	GND
2	OWMD	12	IVCK	23	IDSI	33	OAMF
3	ODD0	13	IPED	24	IRGT	34	ORDT
4	IDD1	14	IPND	25	IAE0	35	ORCK
5	IDD2	15	IPLD	26	IAMW	36	ICS
6	IRSE	16	OCMP	27	IWGT	37	IA0
7	IRSN	17	ODCH	28	IWDN	38	IA1
8	IRSL	18	ODCL	29	14FC	39	IDB0
9	IRR1	19	OCGH	30	IRST	40	IDB1
10	IRR2	20	OCGL	31	IOUT	41	O2FC
		21	VCC			42	VCC

2) BLOCK DIAGRAM

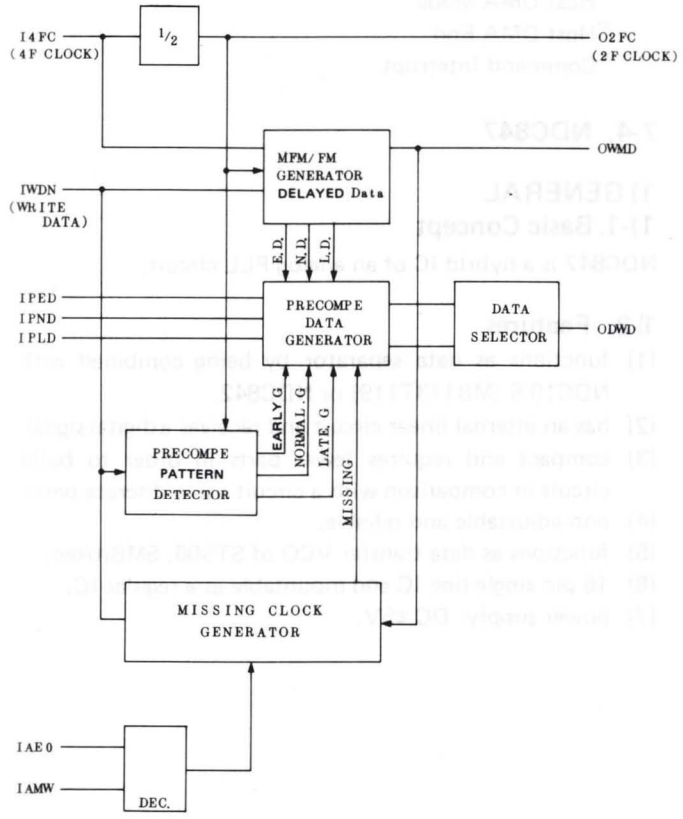
(1) Structure of the chip's Blocks



(2) Structure of the Read Block



(3) Structure of the Write Block



(1) WGT: WRITE-GATE
This inputs a Write-Gate signal for the disk. Without thi this signal, Warite operations cannot be executed.

(2) RGT: READ-GATE
This inputs a Read-Gate signal for the disk. Without this signal, Read operations cannot be executed.

(3) WDN: WRITE-DATA-NRZ
This inputs serial data at writing in the disk.

(4) AMW: AM-WRITE
This should be active high at writing data (address mark), including missing clock.

(5) AE 0: AM-ENABLE-0
Active high; this is input as a missing clock search (address serch) signal in Read-operations. This enables a writing index mark in the floppy disk, by activating with IAMW.

(6) RDM: $\overline{\text{RAW-DATA-M}}$
If this signal is at a low voltage level in address-mark searching, this counts the input Raw Data, and internal Read-conditions will be satisfied.

(7) PED: PRECOMP-EARLY-DATA
This inputs a signal for Write procompensation and becomes early data at the external selection in the mode set.

3) OPEATIONS

3)-1. Reset Input

1. RST (RESET)
Active high; this clears all the registers including all the registers that initialize this chip.

3)-2. Clock Input

1. 4FC (4F-CLOCK)
A basic clock used for internal control and the Write circuit. A half circle of this is output as 2F-Clock.
2. VCK (VCO-CLOCK)
This inputs an output clock of the VCO circuit. In Read operations, the clock generated from this clock is output as Read-Clock.

3)-3. Clock Output

1. 2FC (2F-CLOCK)
This inputs a half circle of the 4F-Clock.
2. RCK (READ-CLOCK)
In Read operations, the clock generated from the VCO clock is output synchronically with Read-Data. In non-reading, a negative clock of $\overline{\text{2F-CLOCK}}$ is output. This is temporarily set high at the switching point with 2F-CLOCK.

3)-4. Raw-Data Input and Drive Select Signals (RR1, RR2 & DS1)

This inputs receiver output of the data sent from the disk. Depending on DS1, either RR1 or RR2 will be selected. The relationship between DS1 and RR1, RR2 is the following.

DS1	RR1/RR2
Low Level	RR1 will be selected
Heigh Level	RR2 will be selected

The reading edge of RR1 and RR2 is basically the rising time by the disk.

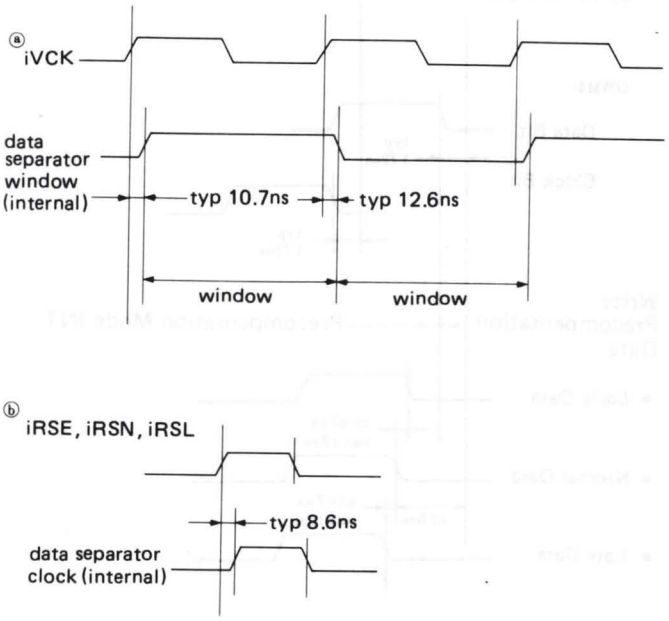
3)-5. Read Control Signals

1. RGT (READ-GATE)
Active high; Gate signal for all the Read operations.
2. AE0 (AM-ENABLE-0)
Active high; this should be active when missing clock data (address mark) is to be searched. With this signal and the AMW signal hish, in Read operations and in Write operations at the floppy disk mode, an Index mark is enabled.

3)-6 Write Control Signals

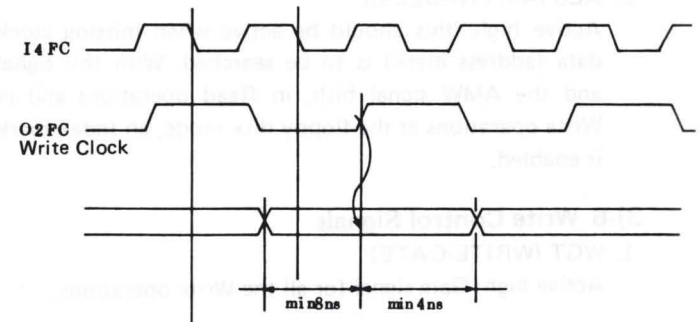
1. WGT (WRITE-GATE)
Active high; Gate signal for all the Write operations.

IVCK and Read Strobe (IRSE, IRSN, IRSL)

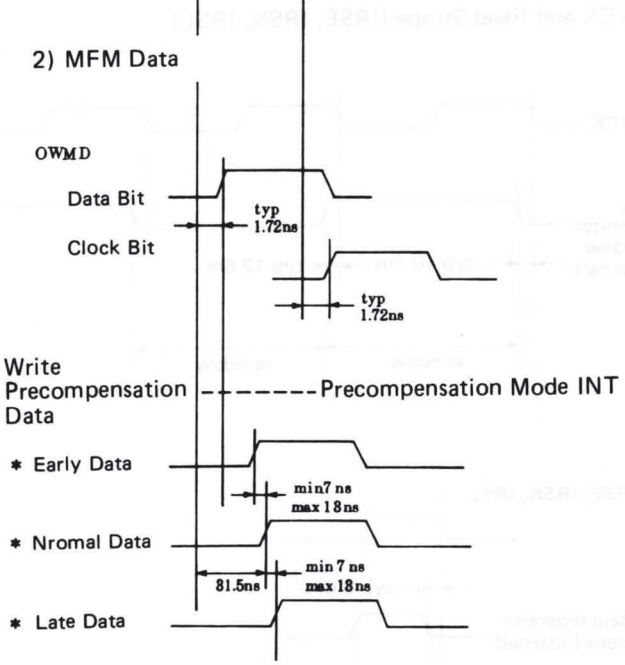


4) WRITE INPUT/OUTPUT

1) Write Clock and NRZ Input Data

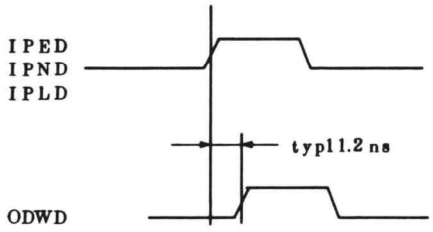


2) MFM Data

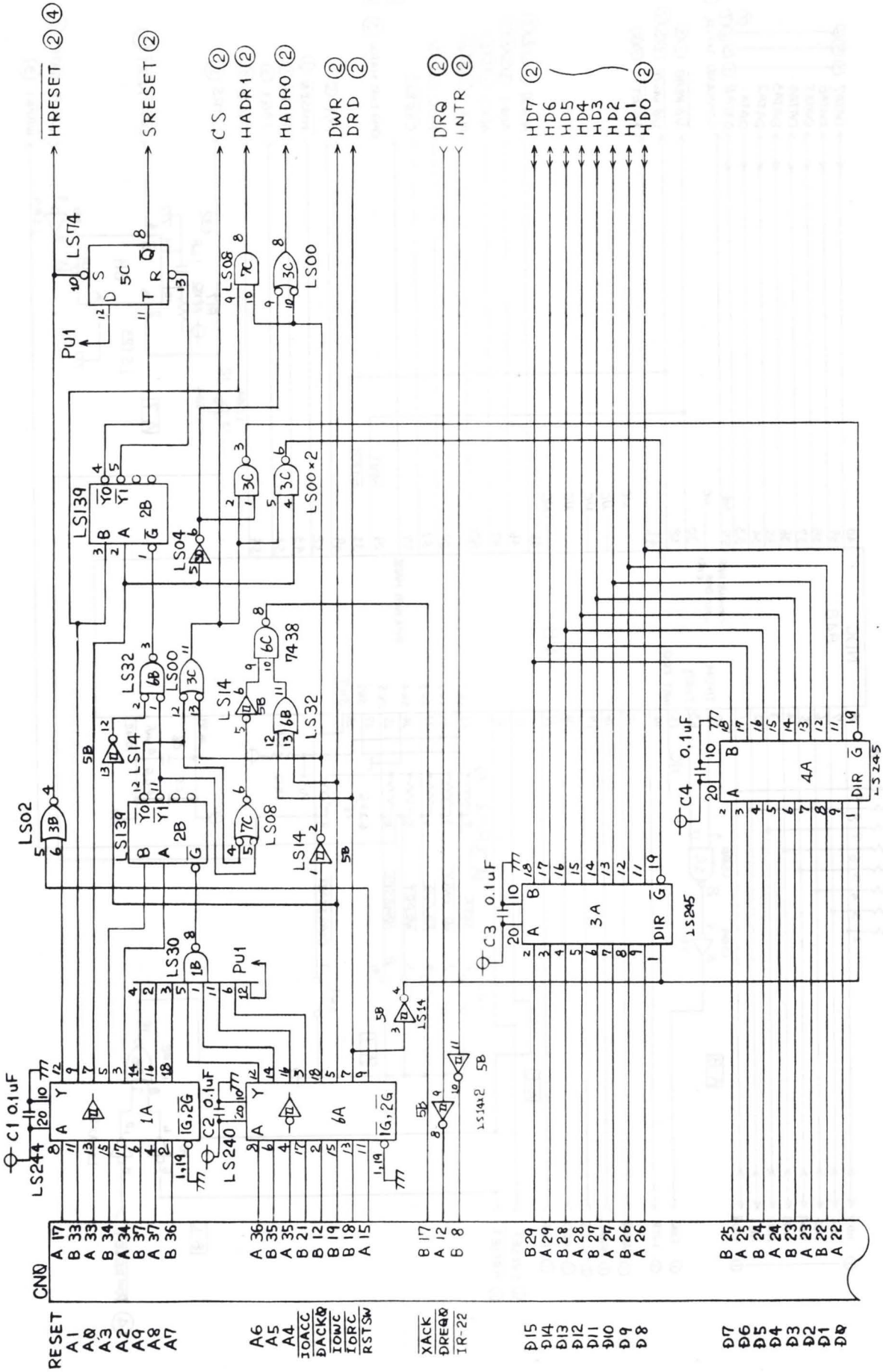


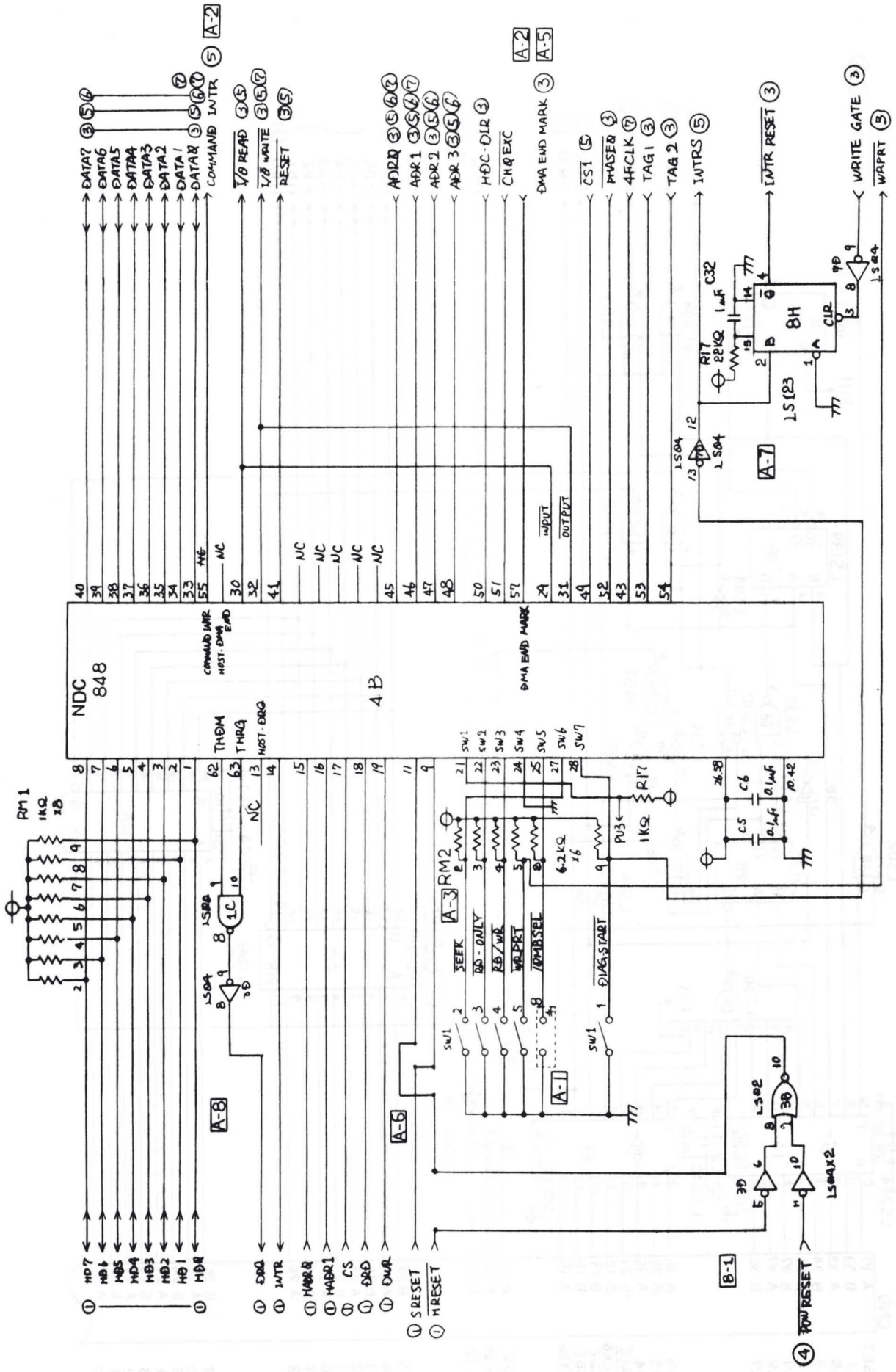
* Early normal, late . . . . . Same for Clock Bit

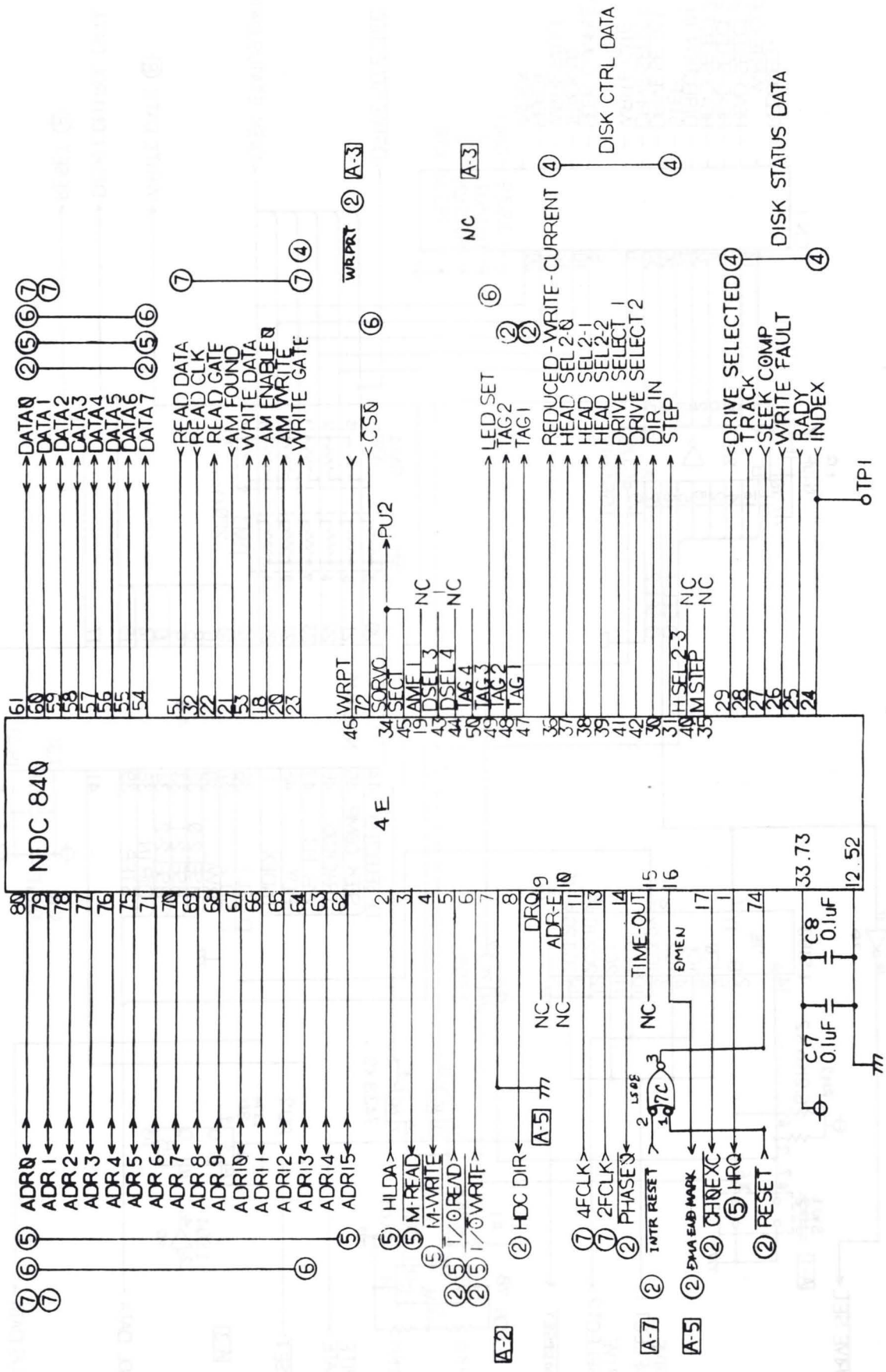
DMD Output 2. . . . . Precompensation Mode EXT

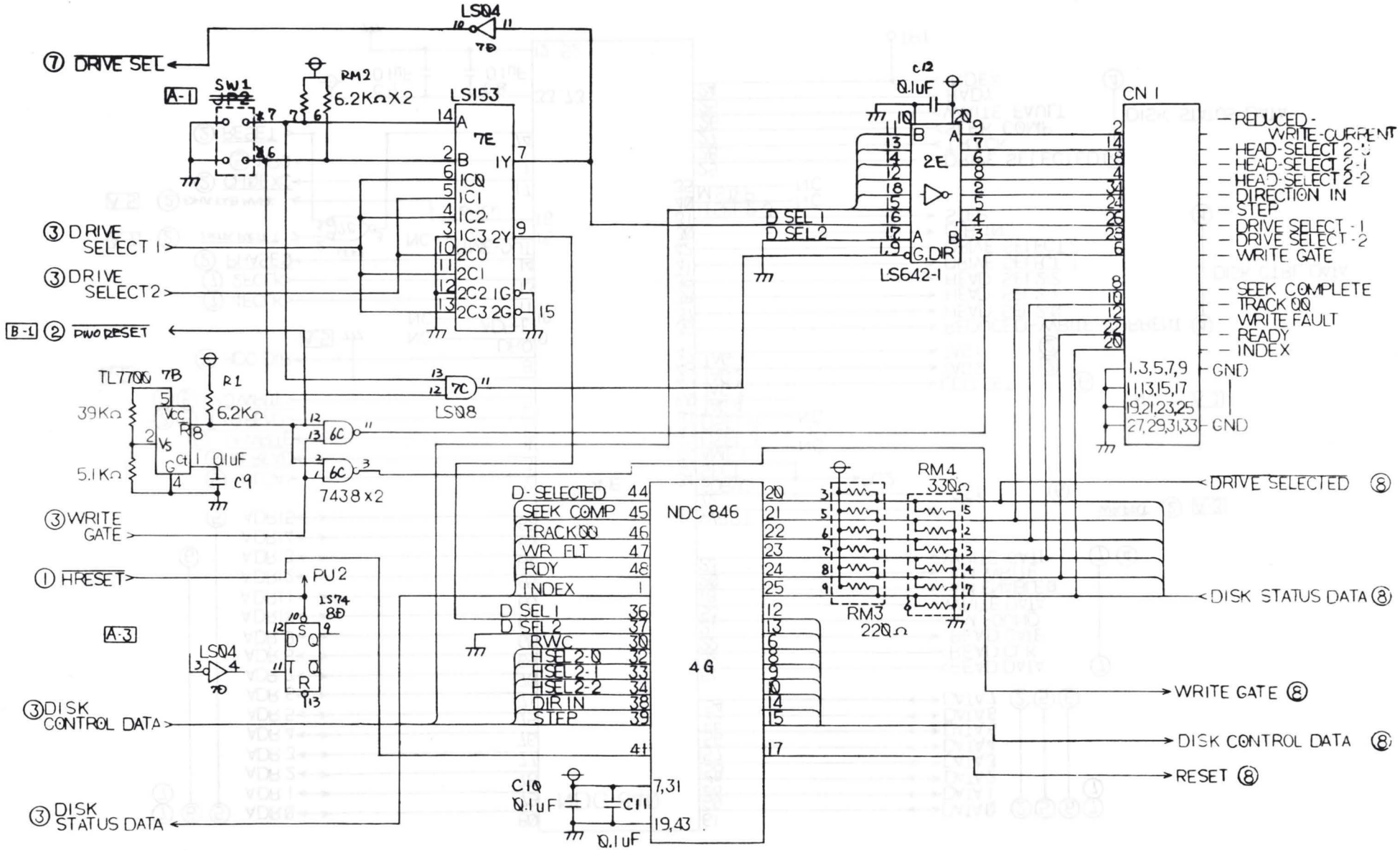


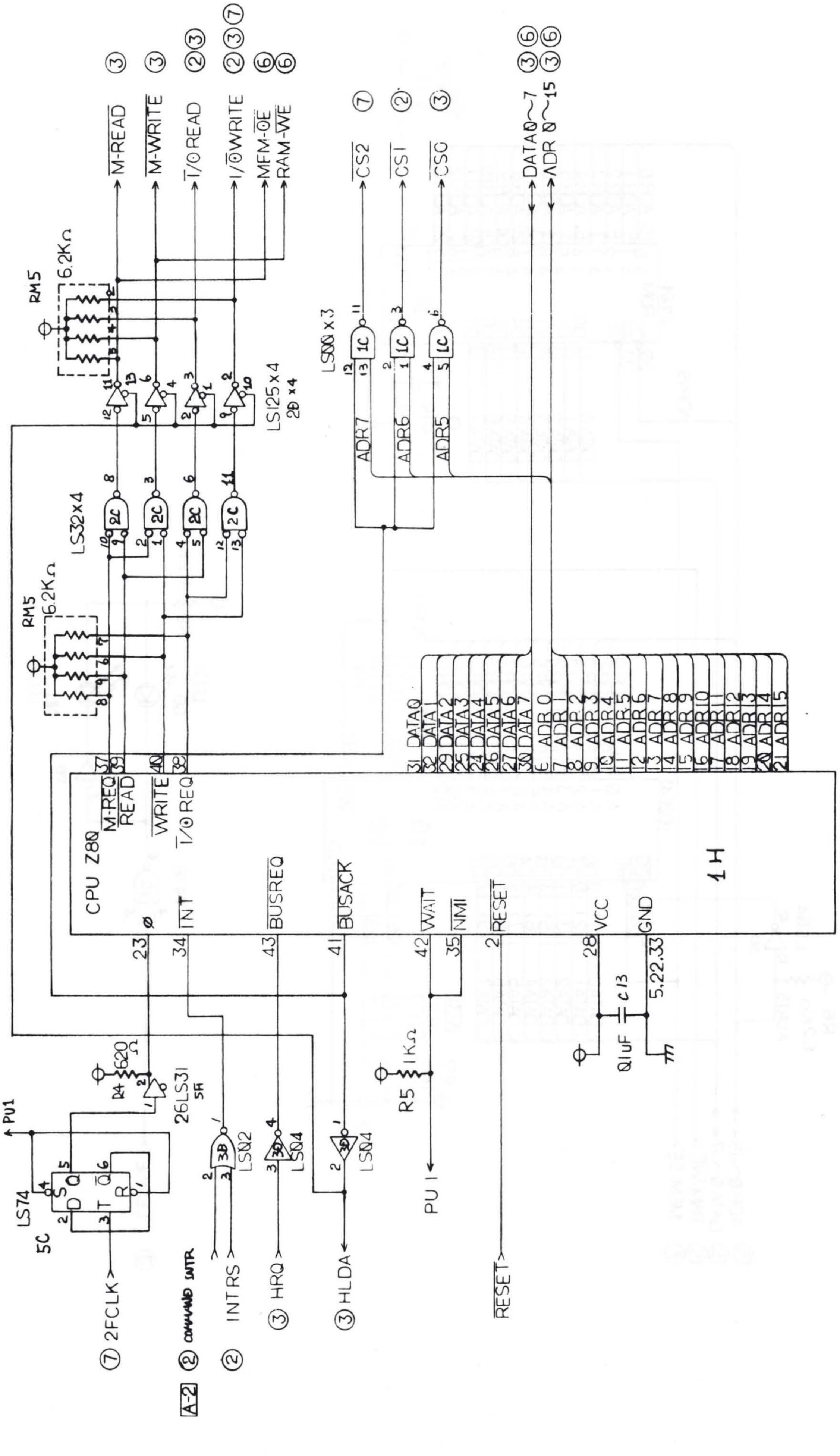
8. CIRCUIT DIAGRAM

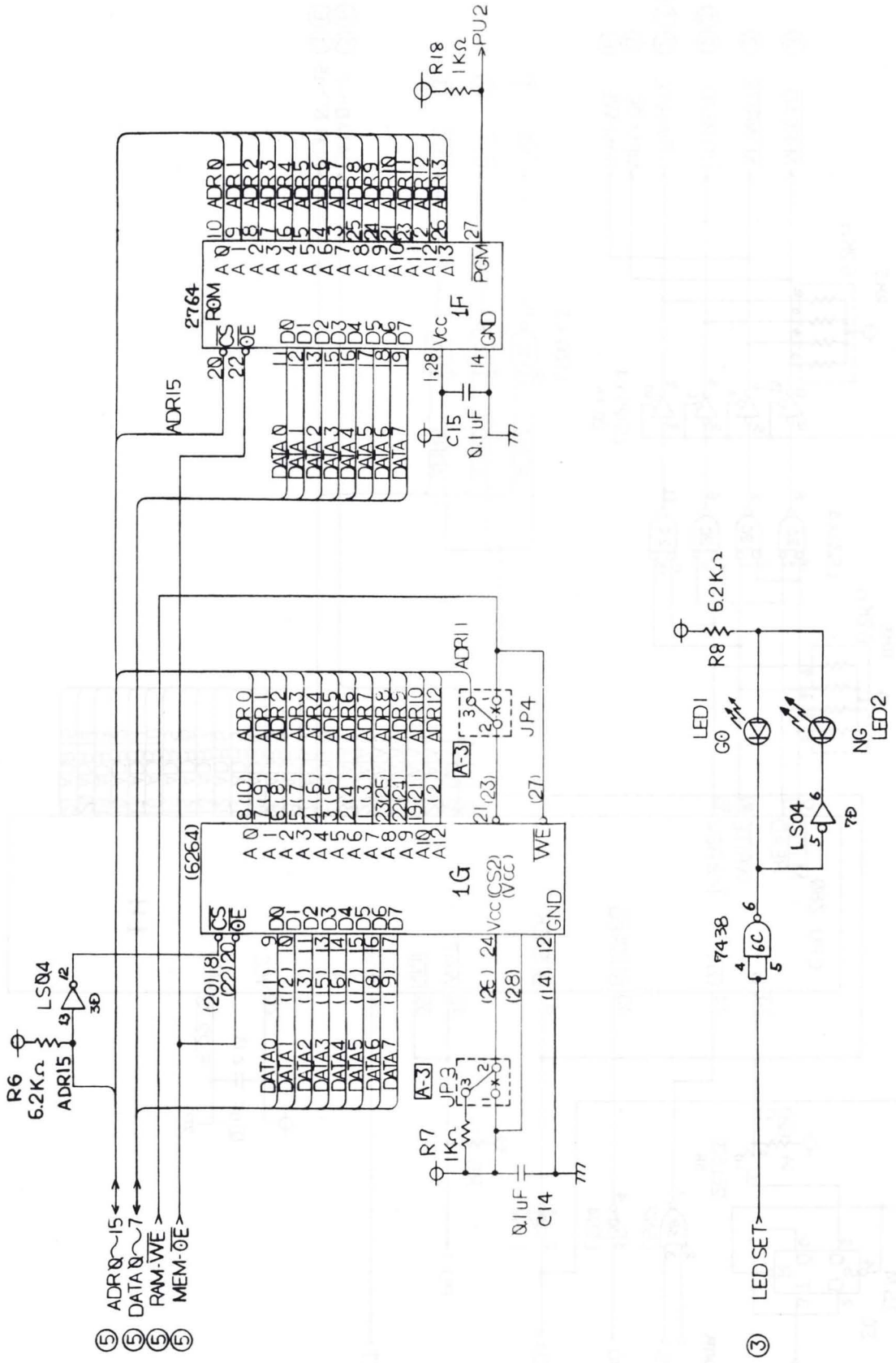


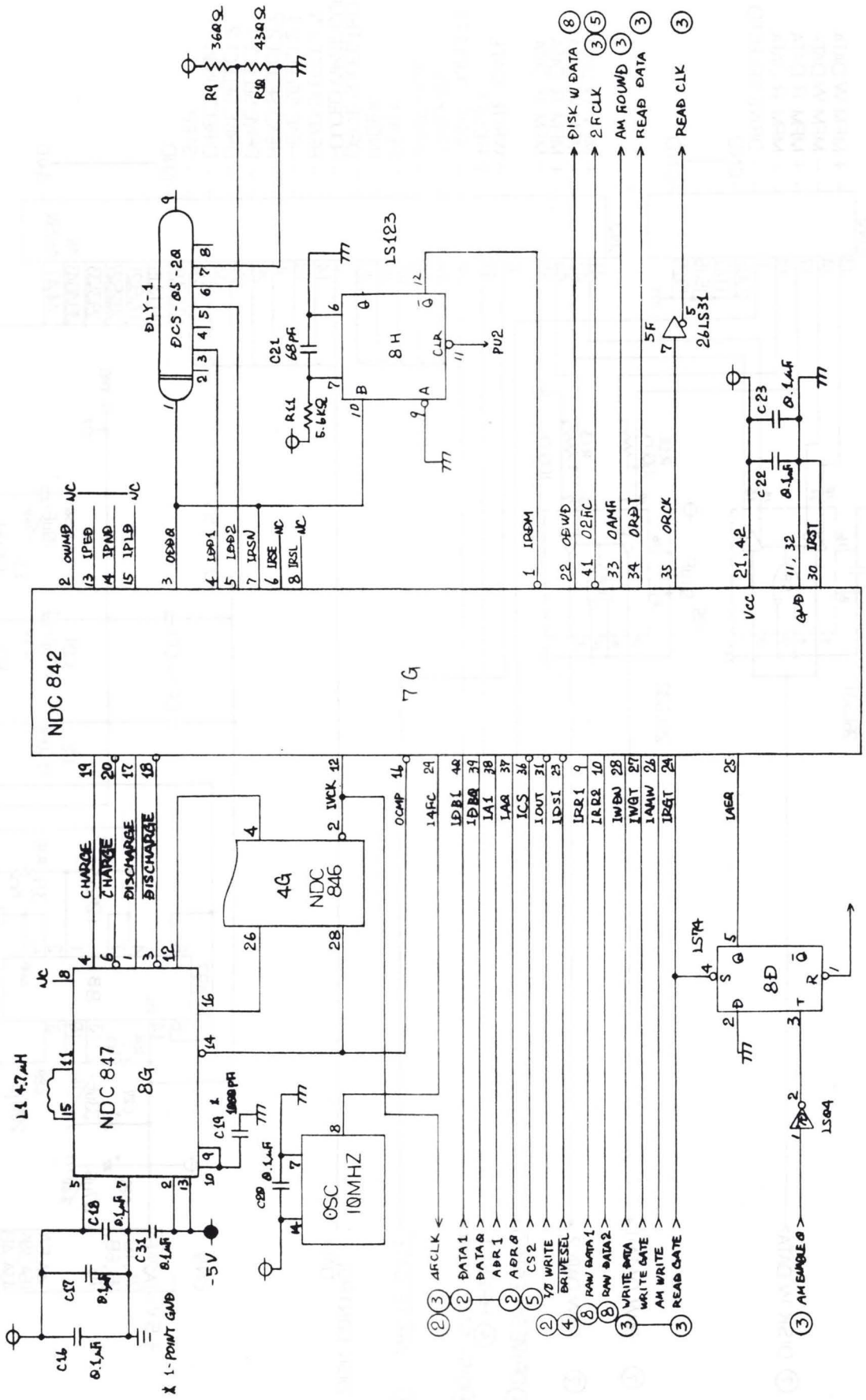

NDC
848
4B
RM1
1KΩ
x8
RM2
6.2KΩ
x8
SEEK
RD-ONLY
RD/WR
WRPRT
ZOMBSEL
DIAG.START
SW1
SW2
SW3
SW4
SW5
SW6
SW7
R17
1KΩ
R17
22KΩ
C32
1μF
C6
0.1μF
C5
0.1μF
8H
LS123
LS04
LS02
LS04X2
LS04
DATA7
DATA6
DATA5
DATA4
DATA3
DATA2
DATA1
DATA0
COMMAND INTR
I/O READ
I/O WRITE
RESET
ADDR
ADR1
ADR2
ADR3
HDC-DIR
CHG EXC
DMA END MARK
CS1
PHASE
4FCLK
TAG1
TAG2
INTRS
INTR RESET
WRITE GATE
WRPAT
HD7
HD6
HD5
HD4
HD3
HD2
HD1
HD0
DRQ
INTR
HADR0
HADR1
CS
DRD
DWR
SRESET
HRESET
POWRESET
COMMAND INTR
HOST-DMA END
THRQ
HOST-DRQ
DMA END MARK
INPUT
OUTPUT
A-1
A-2
A-3
A-5
A-7
A-8
B-1

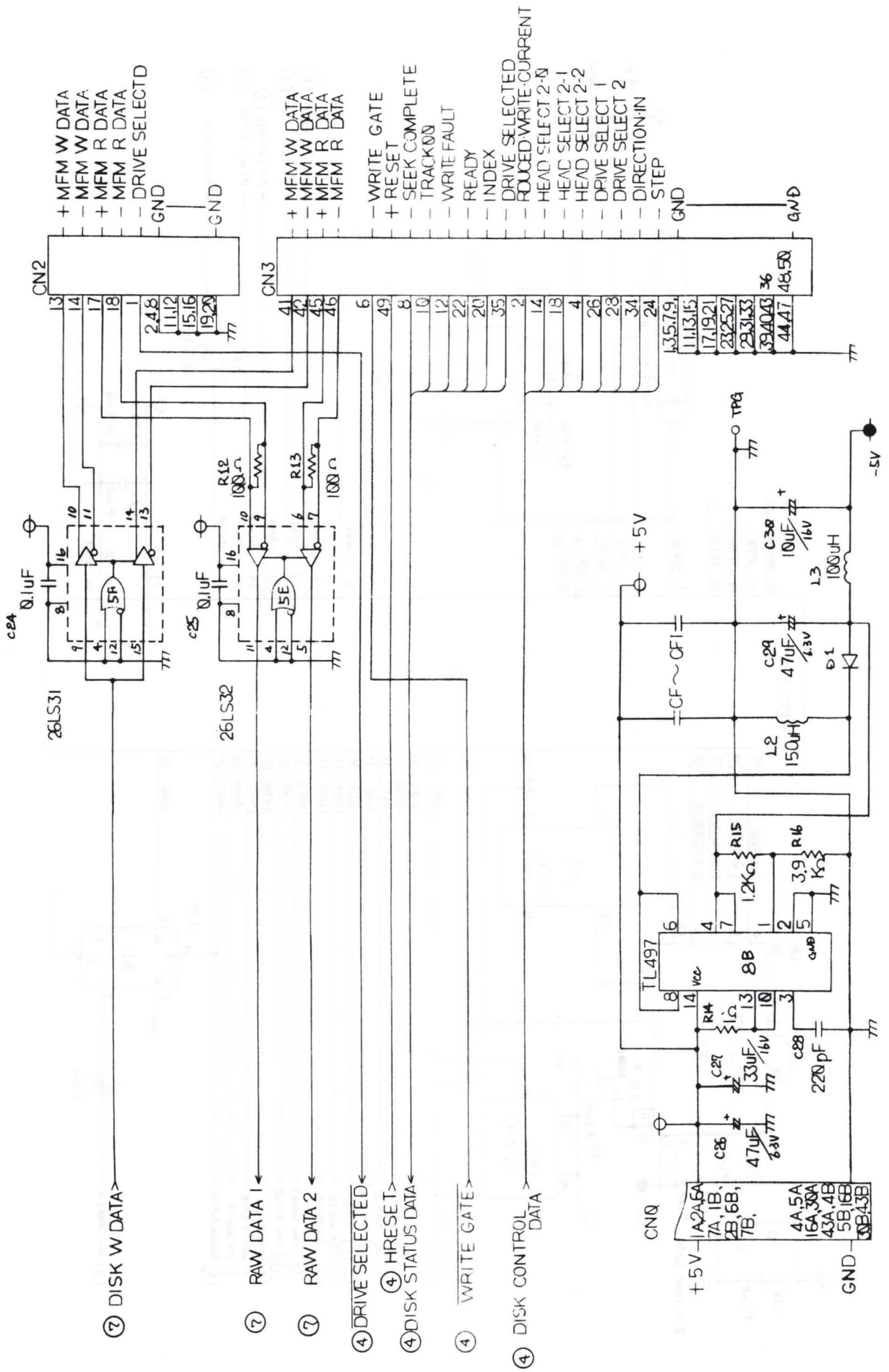

NDC 840
4E
DATA0
DATA1
DATA2
DATA3
DATA4
DATA5
DATA6
DATA7
READ DATA
READ CLK
READ GATE
AM FOUND
WRITE DATA
AM ENABLED
AM WRITE
WRITE GATE
WRPT
SORVO
SECT
AME 1
DSEL 3
DSEL 4
TAG 4
TAG 3
TAG 2
TAG 1
LED SET
REDUCED-WRITE-CURRENT
HEAD SEL 2-0
HEAD SEL2-1
HEAD SEL2-2
DRIVE SELECT 1
DRIVE SELECT 2
DIR IN
STEP
H SEL 2-3
M STEP
DRIVE SELECTED
TRACK
SEEK COMP
WRITE FAULT
RADY
INDEX
DISK CTRL DATA
DISK STATUS DATA
NC
PU2
TP1
ADR0
ADR1
ADR2
ADR3
ADR4
ADR5
ADR6
ADR7
ADR8
ADR9
ADR10
ADR11
ADR12
ADR13
ADR14
ADR15
HLDA
M-READ
M-WRITE
I/O READ
I/O WRITE
HDC DIR
DRQ
ADR-E
4FCLK
2FCLK
PHASE
TIME-OUT
INTR RESET
EMEN
CHGEXC
HRQ
RESET
C7 0.1uF
C8 0.1uF
33.73
12.52
A-2
A-3
A-5
A-7

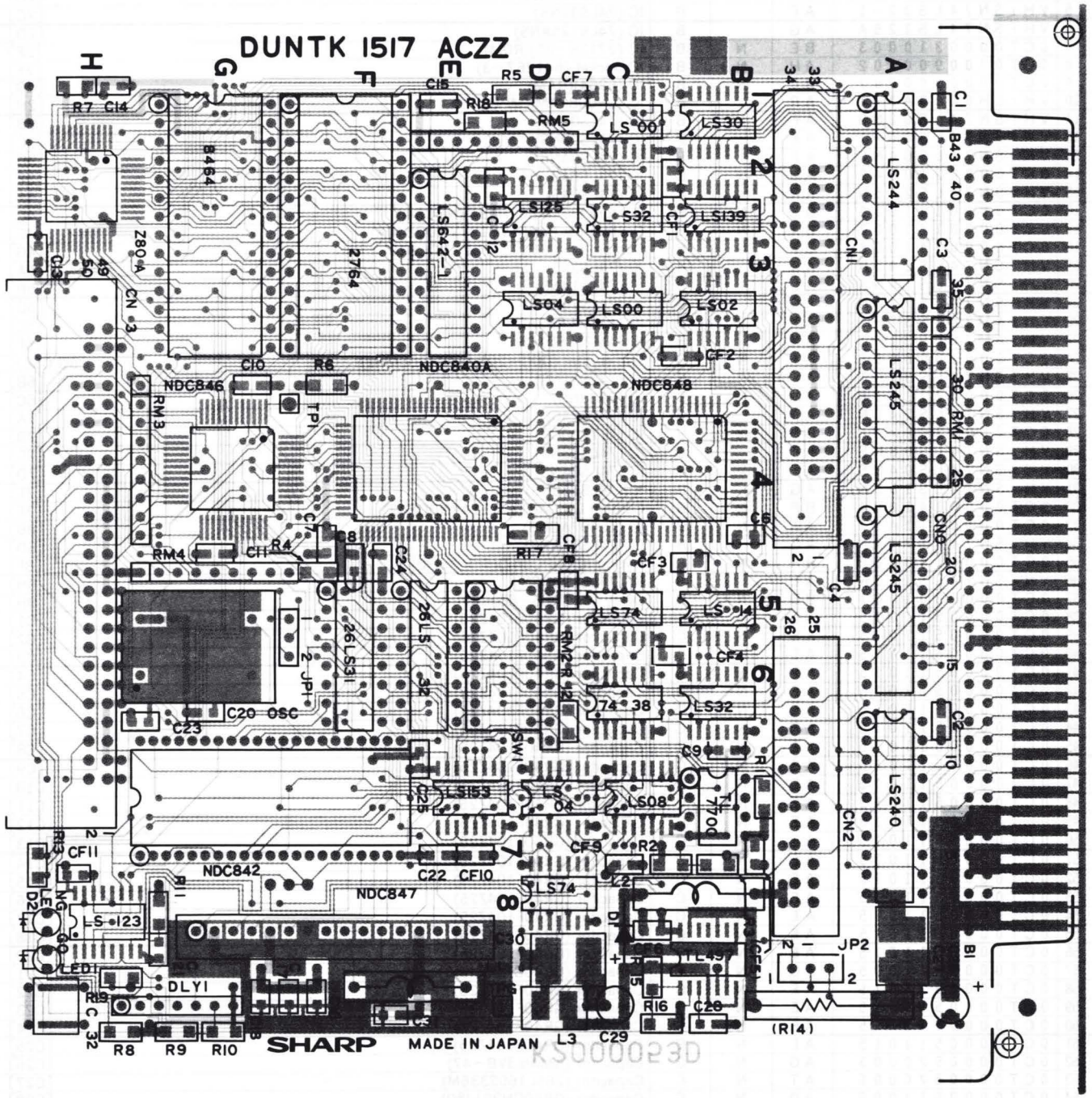

⑦ DRIVE SEL
LS04
7D
A-1
SW1
RM2
6.2KΩX2
LS153
7E
③ DRIVE SELECT 1
③ DRIVE SELECT 2
B-1 ② PWO RESET
TL7700 7B
R1
6.2KΩ
39KΩ
5.1KΩ
R8
0.1uF
C9
7C
LS08
6C
7438x2
③ WRITE GATE
① HRESET
PU2
1S74
8D
A-3
LS04
7D
③ DISK CONTROL DATA
③ DISK STATUS DATA
C12
0.1uF
2E
D SEL 1
D SEL 2
LS642-1
CN 1
REDUCED-WRITE-CURRENT
HEAD-SELECT 2-3
HEAD-SELECT 2-1
HEAD-SELECT 2-2
DIRECTION IN
STEP
DRIVE SELECT-1
DRIVE SELECT-2
WRITE GATE
SEEK COMPLETE
TRACK 00
WRITE FAULT
READY
INDEX
1,3,5,7,9 GND
11,13,15,17
19,21,23,25
27,29,31,33 GND
D-SELECTED 44
SEEK COMP 45
TRACK00 46
WR FLT 47
RDY 48
INDEX 1
D SEL 1 36
D SEL 2 37
RWC 30
HSEL 2-0 32
HSEL 2-1 33
HSEL 2-2 34
DIR IN 38
STEP 39
NDC 846
4G
RM4
330Ω
RM3
220Ω
DRIVE SELECTED ⑧
DISK STATUS DATA ⑧
WRITE GATE ⑧
DISK CONTROL DATA ⑧
RESET ⑧
C10
0.1uF
C11
0.1uF
7,31
19,43


A-2
CPU Z80
1H
M-REQ
READ
WRITE
I/O REQ
INT
BUSREQ
BUSACK
WAIT
NMI
RESET
VCC
GND
LS74
5C
2FCLK
COMMAND INTR
INTRS
HRQ
HLDA
RESET
PU1
26LS31
LS02
LS04
R4 620Ω
R5 1KΩ
0.1uF
C13
RM5 6.2KΩ
LS32x4
LS125x4
LS00x3
M-READ
M-WRITE
I/O READ
I/O WRITE
MFM-OE
RAM-WE
CS2
CS1
CS0
ADR7
ADR6
ADR5
DATA0~7
ADR 0~15


2764
ROM
1F
PGM
Vcc
GND
CS
OE
ADR15
PU2
R18
1KΩ
C15
0.1uF
(6264)
1G
WE
Vcc(CS2)
(Vcc)
JP4
JP3
A-3
R6
6.2KΩ
LS04
R7
1KΩ
C14
0.1uF
R8
6.2KΩ
LED1
GO
LED2
NG
7438
LS04
LED SET
ADR0~15
DATA0~7
RAM-WE
MEM-OE


NDC 842
7G
NDC 847
8G
NDC 846
4G
OSC 10MHZ
8H
8D
DLY-1
DCS-05-28
1S123
28LS31
1S74
1S04
L1 4.7μH
X 1-POINT GND
-5V
VCC
GND
CHARGE
DISCHARGE
DISK W DATA
2F CLK
AM ROM/D
READ DATA
READ CLK
DATA1
DATA0
ABR1
ABR0
CS2
FD WRITE
DRIVESEL
RAW DATA1
RAW DATA2
WRITE DATA
WRITE GATE
AM WRITE
READ GATE
AM ENABLE 0


CN2
+ MFM W DATA
- MFM W DATA
+ MFM R DATA
- MFM R DATA
- DRIVE SELECTD
GND
GND
CN3
+ MFM W DATA
- MFM W DATA
+ MFM R DATA
- MFM R DATA
- WRITE GATE
+ RESET
- SEEK COMPLETE
- TRACK00
- WRITE FAULT
- READY
- INDEX
- DRIVE SELECTED
- REDUCED WRITE CURRENT
- HEAD SELECT 2-0
- HEAD SELECT 2-1
- HEAD SELECT 2-2
- DRIVE SELECT 1
- DRIVE SELECT 2
- DIRECTION-IN
- STEP
GND
GND
C24 0.1uF
C25 0.1uF
26LS31
26LS32
R12 100Ω
R13 100Ω
C26 47uF 6.3V
C27 33uF 16V
R14 1Ω
C28 220pF
TL497
R15 1.2KΩ
R16 3.9KΩ
L2 150uH
L3 100uH
C29 47uF 2.3V
C30 10uF 16V
D1
CF ~ CF1
+5V
-5V
TP9
CN9
+5V
GND
1A,2A,6A
7A,1B,
2B,6B,
7B,
4A,5A
16A,30A
43A,4B
5B,16B
30B,43B
⑦ DISK W DATA
⑦ RAW DATA 1
⑦ RAW DATA 2
④ DRIVE SELECTED
④ HRESET
④ DISK STATUS DATA
④ WRITE GATE
④ DISK CONTROL DATA


DUNTK 1517 ACZZ
SHARP
MADE IN JAPAN
NDC840A
NDC842
NDC846
NDC847
NDC848
Z80-A
8464
2764
LS244
LS245
LS240
LS00
LS02
LS04
LS08
LS30
LS32
LS74
LS123
LS125
LS139
LS153
LS642-1
74 38
DLY1
LED
OSC
JP1
JP2
SW1
TP1
(R14)

9. PARTS GUIDE AND LIST

1 20MB Hard Disk Interface for MZ5600A

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
1	VHiSN74LS30-1	AE		B	IC (74LS30NS)	[1B]
2	VHiSN74LS00-1	AE		B	IC (74LS00NS)	[1C]
3	VHiSN74LS244N	AS		B	IC (74LS244)	[2A]
4	VHiSN74LS139N	AL		B	IC (74LS139NS)	[2B]
5	VHiSN74LS32-1	AF		B	IC (74LS32NS)	[2C]
6	VHiSN74LS125A	AG		B	IC (74LS125ANS)	[2D]
7	0CT0000310003	BE	N	B	IC (27128-30)(ROM)	[2F]
8	0CT0000900002	AH	N	B	IC Socket (641267-3)	[2F]
9	0CT0000300002	BL	N	B	IC (6264)(RAM)	[2G]
10	VHiLH0080A3-1	AR		B	IC (LH0080AM)(MPU)	[2H]
11	VHiSN74LS02NS	AF		B	IC (74LS02NS)	[3B]
12	VHiSN74LS00-1	AE		B	IC (74LS00NS)	[3C]
13	VHiSN74LS04NS	AF		B	IC (74LS04NS)	[3D]
14	0CT0000210642	AU	N	B	IC (74LS642-1)	[3E]
15	VHiSN74LS245N	AR		B	IC (74LS245)	[4A]
16	0CT0000141010	BF	N	B	Custom Lsi (MB62H197)(NDC848)	[4C]
17	0CT0000141002	BX	N	B	Custom Lsi (MB61VH127)(NDC840A)	[4E]
18	0CT0000141008	BF	N	B	Custom Lsi (MB111T152)(NDC846)	[4G]
19	VHiSN74LS245N	AR		B	IC (74LS245)	[5A]
20	VHiSN74LS14NS	AL		B	IC (74LS14NS)	[5B]
21	VHiSN74LS74AN	AG		B	IC (74LS74ANS)	[5C]
22	VHiAM26LS32-1	AX		B	IC (AM26LS32ACN)	[5E]
23	VHiAM26LS31-1	AX		B	IC (AM26LS31CN)	[5F]
24	0CT0001000001	BA	N	B	Dsc crystal (D0C-20NA-10.000MHz)	[6G(OSC)]
25	VHiSN74LS32-1	AF		B	IC (74LS32NS)	[6B]
26	0CT0000221038	AM	N	B	IC (7438NS)	[6C]
27	VHiSN74LS240N	AR		B	IC (74LS240)	[7A]
28	0CT0000300///	BD	N	B	IC (TL7700CP)	[7B]
29	VHiSN74LS08NS	AF		B	IC (74LS08NS)	[7C]
30	VHiSN74LS04NS	AF		B	IC (74LS04NS)	[7D]
31	VHiSN74LS153N	AG		B	IC (74LS153NS)	[7E]
32	0CT0000141004	BP	N	B	Custom Lsi (MB113T114)(NDC842)	[7F]
33	0CT0000311497	AW	N	B	IC (TL497ACNS)	[8B]
34	VHiSN74LS74AN	AG		B	IC (74LS74ANS)	[8D]
35	0CT0000143009	BA	N	B	Hybrid IC (NPC847)(シングル型)	[8F]
36	VHiSN74LS123N	AL		B	IC (74LS123NS)	[8H]
37	0CT0000301001	BD	N	B	Delay line (DCS-05-20)	[9H]
38	0CT0000511015	AE	N	C	Capacitor (GR40F104Z25)	[C1]
39	0CT0000511015	AE	N	C	Capacitor (GR40F104Z25)	[C2]
40	0CT0000511015	AE	N	C	Capacitor (GR40F104Z25)	[C3]
41	0CT0000511015	AE	N	C	Capacitor (GR40F104Z25)	[C4]
42	0CT0000511015	AE	N	C	Capacitor (GR40F104Z25)	[C5]
43	0CT0000511015	AE	N	C	Capacitor (GR40F104Z25)	[C6]
44	0CT0000511015	AE	N	C	Capacitor (GR40F104Z25)	[C7]
45	0CT0000511015	AE	N	C	Capacitor (GR40F104Z25)	[C8]
46	0CT0000511015	AE	N	C	Capacitor (GR40F104Z25)	[C9]
47	0CT0000511015	AE	N	C	Capacitor (GR40F104Z25)	[C10]
48	0CT0000511015	AE	N	C	Capacitor (GR40F104Z25)	[C11]
49	0CT0000511015	AE	N	C	Capacitor (GR40F104Z25)	[C12]
50	0CT0000511015	AE	N	C	Capacitor (GR40F104Z25)	[C13]
51	0CT0000511015	AE	N	C	Capacitor (GR40F104Z25)	[C14]
52	0CT0000511015	AE	N	C	Capacitor (GR40F104Z25)	[C15]
53	0CT0000511015	AE	N	C	Capacitor (GR40F104Z25)	[C16]
54	0CT0000511015	AE	N	C	Capacitor (GR40F104Z25)	[C17]
55	0CT0000511015	AE	N	C	Capacitor (GR40F104Z25)	[C18]
56	0CT0000511015	AE	N	C	Capacitor (GR40F104Z25)	[C20]
57	0CT0000511005	AG	N	C	Capacitor (GR40CH680K50)	[C21]
58	0CT0000511015	AE	N	C	Capacitor (GR40F104Z25)	[C22]
59	0CT0000511015	AE	N	C	Capacitor (GR40F104Z25)	[C23]
60	0CT0000511015	AE	N	C	Capacitor (GR40F104Z25)	[C24]
61	0CT0000511015	AE	N	C	Capacitor (GR40F104Z25)	[C25]
62	0CT0000520003	AG	N	C	Capacitor (KMA6.3VB-47)	[C26]
63	0CT0000520006	AT	N	C	Capacitor (265L1602336M)	[C27]
64	0CT0000511009	AD	N	C	Capacitor (GR40CH221J50)	[C28]
65	0CT0000520003	AG	N	C	Capacitor (KMA6.3VB-47)	[C29]
66	0CT0000520004	AP	N	C	Capacitor (265L1602106M)	[C30]
67	0CT0000511020	AK	N	C	Capacitor (GR40-1F105Z50)	[C32]
68	0CT0000511015	AE	N	C	Capacitor (GR40F104Z25)	[CF1]
69	0CT0000511015	AE	N	C	Capacitor (GR40F104Z25)	[CF2]
70	0CT0000511015	AE	N	C	Capacitor (GR40F104Z25)	[CF3]
71	0CT0000511015	AE	N	C	Capacitor (GR40F104Z25)	[CF4]
72	0CT0000511015	AE	N	C	Capacitor (GR40F104Z25)	[CF5]
73	0CT0000511015	AE	N	C	Capacitor (GR40F104Z25)	[CF6]
74	0CT0000511015	AE	N	C	Capacitor (GR40F104Z25)	[CF7]
75	0CT0000511015	AE	N	C	Capacitor (GR40F104Z25)	[CF8]
76	0CT0000511015	AE	N	C	Capacitor (GR40F104Z25)	[CF9]
77	0CT0000511015	AE	N	C	Capacitor (GR40F104Z25)	[CF10]
78	0CT0000511015	AE	N	C	Capacitor (GR40F104Z25)	[CF11]
79	0CT0000933002	BA	N	C	Connector (HU-260P2K-S13T)	[CN1]
80	0CT0000933001	BD	N	C	Connector (HU-340P2D-S13)	[CN2]

1 20MB Hard Disk Interface for MZ5600A

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
81	0CT0000933003	BG	N	C	Connector (HU−500P2−L13D8C)	[CN3]
82	VHDDS1588L2−1	AB		B	Diode (1S1588)	[D1]
83	0CT0000600002	AF	N	C	Inductor (LAL04NA4R7K)	[L1]
84	0CT0000600009	AN	N	C	Inductor (TPF0410−151K)	[L2]
85	0CT0000601005	AG	N	C	Inductor (NL453232−101K)	[L3]
86	0CT0000720001	AE	N	B	LED (TLR123)(赤色)	[LED1]
87	0CT0000720002	AE	N	B	LED (TLG123A)(緑色)	[LED2]
88	0CT0000411029	AC	N	C	Resistor (CRG 1/8 622J)	[R1]
89	0CT0000411031	AC	N	C	Resistor (CRG 1/8 393J)	[R2]
90	0CT0000411027	AC	N	C	Resistor (CRG 1/8 512J)	[R3]
91	0CT0000411019	AC	N	C	Resistor (CRG 1/8 621J)	[R4]
92	0CT0000411021	AC	N	C	Resistor (CRG 1/8 102J)	[R5]
93	0CT0000411029	AC	N	C	Resistor (CRG 1/8 622J)	[R6]
94	0CT0000411021	AC	N	C	Resistor (CRG 1/8 102J)	[R7]
95	0CT0000411029	AC	N	C	Resistor (CRG 1/8 622J)	[R8]
96	0CT0000411015	AC	N	C	Resistor (CRG 1/8 361J)	[R9]
97	0CT0000411017	AC	N	C	Resistor (CRG 1/8 431J)	[R10]
98	0CT0000411028	AC	N	C	Resistor (CRG 1/8 562J)	[R11]
99	0CT0000411010	AC	N	C	Resistor (CRG 1/8 101J)	[R12]
100	0CT0000411010	AC	N	C	Resistor (CRG 1/8 101J)	[R13]
101	0CT0000411003	AP	N	C	Resistor (SN14−L3A−1Ω J)	[R14]
102	0CT0000411022	AC	N	C	Resistor (CRG 1/8 122J)	[R15]
103	0CT0000411025	AC	N	C	Resistor (CRG 1/8 392J)	[R16]
104	0CT0000411021	AC	N	C	Resistor (CRG 1/8 102J)	[R17]
105	0CT0000411021	AC	N	C	Resistor (CRG 1/8 102J)	[R18]
106	0CT0000411030	AC	N	C	Resistor (CRG 1/8 223J)	[R19]
107	0CT0000410007	AG	N	C	Block resistor (C09×1.0KΩ J)	[RM1]
108	0CT0000410011	AG	N	C	Block resistor (C09×6.2KΩ J)	[RM2]
109	0CT0000410004	AG	N	C	Block resistor (C09X220Ω J)	[RM3]
110	0CT0000410005	AG	N	C	Block resistor (C09×330Ω J)	[RM4]
111	0CT0000410011	AG	N	C	Block resistor (C09×6.2KΩ J)	[RM5]
112	0CT0001100012	AW	N	B	Dip switch (KTD08)	[SW1]
113	0CT0001100000	AE	N	C	Test pin (TP−8G)	[TP1]
114	0CT0001100000	AE	N	C	Test pin (TP−8G)	[TPG]

SHARP

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