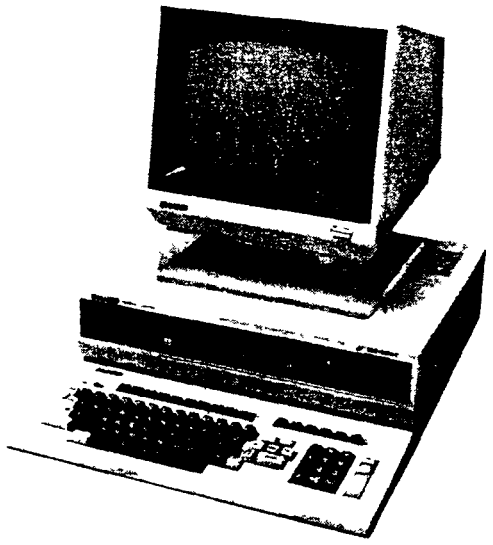
MZ-3500

SHARP SERVICE MANUAL

CODE: 00ZMZ 3500SM/E



PERSONAL COMPUTER

MODEL MZ-3500

CONTENTS

1. Specifications 1
2. Software (Memory) Configuration 7
3. CPU and memory 12
4. CRT display 25
5. MFD interface 52
6. R232C interface 72
7. Printer interface 78
8. Other interface 81
9. Power circuit discription 87
10. Keyboard controller circuit discription 90
11. Self check functions 94
12. IPL flow chart 103
13. Circuit diagram & P.W.B

Parts list & Guide

SHARP CORPORATION

1. SPECIFICATIONS

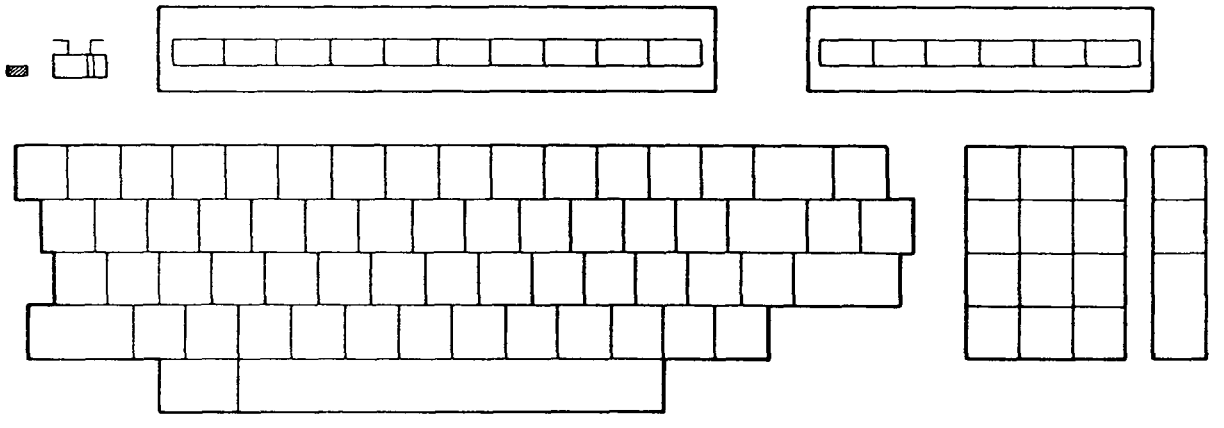
1-1. Specification of the main unit (Model 35XX)

Outline	1) High speed processing using multi-CPU 2) Built in mini floppy disk 3) Built in printer interface and RS232C serial interface 4) Connection of up to two video display units (separate graphic display or overlaid display possible on two individual color monitor units) 5) Permits the use of standard CP/M					
	Model 3530 incluse a single double-side, double density mini floppy disk and 64 KB RAM. Model MZ3540 has two double-side, density mini floppy disks and 64 KB RAM.				Model 3531 includes a single double side, double density mini floppy disk and 128 KB Model 3541 has two double side, double density mini floppy disks, and 128 KB	
	LSI	CPU	Multi-CPU processing		Z80A microprocessor x 2	
		MEMORY	ROM	IPL	8K Byte ROM	
				C, G	8K Byte ROM	
			RAM	For main CPU	64K Bit DRAM x 16 chips or 8 chips	
				For sub-CPU	16K Bit SRAM x 4 chips	
				Shared RAM	16K Bit SRAM x 1 chip	
				VIDEO RAM	16K Bit SRAM x 1 chip 4K Bit SRAM x 2 chips	
		I/O	Custom LSI	Memory mapper	TH	SP6102R001
				Screen controller	CSP-1 CSP 2	SP6102C002 SP6102C003
			GDC	CRT controller	μPD7220	
			FDC	Floppy disk controller	μPD765	
			PIO	Parallel I/O port	8255	
			SIO	Serial I/O port	8251	
			TIMER	Counter	8253	
			CLOCK	Clock	μPD1990AC	
	DISPLAY		Screen structure	80 characters x 25 lines, 80 x 20, 40 x 25, or 40 x 20		
			Elements	8 x 16, 8 x 8		
			Attribute	Reverse, blink, line (horizontal, vertical)		
			Colors	8 colors on each character and background color		
			I/F	2 channels (applicable CRT 640 x 400, 640 x 200, B/W or color)		
	MFD	MZ353X	One double-side, double density floppy disk	256 bytes/sector, 16 sectors/track, 80 tracks/disk		
		MZ354X	Two double-side, double density floppy disks	Built-in interface for optional MFD		
	Other I/F	Light pen				
		Keyboard	Dedicated keyboard			
		Printer	Centronics interface			
		RS232C	No protocol, asynchronus mode, 110 to 9600 bps, half-duplex			
	Other functions	Speaker (500mW)	Battery backup clock	HALT SW	Speaker volume control	
	Software	FDOS	BASIC	High class compatible with PC3200 BASIC, supplemented and graphic control commands		
				Expanded RS232C, GPIB, and GPIO		
			Utilities	BACKUP, INIT, COPY, DEBUG, KILLALL		
		CP/M	Basic CP/M Expanded CP/M			
	Accessories	Intstruction Manual master floppy disk power cord				

1-2. MZ-1K01 (Keyboard) specification

Outline	MZ1K02 U.S. keyboard (ASCII) MZ1K04 German keyboard			MZ1K03: U.K. keyboard (ISO). MZ1K05: French keyboard						
Specification	LSI, IC	Keyboard controller		80C49 or 8749						
		CMOSIC		4049 x 2, 4514						
	Keys (98)	Sculpture key		Mechanical contact key, with life of 10,000,000 operations.						
		Alphanumeric keys	61	Ten key	15	Function keys	6	Definable keys	10	
		Mode switch	1							
	Interfacing cables	For data transfer with the CPU (serial) and power supply (transmission under 15,000 baud)								
		Use of coiled cable with 8-pin DIN plug								
	Other	Repeat function	Automatic repeat occurs 0.64 seconds after continuous depression of the same key.			2	Two-key rollover			
		Indicators (4 LED's)	POWER, Alphanumeric keys							
	Cabinet	Molded	Color	Office gray						
		Size (W x H x L)		467 x 35 x 190	Weight	About 1.5kg (3.3 lb)				

Keyboard layout

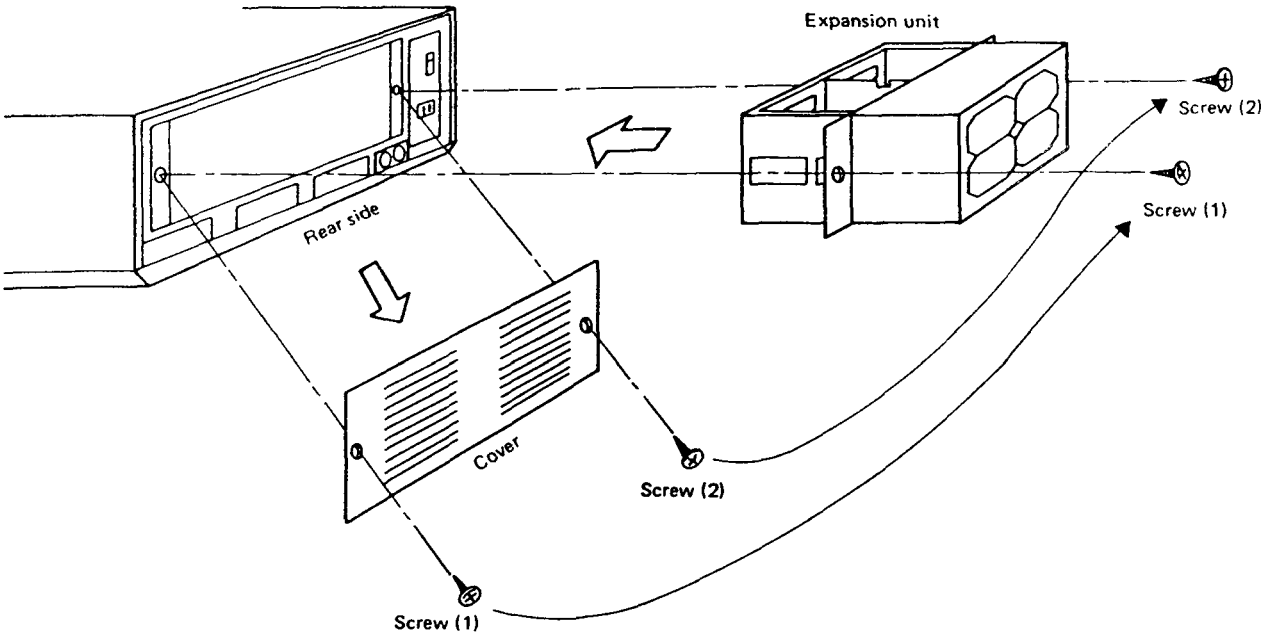


Refer to the page 7 IN "CIRCUIT DIAGRAM"

1-3. MZ-1U02

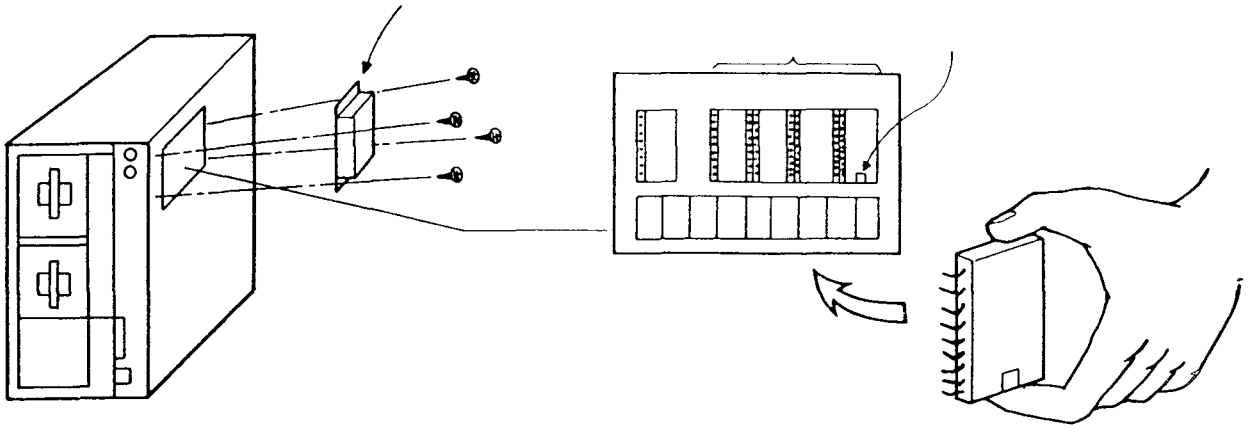
Outline	Expansion unit for the MZ-3500 series CPU, which can be attached to the rear side of the main unit. Optional boards are plugged in to the expansion box. The expansion box will accomodate up to four option boards.
Specifications	Number of slots: 4 slots
	Slot connector. 60-pin edge connector x 4
	Area of the slot inserting option board: 140.5 x 140
	Slot for option and slot number

	Slot 1	Slot 2	Slot 3	Slot 4
MZ-1R06 (expansion RAM)	O		O	
SFD I/F		O		O
Expansion RS232C	O	O	O	O
GPIO	O	O	O	O
GPIB (IEEE I/F)	O	O	O	O



1-4. MZ-1R03

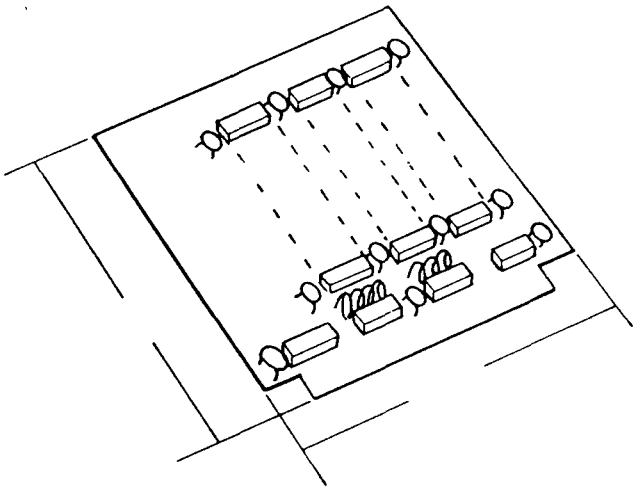
Outline	Optional board used graphic display functions with the Model-3500 series CPU. It includes 32KB of RAM. It is inserted through the slot on the front panel of the PU. The MZ-1U02 expansion box is not required.				
Specifications	LSI	GDC	Graphic controller	μPD7220	
		VIDEO RAM	Basic (buit-in)	16KDRAM x 16 (32KB)	
			Expansion (optional)	16KDRAM x 32 (64KB)	
	Graphic functions (Color must be specified for each dot, when the color video unit is in use)	VIDEO RAM		32KB (basic)	96KB (maximum expansion)
		640 x 200 green monitor		640 x 200 dots Two screens	640 x 200 dots Six screens
		640 x 200 color monitor			640 x 200 dots Two screens
		640 x 400 green monitor		640 x 400 dots One screen	640 x 400 dots Three screens
		640 x 400 color monitor			640 x 400 dots One screen
	Software	BASIC graphic control statements		SDISP	Screen designation for two video units.
				ODISP	Designation of output screen.
				CHANGE DISP	Mode designation
				GCOLOR	Graphic pattern designation
				CLS	Cleared by the color specified.
				PSET	Dot set
				PRESET	Dot reset
				LINE	Line creation
				GTABLE	Table creation
				CIRCLE	Circle creation
				PAINT	Paint over
				GINPUT	Input of graphic pattern
				GDISP	Display of graphic pattern
				GPRINT	Output of graphic pattern on printer
				GREAD	Read of coordinates
				GENTER	Input of pattern within the specified area
				GCURSOR	Graphic cursor position designation
				GSCROL	Graphic screen scrolling
				SYMBOL	Graphic symbol displaying
				SCALE	Scren scle-down designation



1-6. MZ-1R06

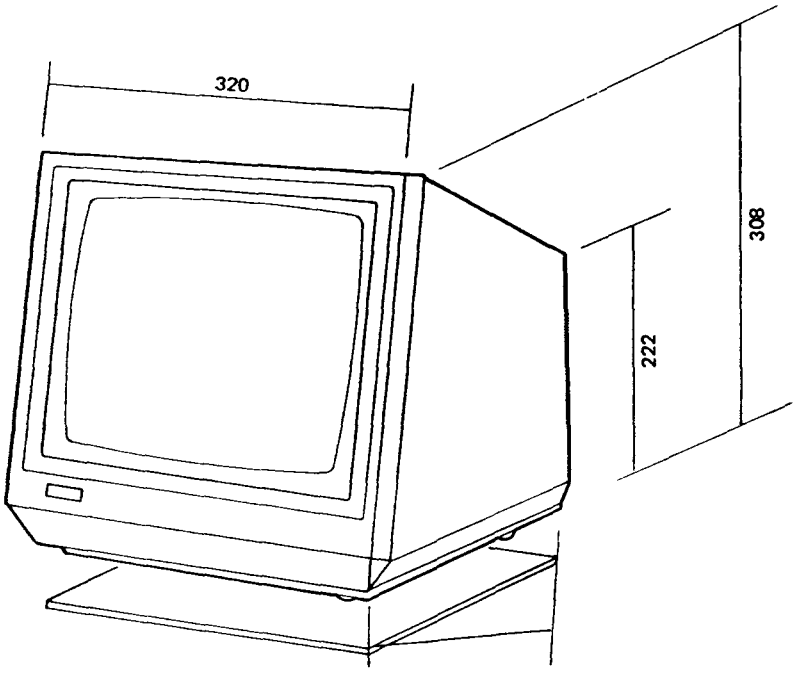
Outline	Optional board for memory expantion of the MZ-3500 sries CPU. with this option the main memory (RAM) can be expanded up to a maximum of 256 KB. This option plug into the expantion box in slot 1 or 3.		
Specifications	LSI	Basic	64KDRAM x 8 (64KB)
		Expansion	64KDRAM x 8 (128KB)
	Memory and user area		

		Main CPU only	Use of MZ-1R06	Using eight 64K RAM's on the MZ-1R06
Total capacity of the main CPU RAM		128 KB	192 KB	256 KB
BASIC (RAM BASE)	SYSTEM AREA	* 57 KB	←	←
	USER AREA	80 KB	128 KB	208 KB

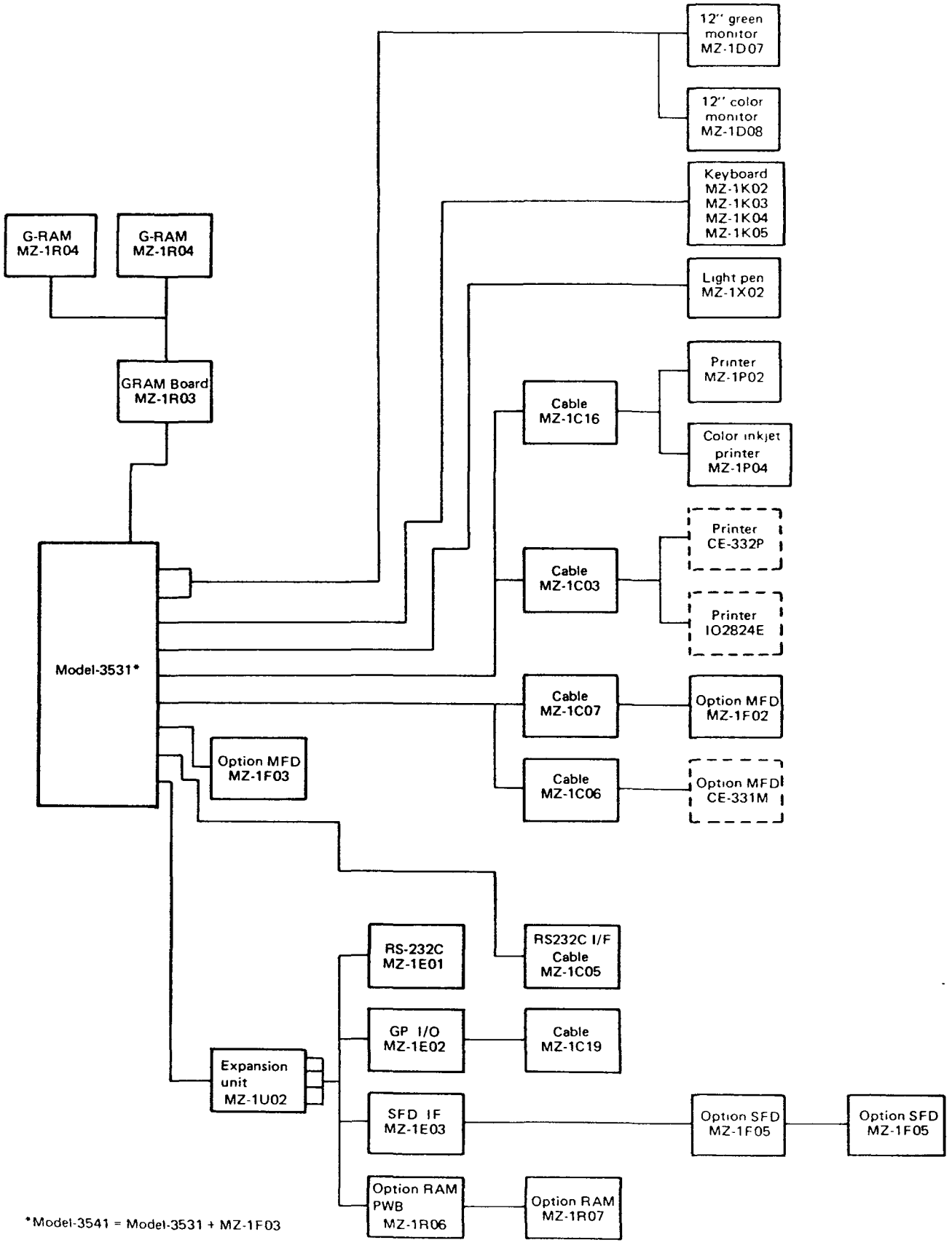


1-7. MZ-1D07

Outline	High resolution MZ 3500 series 12 green monitor				
Specifications	Video tube	Type	Non glare green	Size	12", 90° deflection
		Fluorescent color P39 (green, long PERSISTANCE)			
	Display capacity	Total number of display characters	2,000 characters (80 characters x 25 lines)	Display capacity	640 horizontal dots, 400 vertical lines
	Display size	220 x 145			
	Input signals	Method	Separate input, TTL level		
		Horizontal	20 86kHz	Vertical	47 8 Hz
	Power supply	29W power consumption			
	Cabinet	Molded	Color	Office gray	
		Size (W x H x L)	324 x 310 x 356	Weight	7.2 kg
	Adjusting knobs	3	Vertical synchronization, contrast, brightness		
	Accessories	CPU connection cable and power cord and Tilt stand			



1-8. System configuration of Model 3500



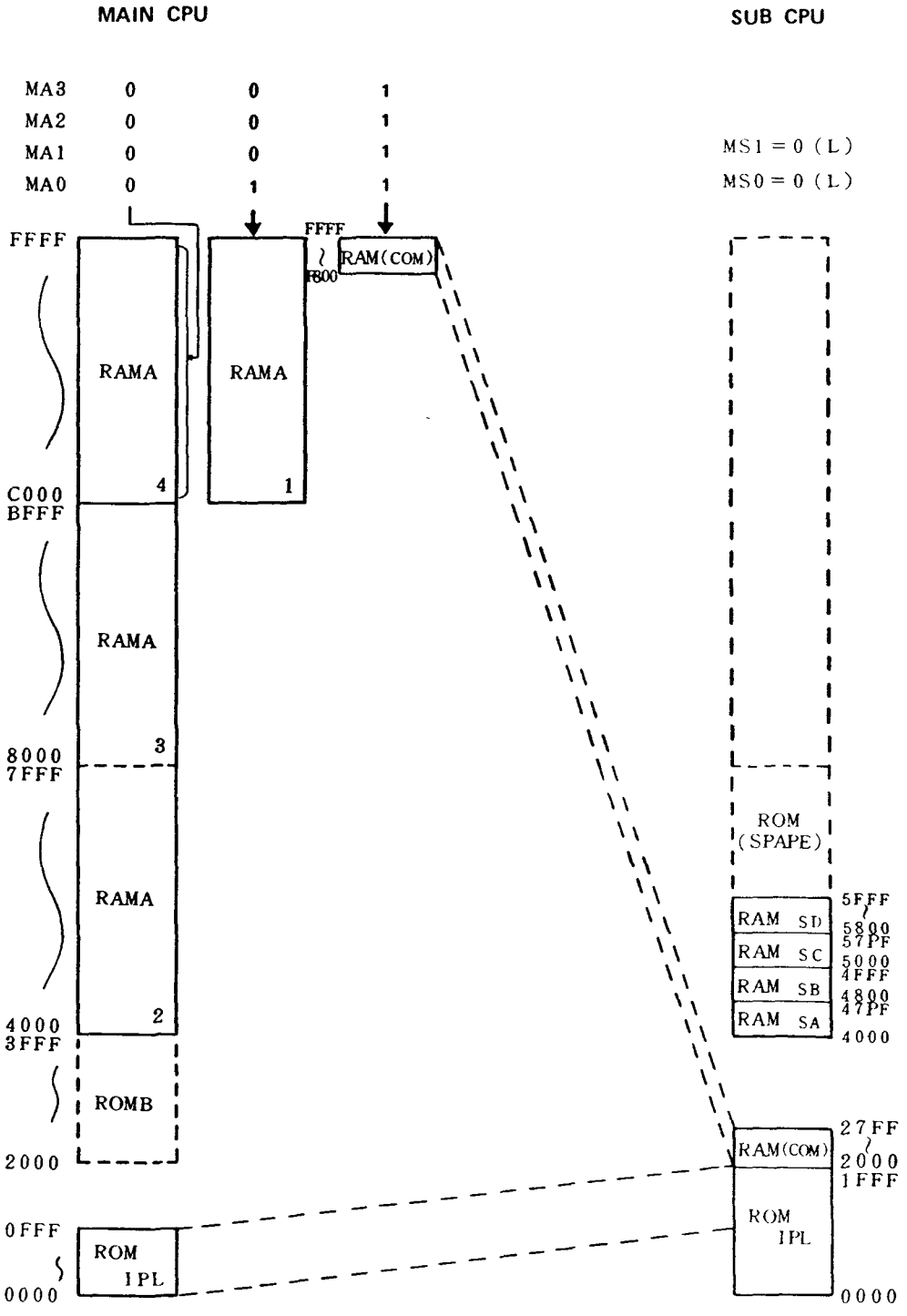
*Model-3541 = Model-3531 + MZ-1F03

2. SOFTWARE (MEMORY) CONFIGURATION

Memory will be operated under four states of SD0 ~ SD3, depending on the hardware and software configurations. In the paragraphs to follow, description will be made for those four states.

2-1. SD0 (INITIALIZE STATE)

SD0 can only exist immediately after power on, and the system executes IPL under this condition and that the system thus loaded will automatically assign memory area for SD1, SD2, and SD3.



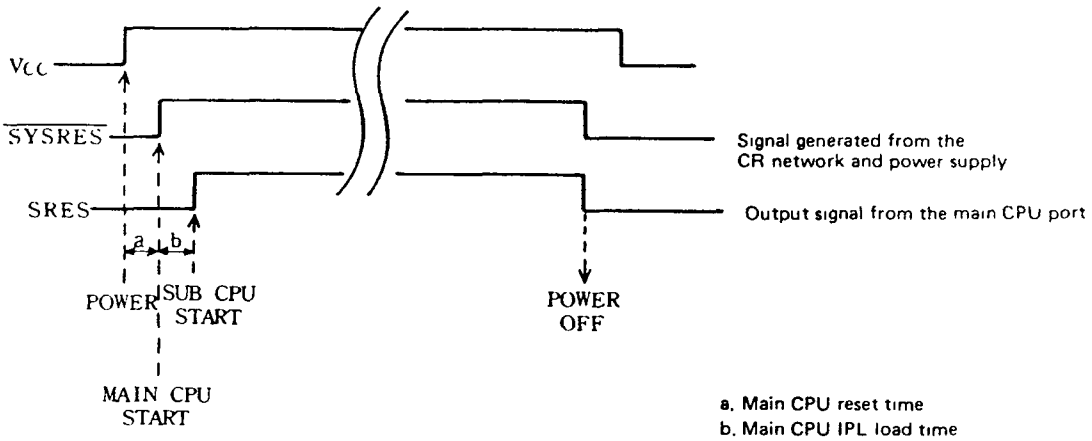
Operational description

(1) Upon reset after power on, the main CPU loads the contents of the initial program loader (IPL) into RAM starting at address 4000H, during which time reset is applied to the sub-CPU.

(2) The main CPU then terminates resetting the sub CPU and starts the sub-CPU. At the same time, the ROM IPL is assigned to the sub-CPU.

(3) The main CPU then send the memory allocation (state) to SD1, and starts to load DOS from the system floppy disk.

TIMING OF RESET SIGNAL

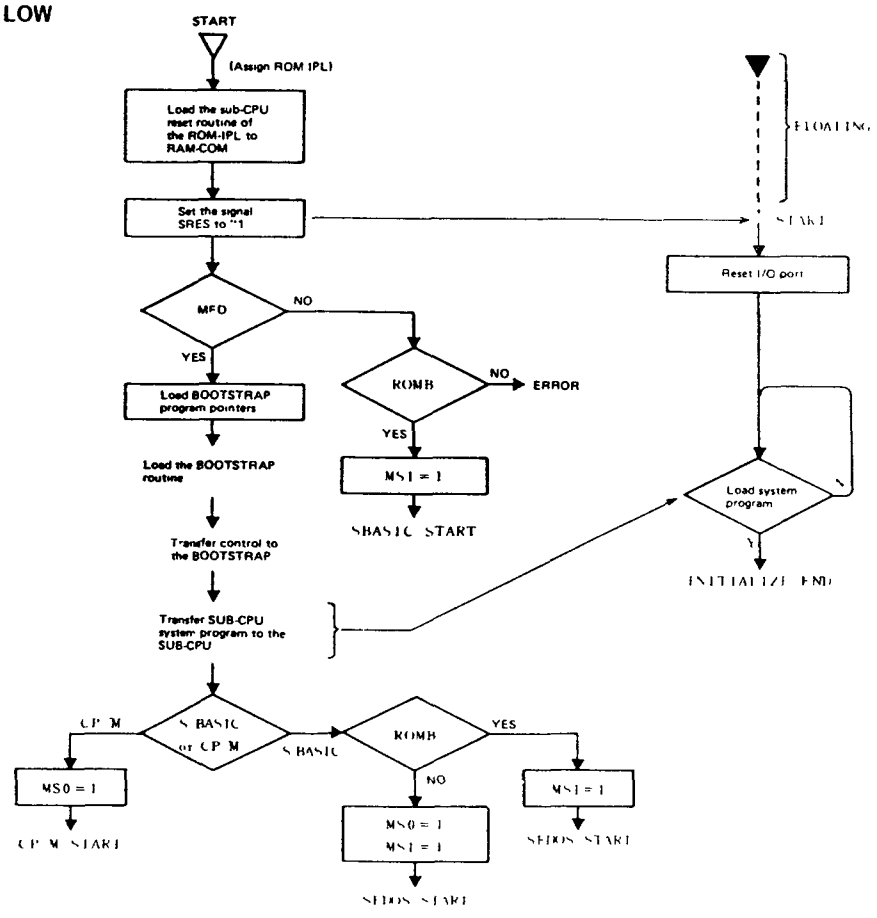


a. Main CPU reset time
b. Main CPU IPL load time

Memory Map Data:

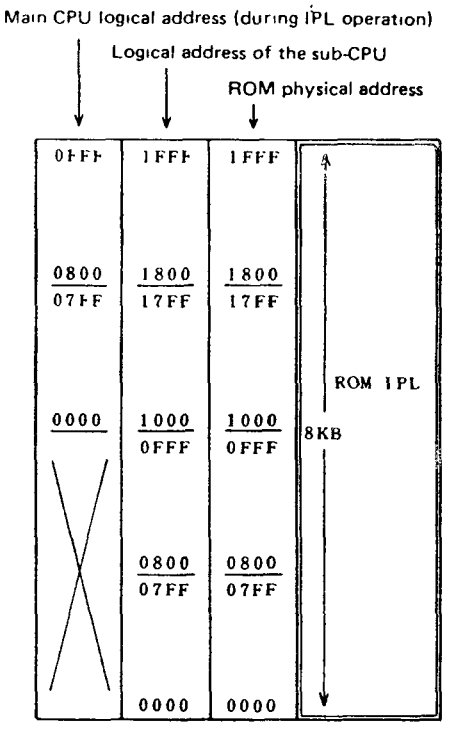
1. ROM-B is tested to determine if ROM's are present.
2. The ROM-IPL functions under control of the main CPU at first, but later it functions under the sub-CPU after the IPL program has been loaded in RAM.
3. RAM-COM is shared by both the main CPU and the sub-CPU.
4. Memories other than described above cannot be accessed under the SD0 state.
5. Bank select, MA0~MA3, is used within the address range of C000H-FFFFH.

INITIALIZE FLOW



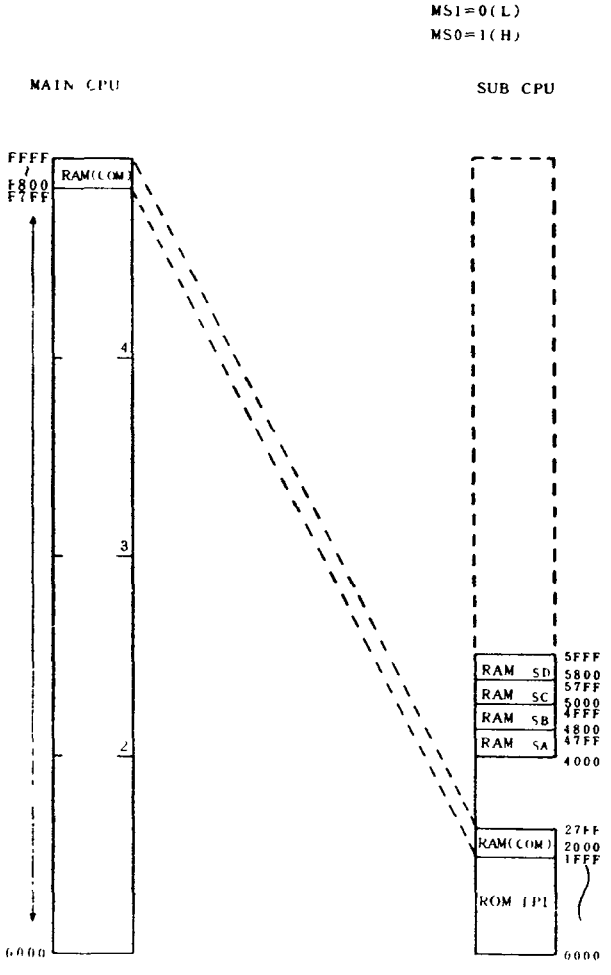
ROM-IPL

1. An 8KB ROM (2764 or mask ROM equivalent) is used for the ROM-IPL.
2. When the system reset signal turns from low to high state after power on, the main CPU starts to operate At this stage, the ROM-IPL is addressed.
3. The CPU starts from address 0000(ROM address 10000)
4. The main CPU sets the sub-CPU reset signal from low to high state as it goes out of its initial state via the memory mapper and the sub-CPU starts to operate. At this point, the ROM-IPL is addressed by the sub-CPU.
5. Address 0000 of the sub-CPU is ROM address (0000) The memory area above ROM address (1000) cannot be used by the sub-CPU because the main CPU initial program has been loaded there.



2-2. SD1 (SYSTEM LOADING & CP/M)

SD1 determines which operating system is in use. The system is loaded in the CP/M (Control Program for Micro-processors) mode.



Operational description

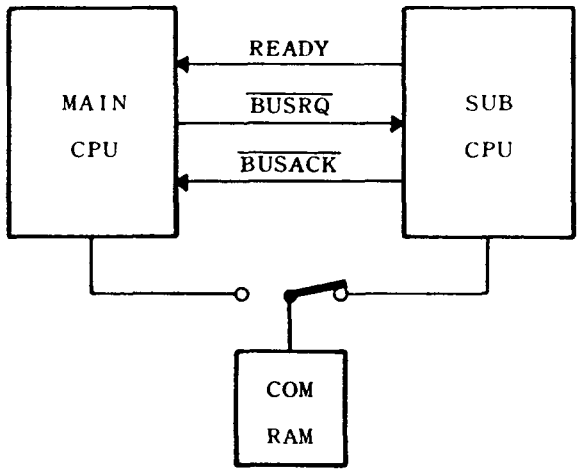
(1) As soon as the sub-CPU is started, it initializes the I/O port and waits for program transfer (IOCS) from the main CPU. This IOCS (Input Output Control System) is the program resident at address 4000H-5FFFH.

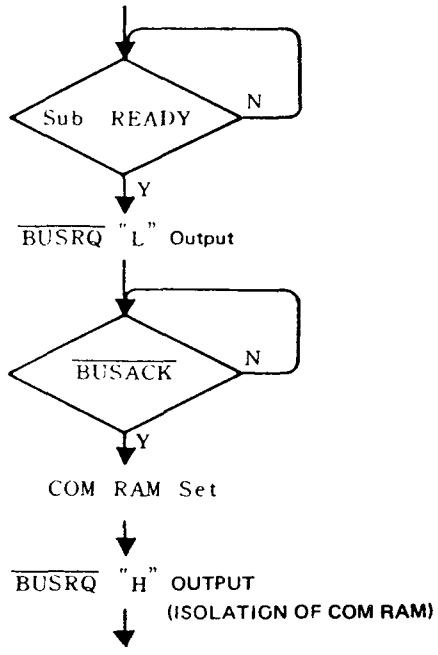
(2) As the main CPU loads the information from sector "1" of track "0" of the floppy disk, it loads the IOCS and bootstrap routine to the sub-CPU.

(3) The bootstrap program is loaded next.

(4) The bootstrap program determines memory allocation.

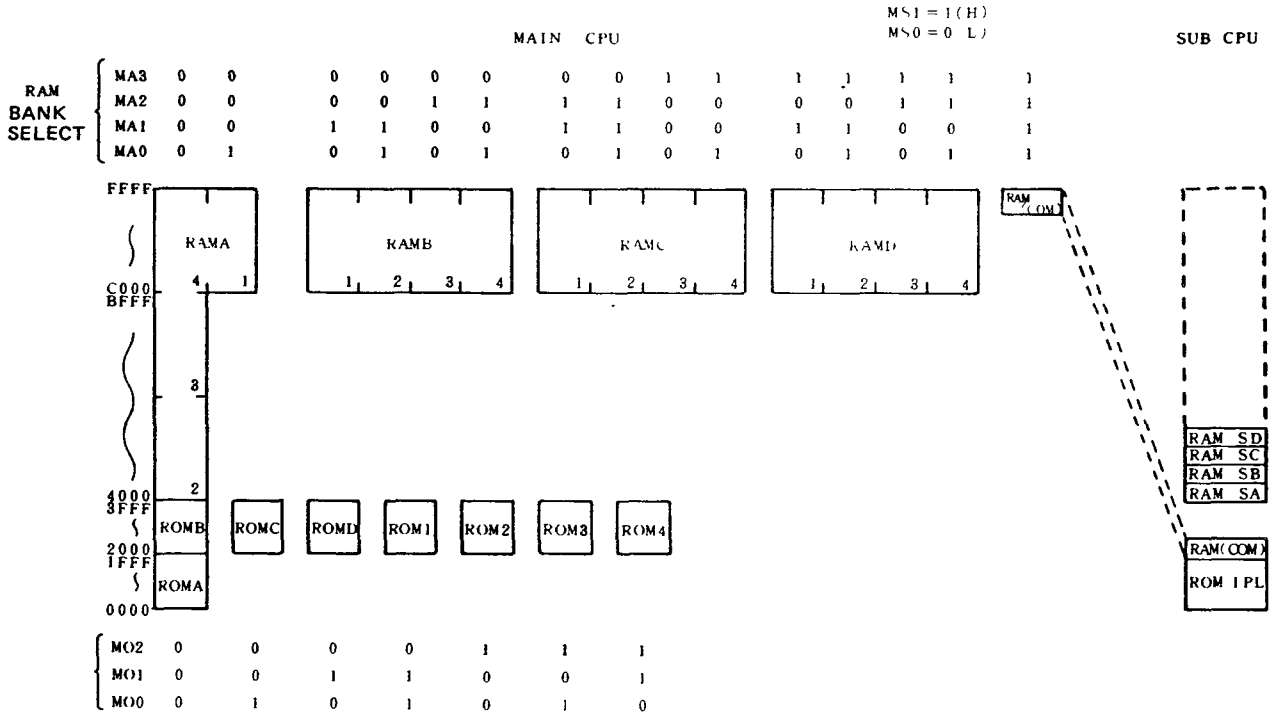
Communication between Main and SUB CPU





2.3. SD2 (ROM based BASIC)

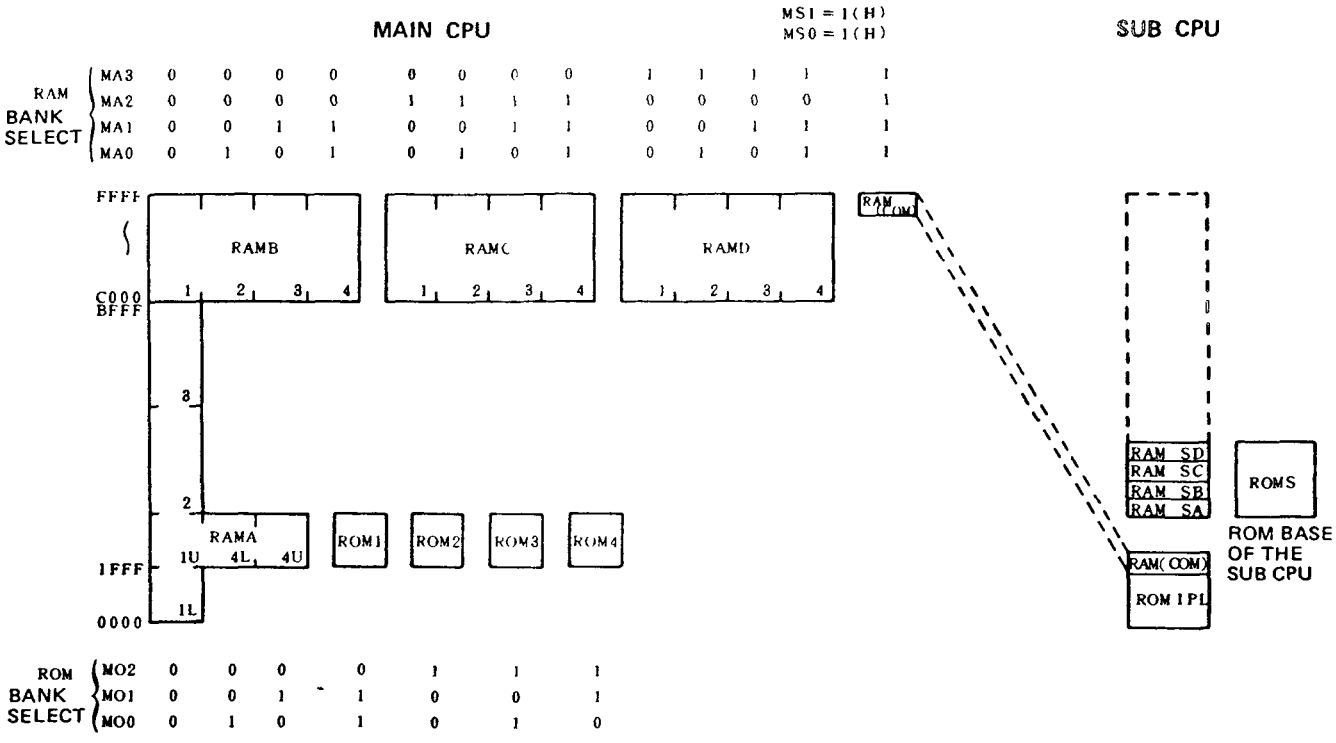
SD2 is active when "SHARP BASIC" is executed via ROM.



1. Bank select, MA0~MA3, is effective for memory area C000H-FFFFH.
2. Bank select, MO0~MA2, is effective for memory area 2000H-3FFFH

2-4. SD3 (RAM based BASIC)

SD3 is active when "SHARP BASIC" is ececuted via RAM.
"SHARP BASIC" is loaded in RAM from the floppy disk.



1. Bank select, MA0-MA3, is effective for memory area C000H-FFFFH.
2. Bank select, MO0-MO2, is effective for memory area 2000H-3FFFH.

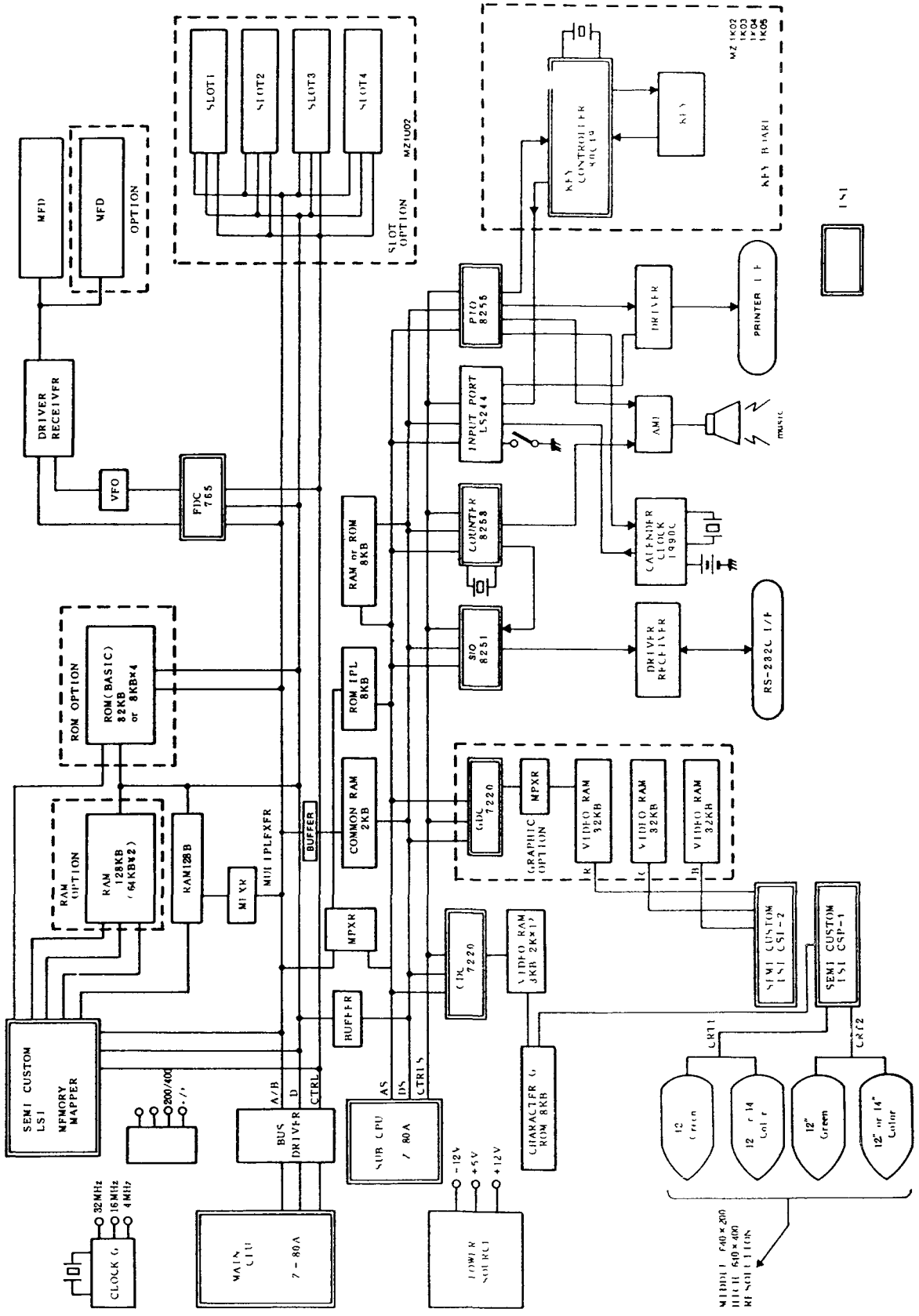
Operational description

The state of the system is determined by the bootstrap program before the load of the system program.

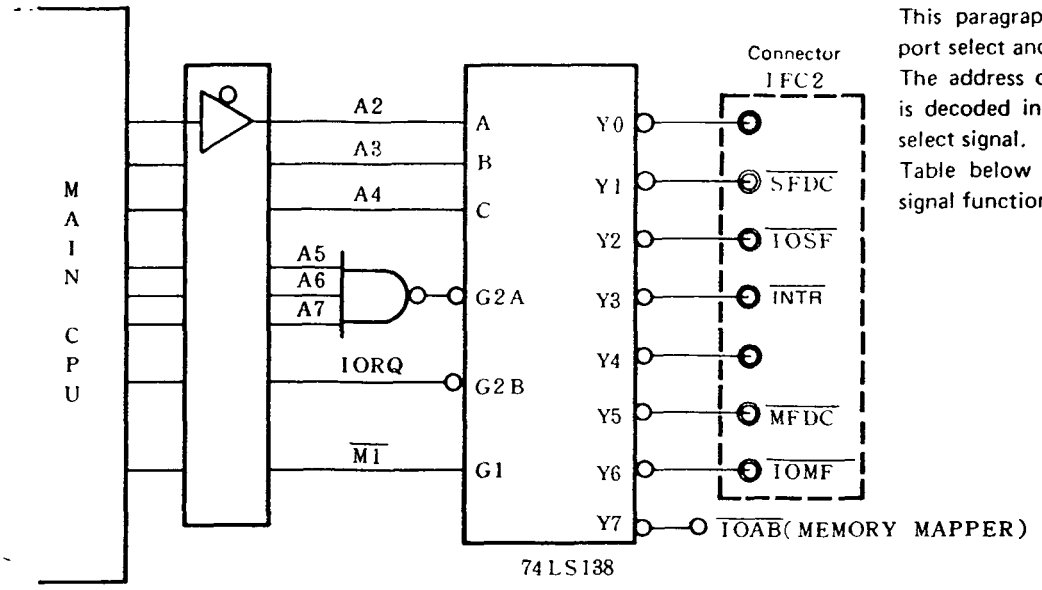
3. CPU AND MEMORY

3-1. Block diagram

1) Relation between MMR (Main Memory Mapper) and main memory.



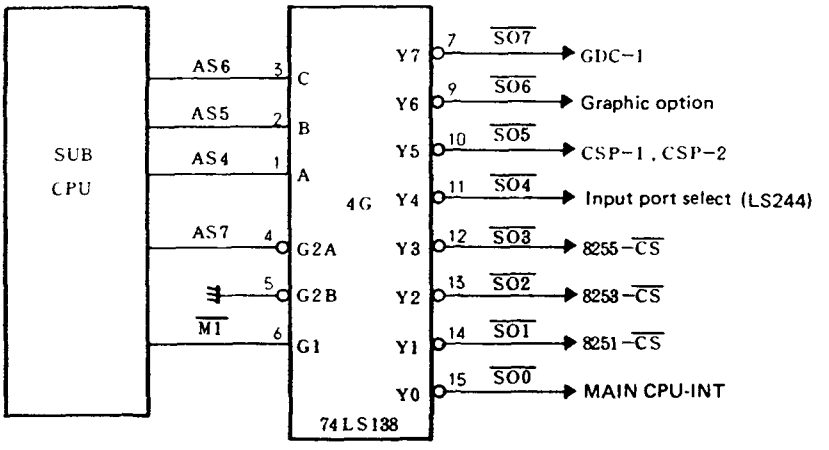
3-2. Main CPU and I/O port



This paragraph discusses main CPU I/O port select and addressing.
The address output from the main CPU is decoded in the 74LS138 to create the select signal.
Table below describes address map and signal functions.

ADDRESS								HEX	Signal name	Description
A7	A6	A5	A4	A3	A2	A1	A0			
0	0	0	0	0	0	0	0	00	NOT USE	
0	0	0	0	0	0	0	1	01		
				~				~		
1	1	0	1	1	1	1	0	DE		
1	1	0	1	1	1	1	1	DF		
1	1	1	0	0	0	X	X	E0 ~ E3	NOT USE	
1	1	1	0	0	1	X	X	E4 ~ E7	SFDC (UPD765)	SFD interface FDC chip select. A0 used for RD and WR. A1 is "don't care".
1	1	1	0	1	0	X	X	E8 ~ EB	IOSF	SFD interface I/O port and DMAC chip select.
1	1	1	0	1	1	X	X	EC ~ EF	INTR	Interrupt signal from the sub-CPU to the main CPU. Flipflop resetting signal.
1	1	1	1	0	0	X	X	F0 ~ F3	NOT USE	
1	1	1	1	0	1	X	X	F4 ~ F7	MFDC (UPD765)	MFD interface FDC chip select.
1	1	1	1	1	0	X	X	F8 ~ FB	IOMF	MFD interface I/O port. A0 used for RD and WR. A1 is "don't care".
1	1	1	1	1	1	X	X	FC ~ FF	IOAB (MEMORY MAPPER)	I/O port select in the memory mapper. A0 and A1 used during RD, WR.

3-3. Sub-CPU and I/O port



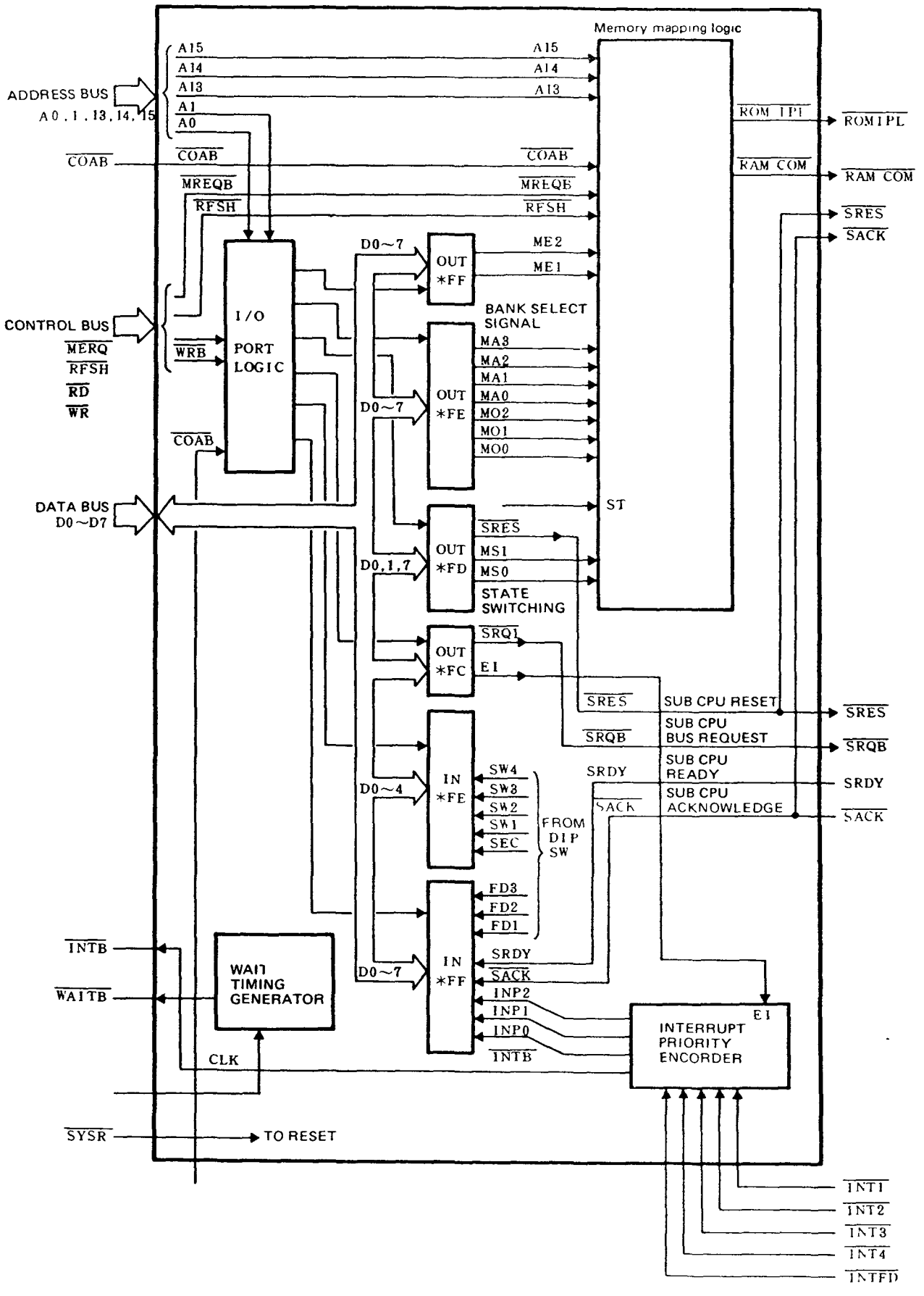
Shown at the left is the circuit used by the CPU to select the I/O ports. The output address from the sub CPU is decoded by the 74LS138 to create the select signal. Shown below is the address map and select signals.

lower / upper	AS 3210	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111	Signal description
AS 7654	MEX	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0000	0	←																Output signal to set the flipflop to apply interrupt (INTO) to the main CPU. Enables communication between CPU's.
0001	1	←																8251 SIO chip select. AS0 is used for data control selection. AS1, AS2, and AS3 are "don't care".
0010	2																	8253 counter chip select. AS0 and AS1 are used for programming during write. AS2 and AS3 are "don't care".
0011	3																	8255 PIO chip select. AS0 and AS1 are used for port/control selection. AS2 and AS3 are "don't care".
0100	4																	8-bit input port. Used for read. AS3 are "don't care".
0101	5																	CRT control I/O port chip select. AS1, AS2, and AS3 are used for write. AS0 is "don't care".
0110	6																	UPD7220 (graphic) chip select. AS0 is used for read and write. AS1, AS2, and AS3 are "don't care".
0111	7																	UPD7220 (character) chip select. AS0 is used for read and write. AS1, AS2, and AS3 are "don't care".
1000	8																	
1001	9																	
1010	A																	
1011	B																	
1100	C																	
1101	D																	
1110	E																	
1111	F																	

NOT USE

3-4. Memory mapper (MMR) SP6102R-001

1) Block diagram



2) Memory mapper (MMR) SP6102R-001 signal description

Pin No.	Polarity / Signal Name	IN/OUT	Function
1	ST	IN	Main CPU DRAM output buffer (LS244) switching strap.
2 ~ 9	D0 ~ D7	IN/OUT	Bidirectional main CPU data bus. (Data bus 0 ~ 7)
10 ~ 12	A15 ~ A13	IN	Main CPU address bus. Used in the memory mapping logic of the MMR for address output for the DRAM, ROM, and shared RAM. (Address bus 13 ~ 15)
13	A1	IN	Main CPU address bus. Used in the I/O port select logic of the MMR to assign device number.
14	$\overline{SRES}$	OUT	Sub-CPU bus request signal. • After power on: Halts the sub-CPU. • After write command (LDA-80H: OUT#FD) by the main CPU: Starts the sub-CPU. This signal is issued after transfer of the main CPU program contained in the ROM-IPL. (Sub CPU Reset)
15	$\overline{SRQ}$	OUT	Sub-CPU bus request signal. • After power on: Resets bus request to sub-CPU. • After write command (LDA-02H: OUT#FC) by the main CPU: Place bus request to the sub-CPU This signal is issued to bus of the sub-CPU, after the main CPU writes to the shared RAM a command parameter to the sub-CPU or reads the message status from the sub-CPU. (Sub CPU Request)
16 ~ 18	AR13 ~ AR15	OUT	Address signal to the main CPU dynamic RAM. The main CPU address signals A13-A15, merged in the memory mapping logic circuit to produce AR13-AR15. This is means by which the 4 basic and CP/M memory maps are made, along with MS1 and MS0.
19	$\overline{R32}$	OUT	BASIC interpreter 32KB mask ROM chip select signal. Valid when SD2 is active (Sharp ROM based BASIC). Command (LDA 02H OUT 3FD) (ROM 32K select)
20	$\overline{IOAB}$	IN	Internal MMR I/O port select logic signal. Goes low by the command IN/OUT #FC-#FF. (Input/Output Address)
21	SRDY	IN	Input of ready signal from the sub-CPU. (Sub CPU Ready)
22	$\overline{ROPB}$	OUT	Chip select signal issued from the main CPU to the 8KB mask ROM. Valid with SD0 active (initialize state). (ROM ipl)
23 ~ 26	$\overline{ROAB}$ ~ $\overline{RODB}$	OUT	Chip select signal for four chip BASIC interpreter 8KB EPROM (A, B, C, D). Valid with SD2 active (Sharp ROM based BASIC). *$\overline{R32B}$ (alternate choice with the 32KB mask ROM chip select signal). (ROM A~D Buffer)
27 ~ 30	$\overline{RSAB}$ ~ $\overline{RSDB}$	OUT	Row address select signal for the main CPU dynamic RAM (block A-block D). $\overline{RAS}$ (ROW ADDRESS SELECT; LINE ADDRESS SELECT) SIGNAL (Row address Select)
31	$\overline{SACK}$	IN	Input of bus acknowledge signal from the sub-CPU. (When the main CPU must write a command in the shared RAM a bus request is issued first, then the command is written in the shared RAM after acknowledgement from the sub-CPU At the end of the command cycle bus request is released and the sub CPU executes the command)

Pin No.	Polarity / Signal Name	IN/OUT	Function
32	$\overline{RF1B}$	OUT	Main CPU 128KB dynamic RAM output buffer (LS244) output enable signal. (RAM buffer 1)
33	$\overline{RF2B}$	OUT	Signal identical to $\overline{RF1B}$ For option RAM (RAM buffer 2)
34	$\overline{WATB}$	OUT	Wait signal to the main CPU (One wait cycle is applied during the memory fetch cycle of the main CPU. It consists of one clock period) (WAIT)
35	$\overline{RCMB}$	OUT	Chip select signal issued from the main CPU to select the RAM shared by the main CPU and the sub-CPU (RAM Common)
36	$\overline{ITFB}$	IN	Interrupt input from the UPD765 FDC (Floppy Disk Controller). (Interrupt from Floppy)
37	$\overline{IT0B}$	IN	Interrupt input from the sub-CPU. (Interrupt from No. 0)
38 ~ 39	$\overline{IT1B}$ ~ $\overline{IT2B}$	IN	Interrupt input from slot 1 or 2. (Interrupt from No. 1, 2)
40	$\overline{MRQB}$	IN	Memory request signal from the main CPU. (Memory Request)
41	$\overline{WRB}$	IN	Write signal from the main CPU. (Write)
42 ~ 43	$\overline{IT3B}$ ~ $\overline{IT4B}$	IN	Interrupt input from slot 3 or 4. (Interrupt from No. 3, 4)
44	SEC	IN	Input from the FDD (Floppy Disk Drive) assignment dip switch (A), No. 1. *See the dip switch description, provided separately. (Section)
45	GND	IN	Ground
46	Vcc	IN	5V supply
47 ~ 48	SW1 ~ SW2	IN	Input from the system assignment dip switch. *See the dip switch description, provided separately.
49	A0	IN	Main CPU address bus Used in the I/O port select logic in the MMR to designate device number.
50	$\overline{RFSH}$	IN	Refresh signal from the main CPU. (Refresh)
51 ~ 52	SW3 ~ SW4	IN	Input from the system assignment dip switch. *See the dip switch description, provided separately.
53	GND	IN	Ground
54	FD1	IN	Input from the system assignment dip switch. *See the dip switch description, provided separately.
55	Vcc	IN	5V supply.
56	FD2	IN	Input from the FDD assignment dip switch (A), No. 2. *See the dip switch description, provided separately.

Pin No	Polarity Signal Name	IN/OUT	Function
57	SYSR	IN	System reset signal. Used to reset I/O port in the MMR. (System Reset)
58	FD3	IN	Input from the sytem assignment dip switch. *See the dip switch description, provided separately.
59	$\overline{\text{COAB}}$	IN	Shared RAM select signal. Address of the shared RAM is #F800-#FFFF for the main CPU (Common RAM Address)
60	$\overline{\text{RO1B}}$	OUT	Select signal for 8KB area allocated to slot 1. Valid when SD2 is active (ROM based BASIC) and SD3 (RAM based BASIC) (ROM 1)
61	GND	IN	Ground
62	Vcc	IN	5V supply
63 64	$\overline{\text{RO2B}}$ $\overline{\text{RO3B}}$	OUT	Select signal for 8KB area allocated to slot 2 or 3. Valid when SD2 is active (ROM based BASIC) and SD3 (RAM based BASIC). (ROM2, 3)
65	$\overline{\text{RDB}}$	IN	Read signal from the main CPU. (Read)
66	CLK		EAIT signal generation clock. (Clock)
67	$\overline{\text{RO4B}}$	OUT	Select signal for 8KB area allocated to slot 4. Valid when SD2 or SD3 (RAM based BASIC) are active. (ROM 4)
68	MPX	OUT	RAS/CAS address switching signal for the main CPU DRAM. High: Row address Low: Column address (Multiplex)
69	GND	IN	Ground
70	$\overline{\text{CASB}}$	OUT	$\overline{\text{CAS}}$ (Column Address) signal for the main CPU 64K DRAM. *Refresh for the RAM only. (Column Address Select Buffer)
71	GND	IN	Ground
72	$\overline{\text{INTB}}$	OUT	Interrupt signal to the main CPU. (Interrupt)
73			Not used

MAIN CPU
I/O PORT IN MEMORY MAPPER

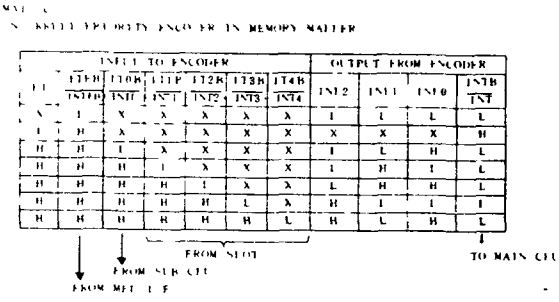
ADDRESS								HEX	DBUS	I/O		
A7	A6	A5	A4	A3	A2	A1	A0					
1	1	1	1	1	1	0	0	FC	D1	OUT	SRQB	SRQ Bus request from the main CPU to the sub-CPU
									D0		☆	
1	1	1	1	1	1	0	1	FD	D7	OUT	SRES	Sub-CPU reset signal
									D1		MS1	Memory system define
									D0		MS0	
1	1	1	1	1	1	1	0	FE	D7	OUT	MA3	Bank select signal to memory area of C000-FFFF.
									D6		MA2	
									D5		MA1	
									D4		MA0	
									D2		MO2	Bank select signal to memory area of 2000-3FFF.
									D1		MO1	
									D0		MO0	
									D4	IN	SW4	System assign switch (SW8)
									D3		SW3	
									D2		SW2	
									D1		SW1	
									D0		SEC	FD assign
1	1	1	1	1	1	1	1	FF	D7	IN	FD3	
									D6		FD2	
									D5		FD1	
									D4		SRDY	Sub-CPU READY signal
									D3		SACK	Sub-CPU acknowledge signal
									D2		INP2	Interrupt status
									D1		INP1	
									D0		INP0	
									D7	OUT	MF2	#1
									D6		ME1	

1. All output signals are reset to low level upon power on, except for SRBQ that goes high.
2. Noted with a star mark "☆" are input/output signals, and rest of others are processed in the LSI.

#1 I/O port output of ME1 and ME2 uses the memory at the addresses.

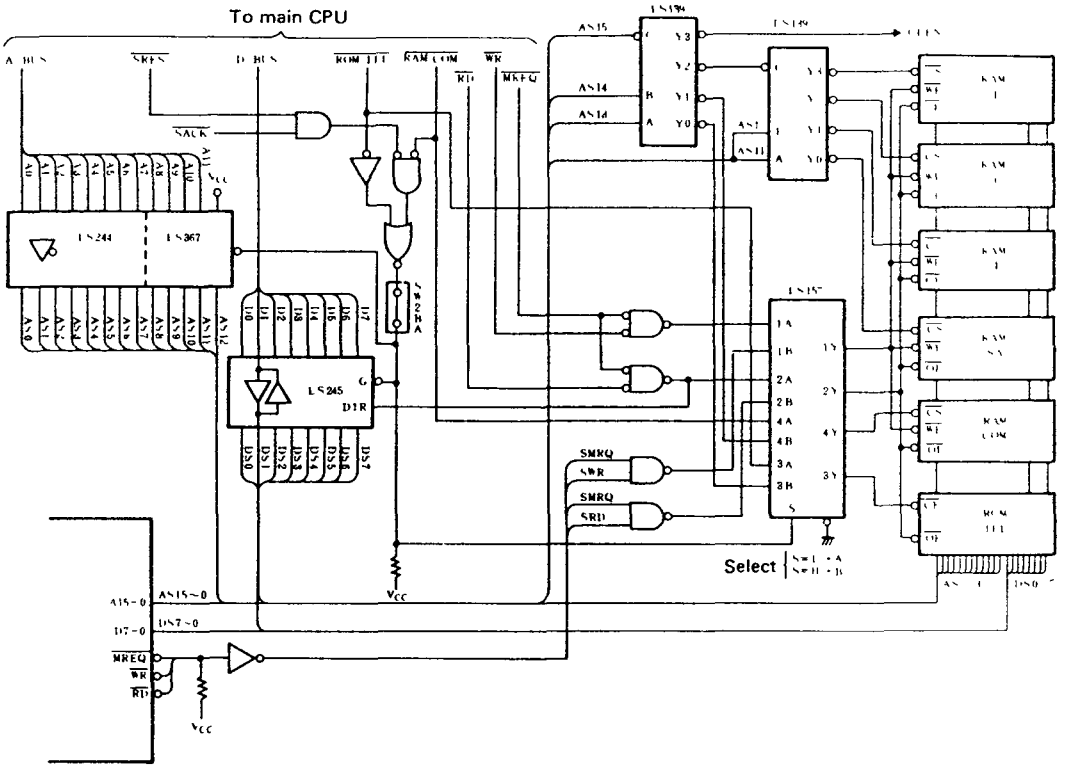
{ ME2 → 8000 ~ BFFF
{ ME1 → 4000 ~ 7FFF

When ME1 and ME2 are in high state, RSAB ($\overline{\text{RASA}}$) is inhibited during memory addresses in RAM-A that correspond to overlayed addresses for ME1 and ME2 This is not true during SD1 mode.



Wait timing generator
WAIT is issued once per main CPU fetch cycle.
Its outut is tri state

3-5. Memory (ROMIPL, RAMCOM, S-RAM) select circuit



1) ROM-IPL select by the main CPU

As $\overline{\text{ROM IPL}}$ turns to low level after power on address bus buffers (LS244, LS367) and data bus buffer (LS245) are enabled. S of the data selector IC (LS157) is set to a low level to enable input 1A-4A. The 3Y and 2Y outputs of the LS157 then go low so that $\overline{\text{CE}}$ and $\overline{\text{OE}}$ of the ROM-IPL are from main CPU. The contents of the IPL-ROM are then read by the main CPU. Because the input pin (#16) of the address buffer (LS367) is connected to Vcc, IPL for the main CPU will be at address 1000 of the IPL-ROM. Switch SW2BA is the operation test dip switch which should be ON at all times.

2) RAM-COM select by the main CPU

When $\overline{\text{RAM COM}}$ is low, $\overline{\text{SRES}}$ high, and $\overline{\text{SACK}}$ low, the select input S of the selector IC (LS157) is in low state so that input 1A-4A becomes effective. That is, the output 4Y is low and either 1Y (WE) or 2Y (OE) becomes low level, so as to enable to read or write RAM-COM.

3) ROM-IPL select by sub-CPU

Normally, the select signal S of the selector is pulled up to Vcc level that inputs 1B-4B are enabled by sub CPU. If A13 thru A15 were to be at low level, the output Y0 of the LS139 becomes low level so that the output 3Y of the LS147 or $\overline{\text{CE}}$ of the ROM-IPL should be at low level. Should $\overline{\text{SRD}}$, $\overline{\text{SMRQ}}$ be at low lebel as well, the output 2Y of the LS157 or $\overline{\text{OE}}$ of the ROM-IPL turnde to low lebel to read the ROM-IPL. Though the sub-CPU can access an address range of 0000 to 1FFF theoretically, it would be from 0000 to 0FFF, actually.

4) RAM-COM select by sub-CPU

Y1 of the LS139 changes to low level when AS13 is high and AS14 and AS15 are low. In other words, the input 4B of the LS157 is at low level which brings the output Y4 to low level, so that CS of the RAM-COM chip select signal should become effective.

If $\overline{\text{SMRQ}}$, $\overline{\text{SRD}}$ or $\overline{\text{SMRQ}}$, $\overline{\text{SWR}}$ is in low level at this point, it enables read ($\overline{\text{OE}}$) or write ($\overline{\text{WE}}$). Address range, however, is 2000 to 3FFF

5) RAM (SA, SB, SC, SD) select by sub-CPU

$\overline{\text{SMRQ}}$, $\overline{\text{SRD}}$ ($\overline{\text{OE}}$) or $\overline{\text{SMRQ}}$, $\overline{\text{SWR}}$ ($\overline{\text{WE}}$) is at low level to select the sub-CPU dedicated RAM, SA-SD. Tne following chip select signal, then becomes valid under these conditions:

RAMSA . . $\overline{\text{AS11}}$, $\overline{\text{AS12}}$, $\overline{\text{AS13}}$, AS14, $\overline{\text{AS15}}$
(address 4000-47FF)

RAMSB . . AS11, $\overline{\text{AS12}}$, $\overline{\text{AS13}}$, AS14, $\overline{\text{AS15}}$
(address 4800-4FFF)

RAMSC . . $\overline{\text{AS11}}$, AS12, $\overline{\text{AS13}}$, AS14, $\overline{\text{AS15}}$
(address 5000-57FF)

RAMSD . . AS11, AS12, $\overline{\text{AS13}}$, AS14, $\overline{\text{AS15}}$
(address 5800-5FFF)

4. CRT DISPLAY

4-1. Specification

		Use of high resolution CRT	Use of medium resolution CRT
Display memory		3KB (characters) 96KB, max (graphic) Option	←
Character display	Screen structure	80 chrs x 25 lines, 80 chrs x 20 lines 40 chrs x 25 lines, 40 chrs x 20 lines	←
	Programmable	8 x 16 dots With lower case descenders	8 x 8 dots
	Character structure	255 characters Alphanumerics and 69 symbols 26 small characters 97 graphic patterns	←
	Attributes	Revers, vertical line, blink, horizontal line Programmable for each character	Blink, revers Programmable for each character.
	Colors	8 colors, programmable for each character	←
Graphic display (option)	32KB type	640 x 400 dots, B/W (one frame) Color designation for each character	640 x 200 dots, B/W (Two frames) Color designation possible for each character
	96KB type	640 x 400 dots, B/W (three frames) Color designation possible for each character Color (one frame)	640 x 200 dots, B/W (six frames) Color designation possible for each character Color (Two frame)
	Screen merge	Merge any graphic screen (1 to 3 frames)	
Merge of chracters and graphics		Merge a character screen with a graphic screen	
Background color		Choice of 8 colors	
Control of two independent screens		Possible to display on separate two screens original graphic screen and character screen Separate graphic screens can be merged into one Possible to affix attributes (CRT2 only) Selection of character/non-character screen display	
Control channel number		Incorporation of two independent video outut channels	
Light pen input (option)		Scans coordinates and character code	

Summary of video display specification

Table 1

Function \ Type of monitor		High resolution CRT (640 x 400 dots mode)				Medium resolution CRT (640 x 200 dots mode)			
		Green monitor		Color monitor		Green monitor		Color monitor	
		Characters	Graphics (option)	Characters	Graphics (option)	Characters	Graphics (option)	Characters	Graphics (option)
		ASCII	B/W	ASCII	Color	ASCII	B/W	ASCII	Color
Elements		8 x 16 8 x 20		8 x 16 8 x 20		8 x 8 8 x 10		8 x 8 8 x 10	
Character structure		5 x 14		5 x 14		5 x 7		5 x 7	
Screen structure (Characters x lines)		80 x 25 mode 80 x 20 mode 40 x 25 mode 40 x 20 mode	640 x 400 dot	80 x 25 80 x 20 40 x 25 40 x 20	640 x 400	80 x 25 80 x 20 40 x 25 40 x 20	640 x 200	80 x 25 80 x 20 40 x 25 40 x 20	640 x 200
Color designation	Basic			By character				By character	
	Option I (48KB)			↑	By character			↑	By dot
	Option II (96KB)			↑	By dot			↑	↑
Small letter descenders		O		O		X		X	
Line creation		O		X		X		X	
Display memory		3KB	32KB	3KB	32KB (I), 96KB(II)	3KB	16KB	3KB	48KB
Frames	Basic	1 frame	No frame	1 frame	No frame	1 frame (1 page)	No frame	1 frame (1 page)	No frame
	Option I (48KB)	↑	1 frame	↑	1 frame	↑	3 frames	↑	1 frame
	Option II (96KB)	↑	3 frames	↑	1 frame	↑	6 frames	↑	2 frames
Screen overlay	Basic	Not possible		←		←		←	
	Option I (48KB)	One character screen against one graphic screen		One character screen against one graphic screen		One character screen against three graphic screens		One B/W character screen against three graphic screens One color character screen against one graphic screen	
	Option II (96KB)	One character screen against three graphic screens		One B/W character screen against three graphic screens One color character screen against one graphic screen		'		'	

NOTE Graphics option

1) Character display

1.1. Screen structure

CRT used / Character	High resolution CRT (640 x 400 dot) fH = 20.9KHz (New)fV = 47.3Hz	Medium resolution CRT (640 x 200 dot) fH=15.7KHz fV = 60Hz
ASCIL	80 x 25 lines 80 x 25 lines 40 x 25 lines 40 x 20 lines	←

Dip switch in the main unit is used to select assignment of high resolution/medium resolution CRT.
Display mode must be chosen by programming.

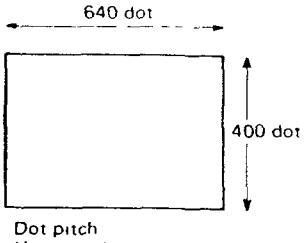
1-2. Character structure and picture elements

	640 x 400		640 x 200	
	Elements	Structure	Elements	Structure
ASCII	8 x 16 8 x 20	5 x 14	8 x 8 8 x 10	5 x 7
Graphic symbol	↑	8 x 16	↑	8 x 8
	Small letter descenders and line creating functions are available.		Small letter descenders and line creating functions are not available.	

NOTE: In the case of 8 x 8 and 8 x 16 picture elements, vertically adjoining graphic symbols will joint together in the 25-line mode.
As for character structure of 6 x 14, 7 x 14, 6 x 7, or 7 x 7, decision must be given on an actual dot pattern.

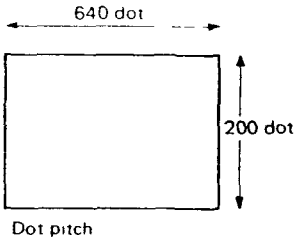
2) Graphic display (option)

(High resolution CRT)



Dot pitch
Horizontal vertical = 1 1

(Medium resolution CRT)



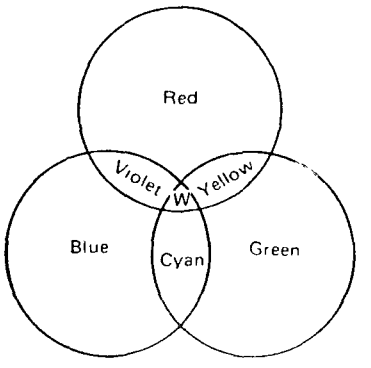
Dot pitch
Horizontal vertical ≒ 1 : 2

3) Color designation

Eight colors are usable (white, yellow, cyan, green, violet, red, blue, black)
Color designation

		640 x 400 dot	640 x 200 dot
ASCII		By character	By character
Graphics	48K byte	By character	By dot
	96K byte	By dot	By dot

Background color
8 colors for designation



W White

Three basic colors

4) Attribute

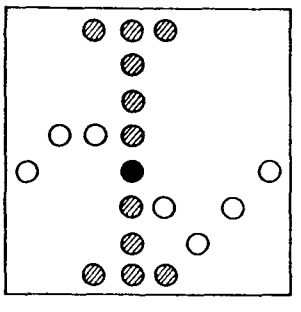
	B/W	Color
AT1	Vertical line	B
AT2	Horizontal line	R
AT3	Reverse	G
AT4	Blink	Blink

Designated for each character.

Line and character may exist in the same element (Line may also be displayed on the 80 characters x 25 lines screen.)

5) Screen overlay

It will be possible to have an overlaid screen that consists of one character (screen and a maximum of three graphic screens. (For detail of overlay screen, refer to Table 1.)
In the color mode, if there are two colors in the same screen and other designated for a dot on the graphic screen element — the one designated for a character on the character — both colors will be merged altogether to produce image.



(Red)
Dot color designated by character attribute

(Blue)
Dot color designated by graphic dot.

(Violet)
Dot composed of more than two color designations.

6) Screen overlay and displaying on two independent CRT's

As there are two video output channels it will be possible to display two independent screens on separate video display unit Overlay is possible on either of screens (See preceding item 5)) The following bit selection is needed for screen overlay

	Address				Data			Internal	
	Hex	AS 3	AS 2	AS 1	AS 0	DS 2	DS 1	DS 0	S gnal name of CSP	Function
CSP 1	50	0	0	0	0			1	ECH1	Choice of outputting the character screen on CRT1 0 No 1 Yes
							1		ECH2	Cho ce of outputting the character screen on CRT2 0 No 1 Yes
						1			EAT2	Choice of whether attribute or cursor be put on the frame that displayed on CRT2 (0 No 1 Yes)
	51	0	0	0				1	SR1	Displays on CRT1 the blue elements contained in the VRAM
							1		SR2	Displays on CRT1 the red elements contained in the VRAM
						1			SR3	Displays on CRT1 the green elements contained in the VRAM
	52	0	0	1	0			1	SR4	Displays on CRT2 the blue elements contained in the VRAM
							1		SR5	Displays on CRT2 the red elements contained in the VRAM
						1			SR6	Displays on CRT2 the green elements contained in the VRAM
	53	0	0	1	1			1	BGC B	} Choice of background color display
							1		BGC R	
						1			BGC G	
	54	0	1	0	0			1	COLOR	Color mode
							1		BODER	Border color mode in effect
						1				
	55 (5D)	0	1	0	1			1	08/16	Defines the data size for the graphic RAM (0 8 bits, 1 16 bits)
							1		40/80	Defines display digits for the character screen
						1				(0 40 digits 1 80 digits)
	56	0	1	1	0			1	RA-400	Connection of a 400 raster CRT
							1		V RAM2	Connection of the 96K bytes VRAM
						1			V RAM1	Connection of graphio GDC
	57	0	1	1	1			1	25/20	25 lines/20 lines switching (0 25 lines, 1 20 lines)
							1			
						1				
CSP 2	5D	1	1	0	1			1	08/16	Defines data size for the graphic RAM (0 8 bits 1 16 bits)
							1		40/80	Defines display digits for the character screen
						1				(0 40 digits, 1 80 digits)

NOTE Both CRT1 and CRT2 must be high resolution CRT's (640 x 400) or medium resolution CRT's (640 x 200) Output to each CRT may be possible in the following combination .

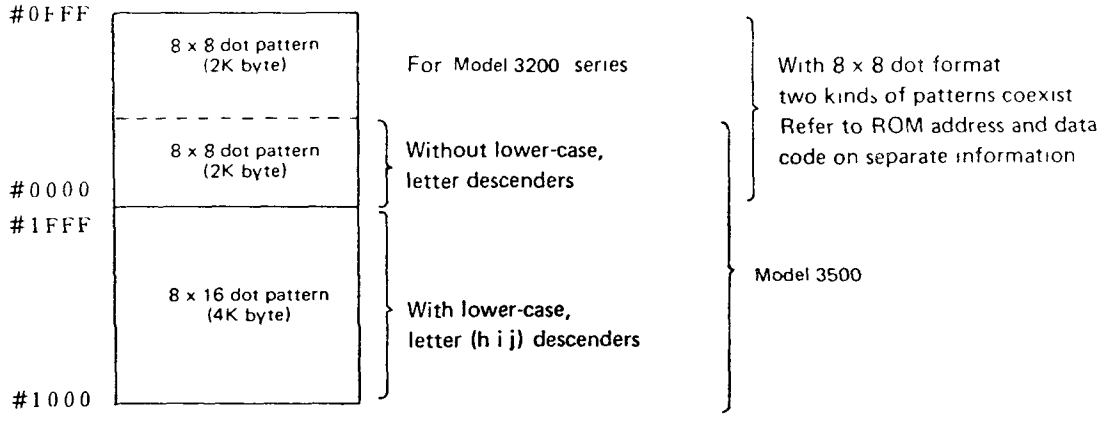
Output to each CRT may be possible in the following

CRT1	CRT2
CH(AT)	CH(AT)
GF(AT)	GF AT)
CH AT)+GF (AT)	CH(AT)+GF AT
	CH
	GF
	CH+GF

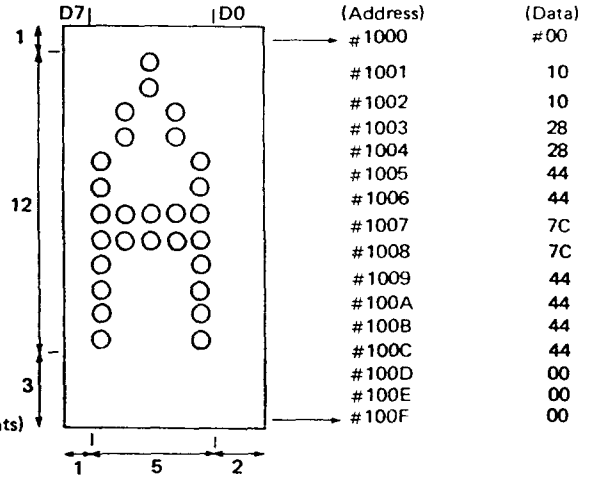
CH ASCII
GF Graphic screen, including overlay of two graphics screens
(AT) Attached with attribute

7) ASCII CG

Uses an 8KB MROM contains two patterns:
640 x 400 dots (8 x 16 dots) and 640 x 200 dots (8 x 8 dots)



☆ Address and pattern in picture element



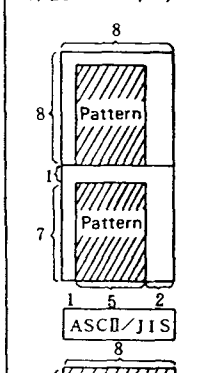
(Address)	(Data)
#1000	#00
#1001	10
#1002	10
#1003	28
#1004	28
#1005	44
#1006	44
#1007	7C
#1008	7C
#1009	44
#100A	44
#100B	44
#100C	44
#100D	00
#100E	00
#100F	00

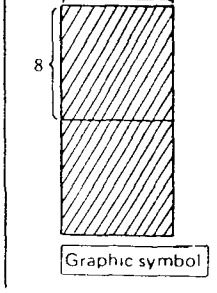
(Example of 5 x 12 dots pattern for 1 x 16 elements)

8) Element structure, character structure, and line

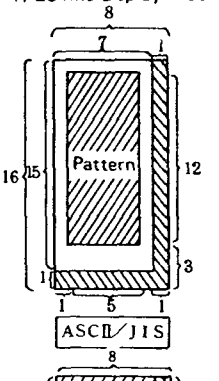
Element structure, character structure, and line
/ – Character pattern area
\ – Line area
× – Area where pattern and line are overload

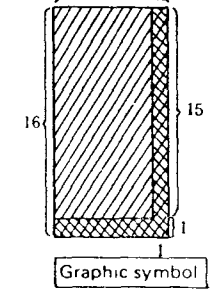
640 x 200 dot	640 x 400 dot
1) 25 line display mode	1) 25 line display mode





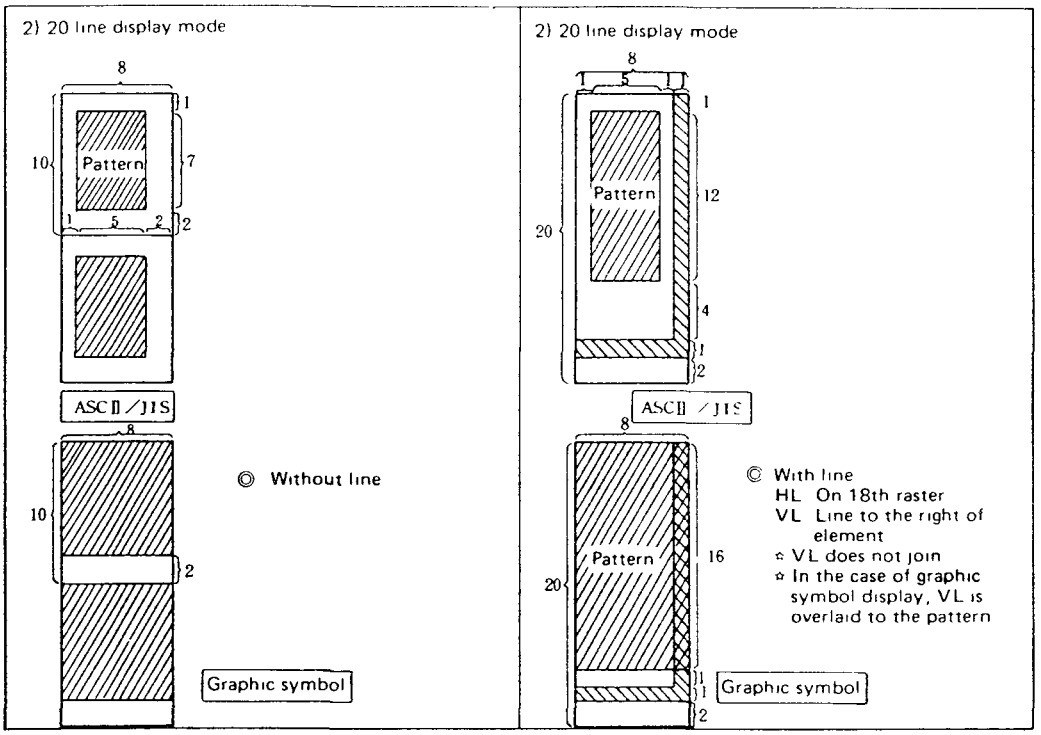
◎ Without line





◎ With line
HL On 16th line
VL Line ot the right of element

☆ In the case of graphic symbol display
☆ Both HL and VL are overlaid to the pattern



9) Cursor

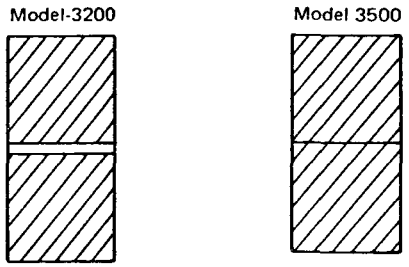
Sharp of the cursor: Same as seen in Model 3200
Reverse and blink)

10) Light pen input

Incorporates the light pen input connector and its interface. The light pen, however, is an option.
Accuracy: By each character
Function: Coordinates/character code

11) Difference in specification with that of Model 3200

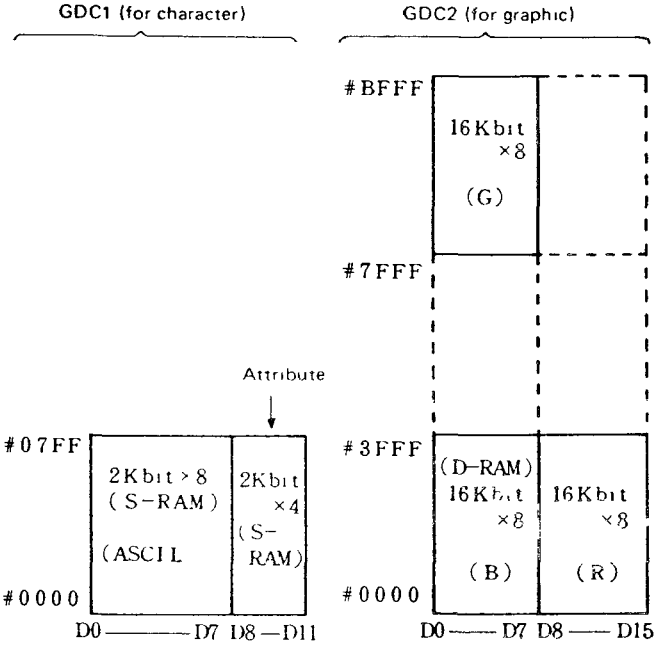
(1) There are two modes for the Model 3200; normal mode (6 x 9 elements) and graphic mode (6 x 8 elements). In the normal mode of 25-line displaying of the PC-3200, vertically adjacent graphic symbols do not joint. But, they will joint with the Model 3500.



(2) No line will be displayed for the medium resolution CRT (640 x 200 dot).
It is possible to display line on the high resolution CRT, compatible to line the utilizing program of the Model 3200

4-2. Video RAM

1) Structure of VRAM



Solid line 48KB option
Broken line. To be added to comprise the 96KB option.

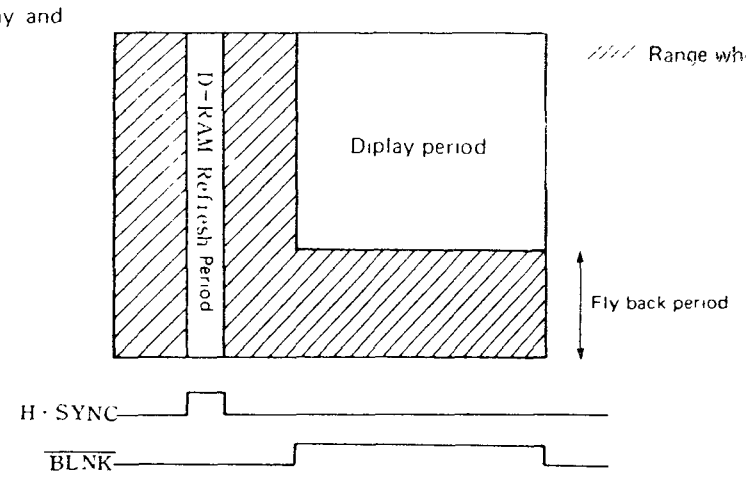
VRAM capacity
Basic 3KB (including attibutes)
Graphic option 1: 48KB
Graphic option 2 96KB

Bit structure of VRAM

CRT		640 x 400 dot	640 x 200 dot
Character VRAM		8 bit / word	8 bit / word
Graphic V RAM	48 KB	16 bit / word	8 bit / word
	96 KB	16 bit / word	16 bit / word

2) Read/write from Z 80 to VRAM

(1) Timing period for display and V-RAM Read/write.

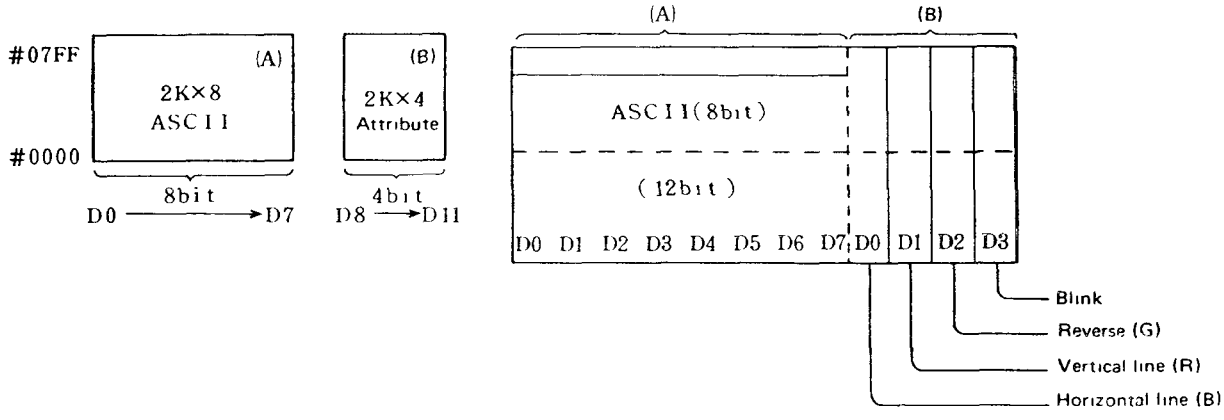


//// Range where GDC can draw.

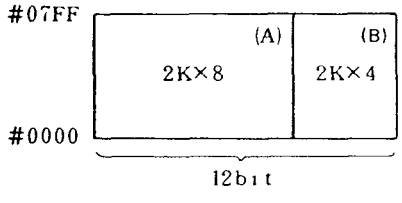
(2) Timing that the Z-80 can read/write VRAM
The Z-80 can read/write VRAM when GDC FIFO buffer is either empty or Full, and can be accessed by refreshing during the display period. Number of characters that can be read/write within one raster in any mode.

3) Structure of character VRAM

(1) When read/write from GDC

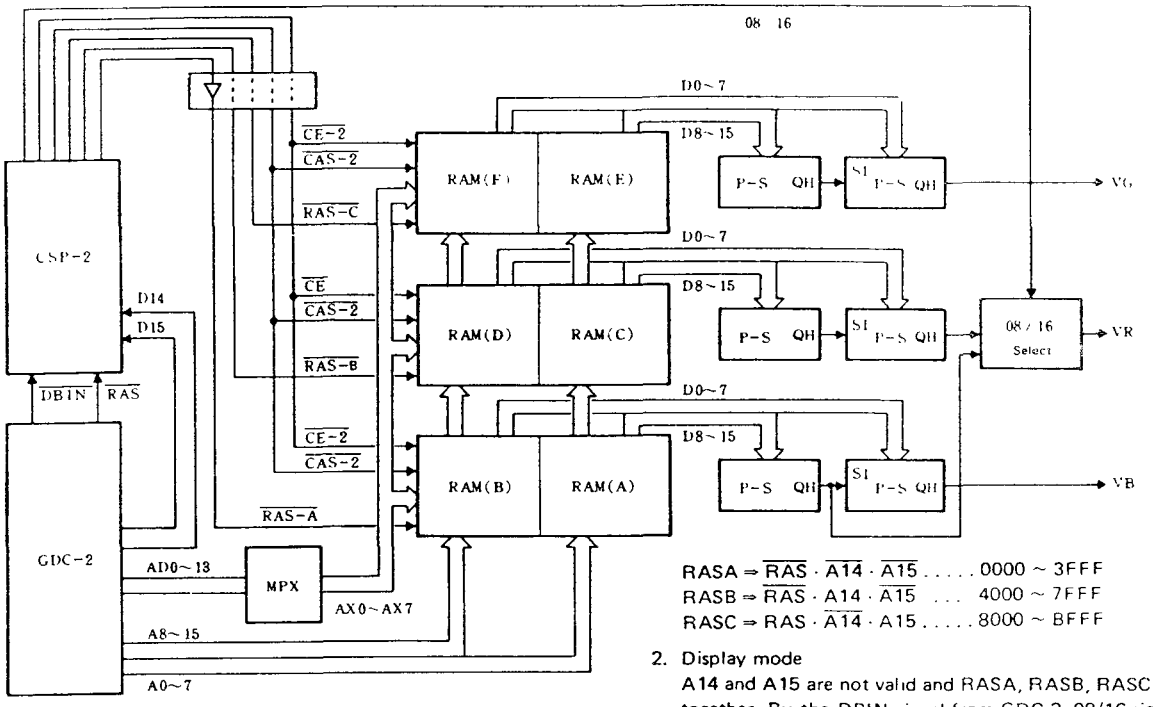


(2) During display



4) Graphic VRAM memory (MZ1R03)

● Block Diagram



RASA ⇒ $\overline{RAS} \cdot \overline{A14} \cdot \overline{A15}$ . . . . . 0000 ~ 3FFF
RASB ⇒ $\overline{RAS} \cdot A14 \cdot \overline{A15}$ . . . 4000 ~ 7FFF
RASC ⇒ $RAS \cdot \overline{A14} \cdot A15$ . . . . . 8000 ~ BFFF

1. read/write Mode
The select signal RASA, RASB and RASC are generate from RAS, A14 and A15 which is signal of GDC-2.
The address is allocated to each area selected by above signal.

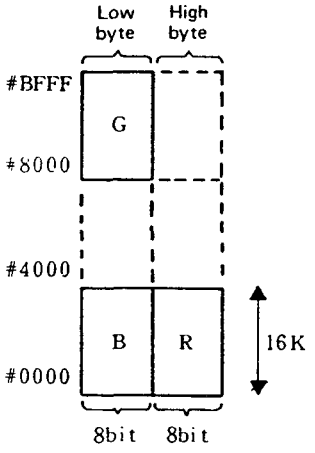
2. Display mode
A14 and A15 are not valid and RASA, RASB, RASC are selected together. By the DBIN signal from GDC-2, 08/16 signal is generated by CSP-2.
The signal of 08/16 select, after P-S conversion for RAMA, RAMB output signal then output to VB by serial signal, or sprit the signal to VB and VR.
(08/16 select: 08 for 200 rasters, 16 for 400 rasters)

Read/write by Z-80 via the GDC

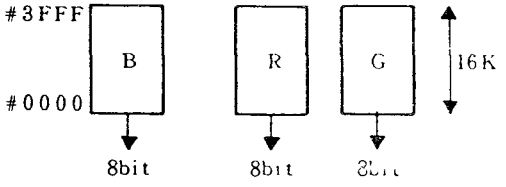
During displaying

(1) 640 x 200 dots display mode

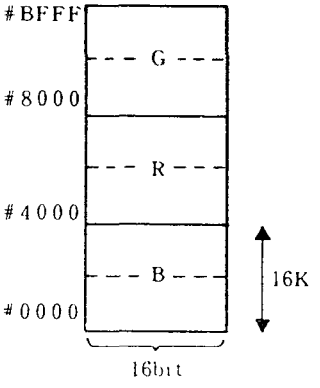
Option I
(48K byte)
8bit structure



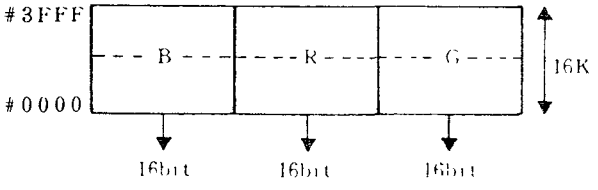
B/W: 3 frames
Color: 1 frame



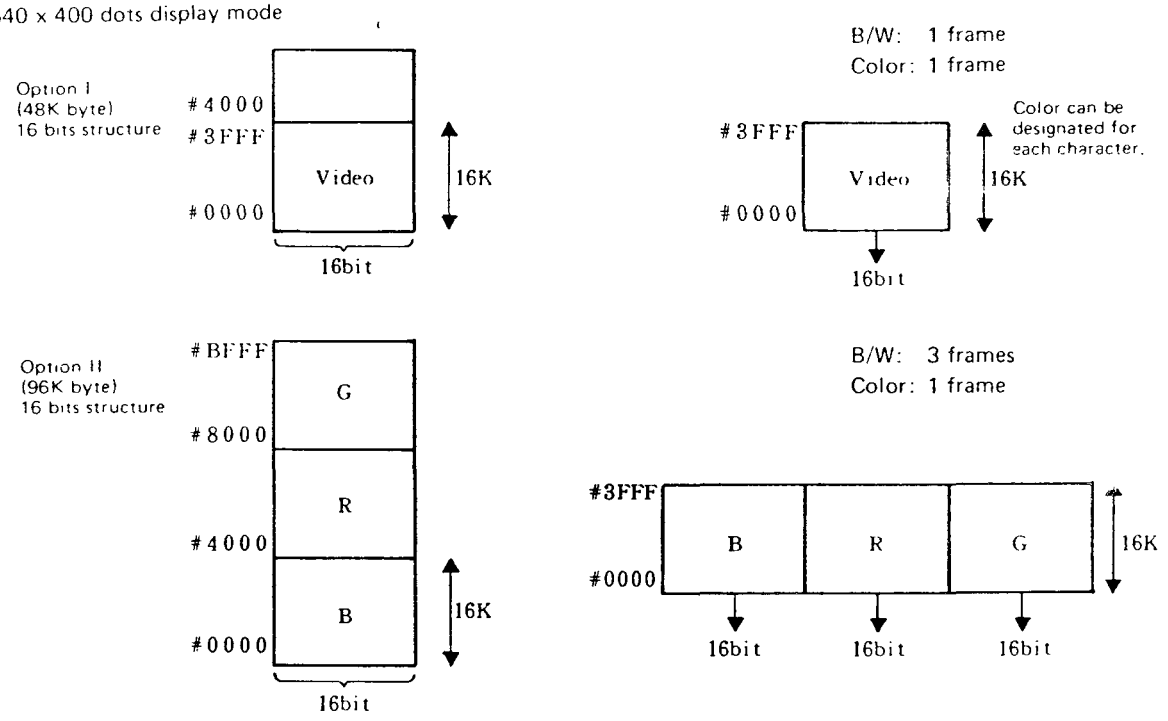
Option II
(96K byte)
16bit structure



B/W: 6 frames
Color: 2 frames



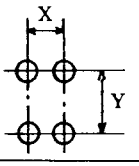
(2) 640 x 400 dots display mode



5) Synchronize signal timing

(1) For 640 x 200 dots display mode

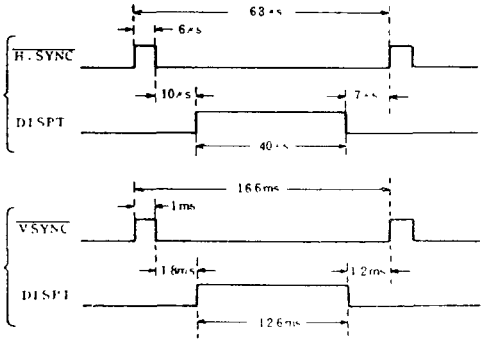
fH = 15.87kHz
fV = 60 Hz



X : Y ≒ 1 : 2

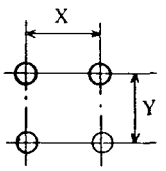
	GDC-1 (80 digits) Character display (40 digits)	GDC-2 (graphic) 8 bits	GDC-2 (graphic) 16 bits
Dot clock (0D)	(16MHz) (8MHz)	16MHz	16MHz
2XCCLK	(4MHz) (2MHz)	4MHz	2MHz
Horizontal display time	40μs	←	←
HFP	7μs	← (14 Chr.)	10μs
HS	6μs	(12 Chr.) (tREF=0.8ms)	5μs (tREF=1.6ms)
HBP	10μs	← (20 Chr.)	8μs
Vertical display time	12.6ms	←	←
VFP	1.2ms	←	←
VS	1 ms	←	←
VBP	1.8ms	←	←

Total rasters: 261 rasters
Display raster: 200 rasters



(2) 640 x 400 bits display mode

fH = 20.92 kHz
fV = 47.3 Hz



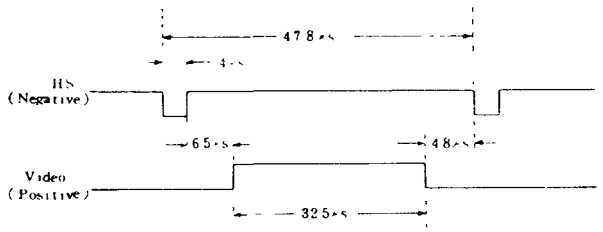
X : Y : 1 : 1

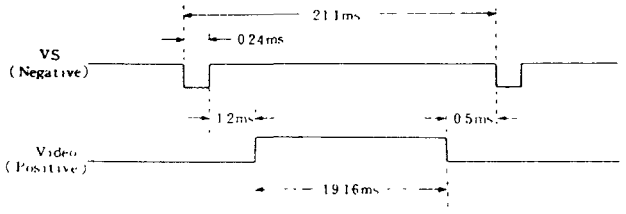
	GDC-1 (80 digits) Character display (40 digits)	GDC-2 (graphic) 8 bits	16 bits
Dot clock (0D)	(19 66MHz) (9 83 MHz)	19.66MHz (50.86ns)	9.83MHz (101 92ns)
2XCCLK	(4.9152MHz) (2.4575MHz)	4.9152MHz (203.45ns)	2 4575MHz (406 9ns)
Horizontal display time	32 55μs 80 Chr. /40 Chr.	←	←
HFP	4.88μs	←	←
HS	4μs	← (tREF=0.6ms)	← 5 Chr. (tREF=1.23ms)
HBP	6 5μs	←	←
Vertical display time	19.16ms	←	←
VFP	0.527ms	←	←
VP	0.24 ms	←	←
VBP	1.198ms	←	←

Total rasters: 441 rasters
Display rasters 400 rasters

(3) CRT synchronizing signal specification (400 raster CRT)

1. Horizontal synchronization frequency (fH): 20.92kHz
2. Vercial synchronization frequency (fV): 47.3Hz
3. Total rasters: 441 rasters
4. Rasters used: 400 rasters
5. Display dots: 640 x 400 dots
6. Dot clock: (19.66MHz)
7. Timing





VFP: 11 rasters (0.5ms)
VS: 5 rasters (0.24ms)
VBP: 25 rasters (1.2ms)

8. Output method HS, VS, and VIDEO are indpendent outputs.
9. HS, VS, and VIDEO signals are supplied from the LS type TTL IC (totem pole)

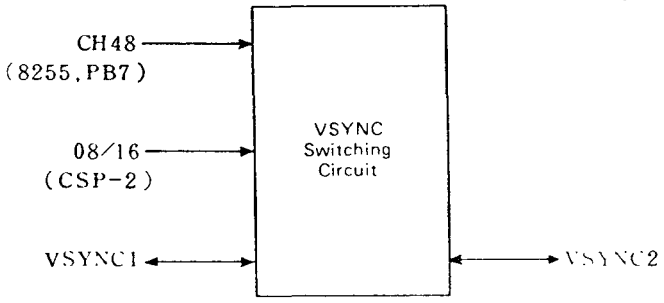
6) Setup of GCD master/slave

(1) Master/slave setup by combination

Character GDC / Graphic GDC	40 digits	80 digits
Without VRAM PWB	Character	Character
8 bit structure 48K byte 200 rasters	Character	Character
16-bit structure 96K byte 48K byte 400 rasters	Character	Graphic

* Master should be setup in the above manner.

(2) I/O signal switching

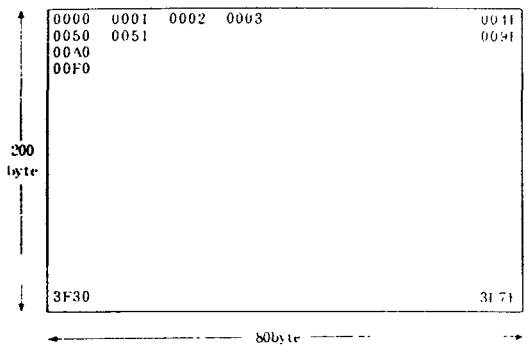


CH48 – { 0: For 40 digit display
1: For 80 digit display
There is a 40/80 digit switching signal I/O port in the gate array of CSP1 and CSP2, but, the I/O signal called CH48 is provided apart from the I/O port.

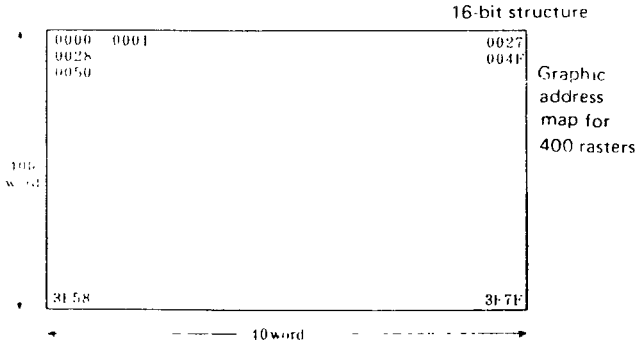
08/16 – I/O port inside CSP1 and CSP2.

7) Graphic V-RAM Address

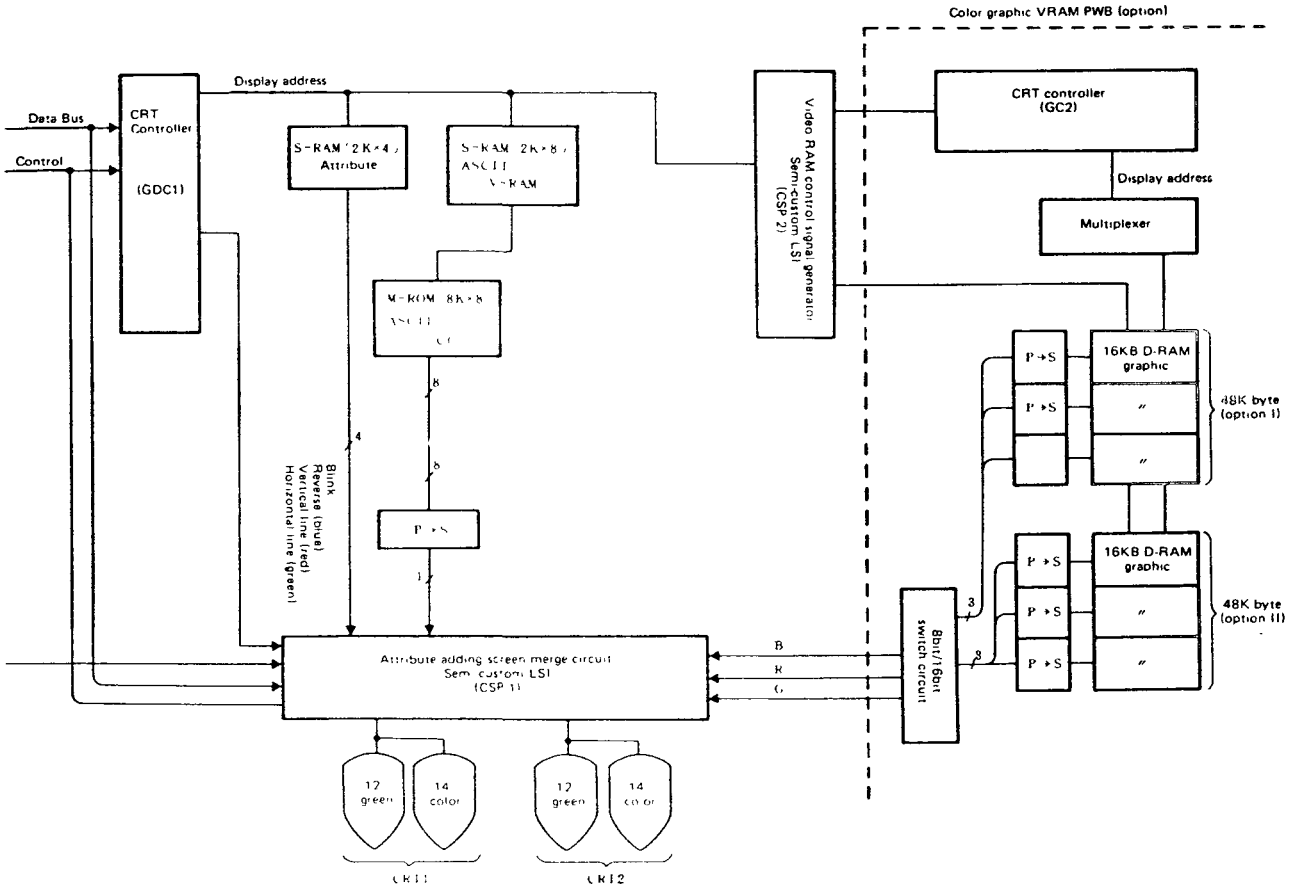
Relation between VRAM address and screen (640 x 200 dots)



Relation between VRAM address and screen



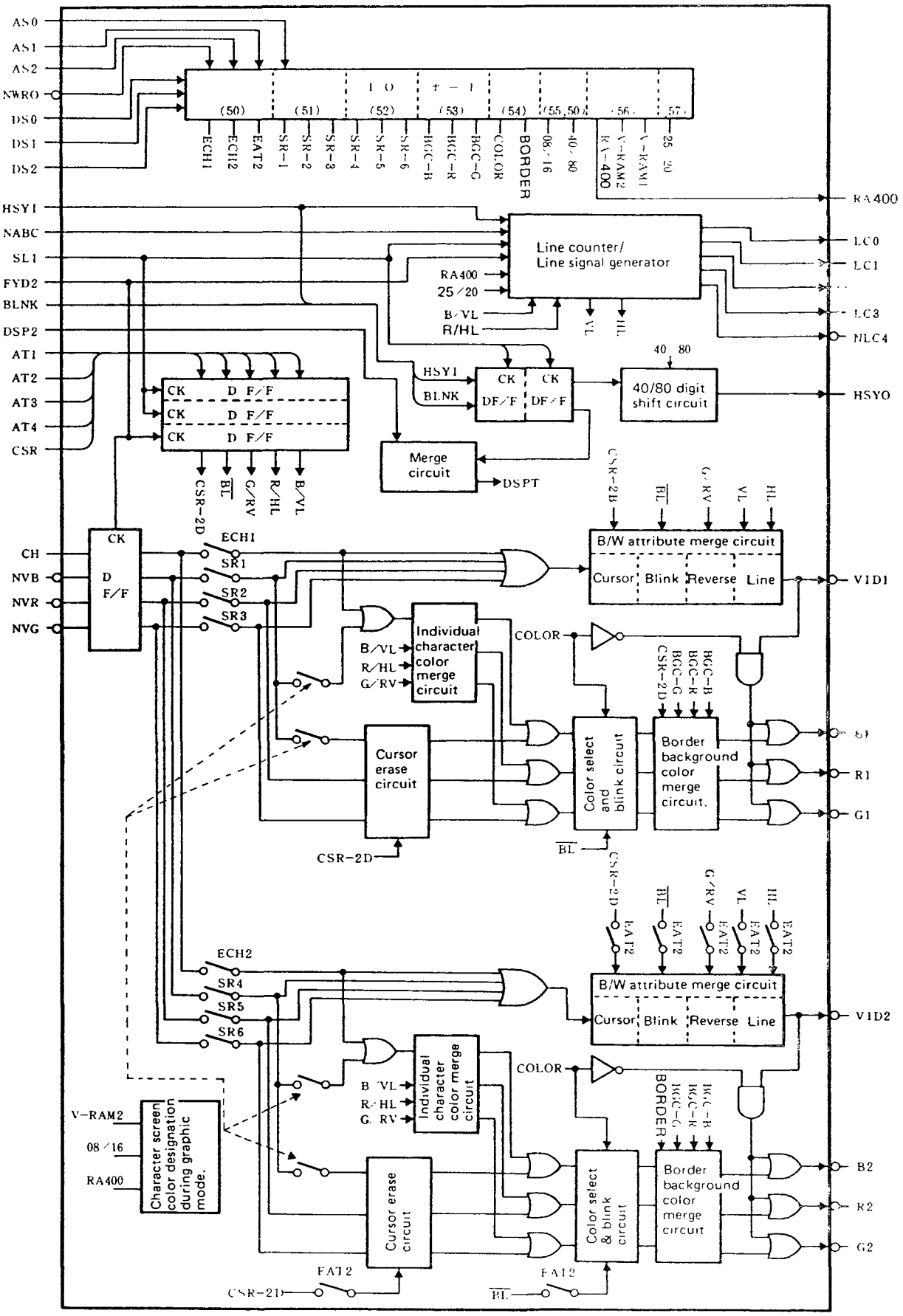
CRTC block diagram



4.5. Master slice LSI (CSP-1) SP6102C-002 signal description

Pin No.	Priority / Signal Name	IN/OUT	Function
1	HSY1	IN	Horizontal synchronizing signal from the GDC1 Also, it becomes the refresh timing signal in the dynamic RAM mode.
2	$\overline{NABC}$	IN	Input from the UPD7220 GDC1. When the GDC1 is in the character display mode, the attribute, blinking timing and line counter clear signals are multiplexed.
3	CSR	IN	Input from the GDC1 which is the cursor display input when the GDC1 is in the character display mode.
4 ~ 6	AS0 ~ AS2	IN	Address bus input from the sub-CPU. AB0 = AS0, AB1 = AS1, AB2 = AS2
7 ~ 9	DS0 ~ DS2	IN	Data bus input from the sub-CPU. DB0 = DB0, DB1 = DB1, DB2 = DB2
10	G2	OUT	Green image output to the CRT2.
11	$\overline{NWRO}$	IN	CSP1 I/O port select signal (OUT #5X)
12	$\overline{NVB}$	IN	Input of the blue image from the graphic RAM(A) and (B).
13	$\overline{NVR}$	IN	Input of the red image from the graphic RAM (B), (C), and (D).
14	$\overline{NVB}$	IN	Input of the green image from the graphic RAM (E) and (F).
15	FYD2	IN	Input of the graphic RAM parallel/serial conversion IC 74LS166 shift out clock. (Used to latch the image data in CSP1.)
16~18	AT2 ~ AT4	IN	Attribute data input from the 2114A-1 attribute RAM. {AT-2 – Horizontal line/R AT-3 – Reverse/G AT-4 – Blink}
19	CH	IN	Input of character display data signal.
20, 21	GND	IN	0V supply
22	DSP2	IN	Input of display timing signal supplied from the CSP-2. (BLINK signal from the GDC2 is delayed by two flipflop intervals in the CSP-2 to creat this signal.)
23	$\overline{VID2}$	OUT	VIDEO output to CRT2.
24	LCO	OUT	Character CG line counter output. (Becomes address input to the CG when LCO = CG address A0.)
25	AT1	IN	Attribute data input (vertical line/B) from the 2114A-1 attribute RAM.
26~28	LC1 ~ LC3	OUT	Character CG line counter output. (LC1 = A1, LC2 = A2, LC3 = A3CG = A3)
29	$\overline{NCL4}$	OUT	Character CG output data latch timing.
30	HSYO	OUT	CRT1, 2 horizontal synchronizing signal
31	RA40	OUT	The signal that turns high level when the 400-raster CRT is in connection. LDA, 01H OUT#56
32	$\overline{VID1}$	OUT	VIDEO output to the CRT1.
33	B1	OUT	Blue image output to the CRT1.
34	R1	OUT	Red image output to the CRT1.
35	$\overline{G1}$	OUT	Green image output to the CRT1.
36	SL1	IN	Character CG output parallel/serial converter IC 74LS166 shift load signal, and character CG address latch signal input. (Used for the image data latch signal in the CSP-1 and horizontal synchronizing signal delay flipflop clock.)
$\overline{37}$	B2	OUT	Blue image output to CRT2.
$\overline{38}$	R2	OUT	Red image output to CRT2.
39	BLNK	IN	Erase signal from the GDC1 which becomes input at the following times. 1. Horizontal flyback period 2. Vertical flyback period 3. Period from the execution of the SYNC SET command to the execution of the DISP START command. 4. Line drawing period
40	Vcc	IN	+5V supply.

CSP-1 Block Diagram

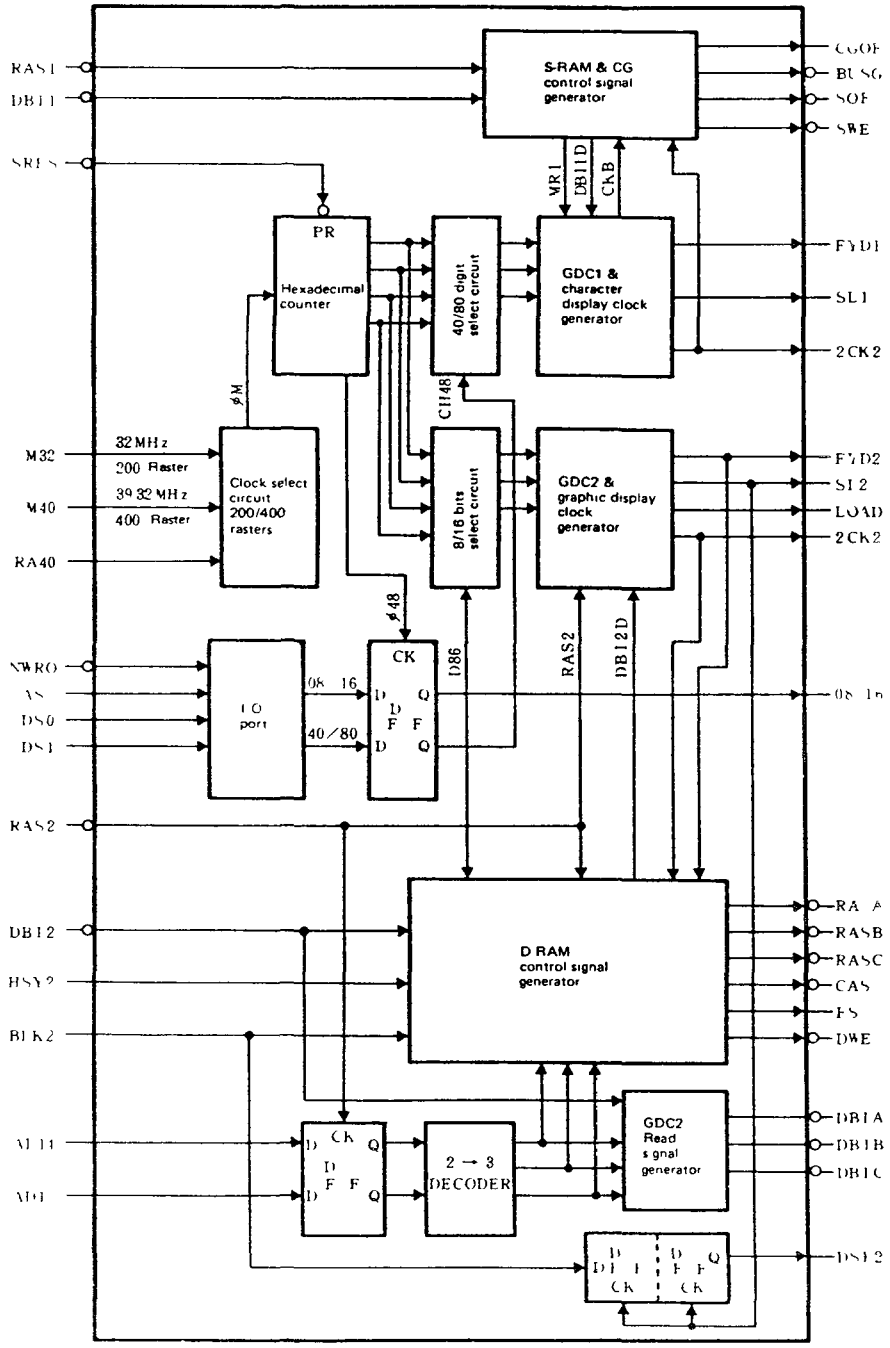


4-6. LSI (CSP-2) SP6012C-003 Signal Description

Pin No	Polarity / Signal Name	IN/OUT	Function
1	HSY2	IN	Horizontal synchronizing signal from GDC2 which also becomes the refresh timing signal in the dynamic RAM mode.
2	$\overline{BLK2}$	IN	Erase signal input from the GDC2 which is supplied 4T the following times: 1. Horizotal flyback period. 2. Vertical flyback period. 3. Period from the execution of the SYNC SET command to the execution of the DISP START command. 4. Line drawing period.
3	$\overline{DWE}$	OUT	WRITE ENABLE output for the graphic dynamic RAM.
4 ~ 5	AD14~AD15	IN	Input of the display output signals (AD14, AD15) from GDC2. (Used to create $\overline{DB1A}$-$\overline{DB1C}$ in the CSP-2.)
6	$\overline{DBI2}$	IN	Input from the GDC2 by which the image memory output is sent on the data bus. (Used to create $\overline{RASA}$-$\overline{RASC}$, $\overline{CAS}$, PS, $\overline{DWE}$ in the CSP-2.)
7	$\overline{DBI1}$	IN	Input from the GDC1 by which the image memory output is sent on the data bus. (Used to create $\overline{BUSG}$, $\overline{SOE}$, $\overline{SWE}$ in the CSP-2.)
8	$\overline{BUSG}$	OUT	Gate signal of the bidirection bus buffer (LS245) which is used to read/write attribute, and character, data from the static RAM (2114A-1, 6116P-3).
9	$\overline{SOE}$	OUT	OUTPUT ENABLE for character static RAM (6116P-3).
10	$\overline{SWE}$	OUT	WRITE ENABLE for attribute, character static RAM.
11	0816	OUT	8-bit/word and 16-bit/word select signal. (8-bit/word chosen with LDA, 00H OUT#5D, and 16-bit/word is chosen with LDA, 01H OUT#5D.)
12	$\overline{RAS1}$	IN	Memory control signal $\overline{RAS}$ from GDC1. (Used to create $\overline{CGOE}$, $\overline{SL1}$ in CSP-2.)
13	$\overline{RAS2}$	IN	Memory control signal $\overline{RAS}$ from CDC3. (Used to create $\overline{SL2}$, $\overline{LOAD}$, $\overline{RASA}$-$\overline{RASC}$, $\overline{CAS}$, FS, $\overline{DB1A}$-$\overline{DB1C}$, DSP2 in CSP-2.)
14	AS3	IN	Address bus input from the sub-CPU (AS3 = AB3)
15	$\overline{NWRO}$	IN	Chip select (OUT#5X) of the I/O port in CSP-2.
16~17	DS0~DS1	IN	Data bus input from the sub-CPU (DS0 = DB0, DS1 = DB1).
18	RA40	IN	The signal that goes to high level (input from CSP-1) when the 400-raster CRT is connected. (Used for clock frequency selection in CSP-2.)
19	M40	IN	Clock input from the clock generator (39.32MHz, for 400-raster mode.)
20	GND	IN	0V supply
21	SL2	OUT	Graphic DRAM output parallel/serial converter IC 74LS166 shift load signal.
22	$\overline{RASA}$	OUT	Graphic DRAM (A), (B) RAS signal.
23	2CM2	OUT	Double character clock output. In the character display mode, a single phase clock of the half the one character wide frequency is supplied. In the graphic display mode, a single phase clock of 8/16 dot frequency is supplied to GDC2.
24	LOAD	OUT	Graphic DRAM output parallel/serial converter IC 74LS166 load timing clock.
25	Vcc	IN	+5V supply.
26	FYD2	OUT	Graphic DRAM output parallel/serial converter IC 74LS166 shift out clock.
27	2CK1	OUT	Double character clock output same as 2CK2. In the character display mode, a single phase clock of one half the one character wide frequency is supplied to GDC1.
28	SL1	OUT	Character CG output parallel/serial converter IC 74LS166 shift out clock.
29	SL1	OUT	Character CG output parallel/serial converter IC LS166 shift load signal. Character CG address.
30	CGOE	OUT	Character CG output enable signal.
31~33	$\overline{DB1C}$~$\overline{DB1A}$	OUT	Timing signal by which the graphic DRAM output is sent on the data bus.
34~35	$\overline{RAS\text{-}C}$ ~ $\overline{RAS\text{-}B}$	OUT	Graphic DRAM RAS (ROW ADDRESS SELECT) signal. $\overline{RAS\text{-}B}$; RAM(C), (D) $\overline{RAS\text{-}C}$; RAM (E), (F)

Pin No	Priority / Signal Name	IN/OUT	Function
36	M32	IN	Clock input 32MHz, 200 raster
37	FS	OUT	Graphic DRAM address multiplexer signal (High order 8 bits [AD8 AD15] /low order 8 bits [AD0 AD7] select signal)
38	DSP2	OUT	Display timing signal (In the CSP 2, the signal BLINK from GDC2 is delayed by 2 collor intervals to create this signal)
39	$\overline{CAS2}$	OUT	Graphic D RAM CAS (COLUMN ADDRESS SELECT) signal (Line address selection)
40	Vcc	IN	+5V supply

CSP 2 Block Diagram



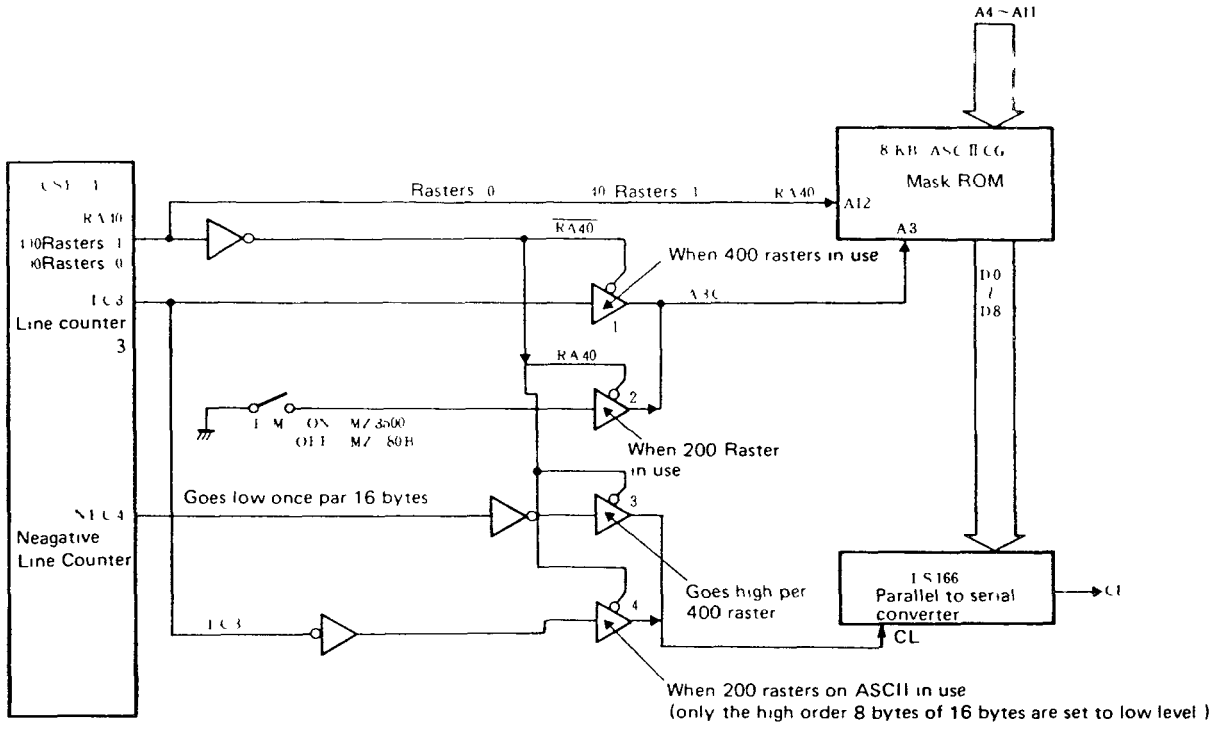
4-7. GDC (Graphic display controller) (UPD7220) signal description

Pin No.	Polarity / Signal Name	IN/OUT	Function
1	2XCCLK	IN	Double character clock supplied from the external dot timing generator which has the following two modes: 1. Character display mode: Single phase clock at one half of the one character wide cycle 2. Graphic display mode: Single phase clock of eight dots that cycles
2	$\overline{DBIN}$	OUT	Memory control signal supplied to the image memory from the GDC, which causes the image memory output data to be sent on the data bus.
3	HSYNC-REF	OUT	Memory control signal sent to the image memory from the GDC, which is the horizontal synchronizing signal. • Since the image drawing process is automatically interrupted in the dynamic RAM mode the refresh address is output during the HSYNC period. It can also be used as the refresh timing signal. • Refresh is accomplished by suppressing the CAS signal derived from the $\overline{RAS}$ signal in the external circuit when the HSYC is at high lebel (Horizontal Synchronous – Refresh timing)
4	VSYNC EX.SY NC	IN/OUT	Establishes one of following two modes, depending on whether the GDC is operated by the master or the slave. 1. When the master is operational: sends out the vertical synchronizing signal. 2. When the slave is operational: The synchronizing signal generation counter is initialized by a high level input.
5	BLNK	OUT	Erase signal output is issued at the following times (blanking signal): 1. Horizontal flyback period. 2. Vertical flyback period 3. Period from the execution of the SYNC SET command to the execution of the DISP START command.
6	$\overline{RAS}$	OUT	Memory control signal sent to the image memory from the GDC. • In the dynamic RAM mode, it is used as the reference signal of $\overline{RAS}$. When at high level, used as the timing signal by which the address signal is latched. (Row Address Strobe)
7	DRQ (NO USE)	OUT	DMA request output which is connected with the DRQ input of the DMA controller is output by the following two commands: 1. DREQE (DMA request write): CPU memory to image memory. 2. DREQR (DMA request read). Image memory to CPU memory. It will be continuously output until the DMA transfer word/byte number set by the VECTW (vector write) command becomes zero. (DMA Request)
8	$\overline{DACK}$ (NO USE)	IN	Signal supplied from the DMA controller that is subsequently decoded by the GDC as the read or write signal during DMA. (DMA Acknowledge)
9	$\overline{RD}$	IN	In the external circuit $\overline{RD}$ is combined with the chip select signal (CS). And is used when the CPU reads from the GDC either data or status flag and the signal DACK. (Read strobe)
10	$\overline{WR}$	IN	In the external circuit $\overline{WR}$ is combined with the chip select signal. And is used when the CPU writes to the GDC either a command or parameter and the signal DACK. (Write strobe)
11	A0	IN	Normally, connected with the address line and is used to designate data type. (Address Bus 0)
12~19	D80~D87	IN/OUT	Bidirectional data bus connected to the system bus. (Data Bus 0 ~ 7)
20	GND	IN	0V supply.
21	LPEN	IN	Light pen strobe input. When a input light is sensed by the light pen, it outputs a high level signal. The CPU can then read the display address via the LPENR (Light Pen Read) command.
22~34	AD0~AD12	IN/OUT	Bidirectional address/data bus connected between the image memory and the GDC on which address and data are sent on the bus by means of multiplexer. ALE (Address Latch Enable) is drived from the RAS output in the external circuit. (Address/Data bus 0 ~ 12)

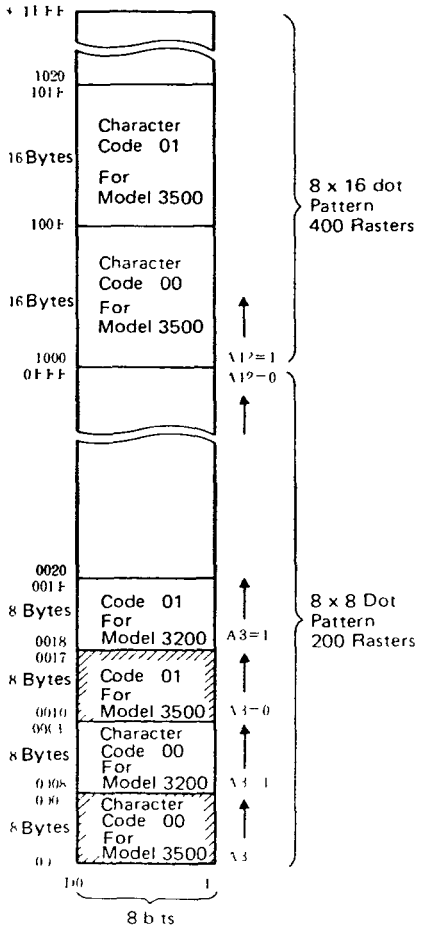
A0	$\overline{RD}$	$\overline{WR}$	Function	Device number of the Model 3500	
				GDC1	GDC2
0	0	1	READ STATUS FLAG	IN #70	IN #60
1	0	1	READ DATA	IN #71	IN #61
0	1	0	WRITE PARAMETER	OUT #70	OUT #60
1	1	0	WRITE COMMAND	OUT #71	OUT #61

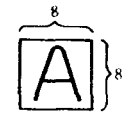
Pin No	Polarity / Signal Name	IN/OUT	Function
35~37	AD13(LC0)~ AD15(LC2)	IN/OUT	Provides the following functions based on the operational mode of the GDC (graphic display mode, character display mode 0, character display mode 1). 1. In the graphic display mode and character display mode 0: Bidirectional address/data bus 2. In the character display mode 1: Line counter output in connected to the character generator ROM or graphic RAM address. • In the graphic and character display mode 0: AD13~AD15. • In the character display mode 1: LC0~LC1. (Address Data bus 13 ~ 15) (Line Count 0 ~ 2)
38	A16 (LC3) ($\overline{\text{AT BLI}}$ / $\overline{\text{NK-CLC}}$)	OUT	Provides the following functions based on the operational mode of the GDC (graphic display mode, 0, character display mode 1): 1. Graphic display mode: Image memory address output. 2. Character display mode 1: Line counter output. 3. Character display mode 0: Attribute/blinking/timing signal and external line counter clear signal (Address 16) (Line Count 3) (Attribute Blink – Clear Lire Counter)
39	A17 (CSR) (CSR-IMAGE)	OUT	Provides the following functions based on the operational mode of the GDC (graphic display mode, character display mode 0, character display mode 1): 1. Graphic display mode: Image memory address output. 2. Character display mode 1: Cursor display output. 3. Character display mode 0: Cursor display output, character display area (graphic) display area select timing signal. (Address) (Cursor) (Cursor-image)
40	Vcc	IN	+5V supply.

4 8 CG Address Select Circuit

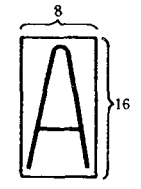


ASCII C.G. Structure





ASCII character structure
of the 200 raster CRT



ASCII character structure
of the 400 raster CRT

[Circuit description]

(Purpose)

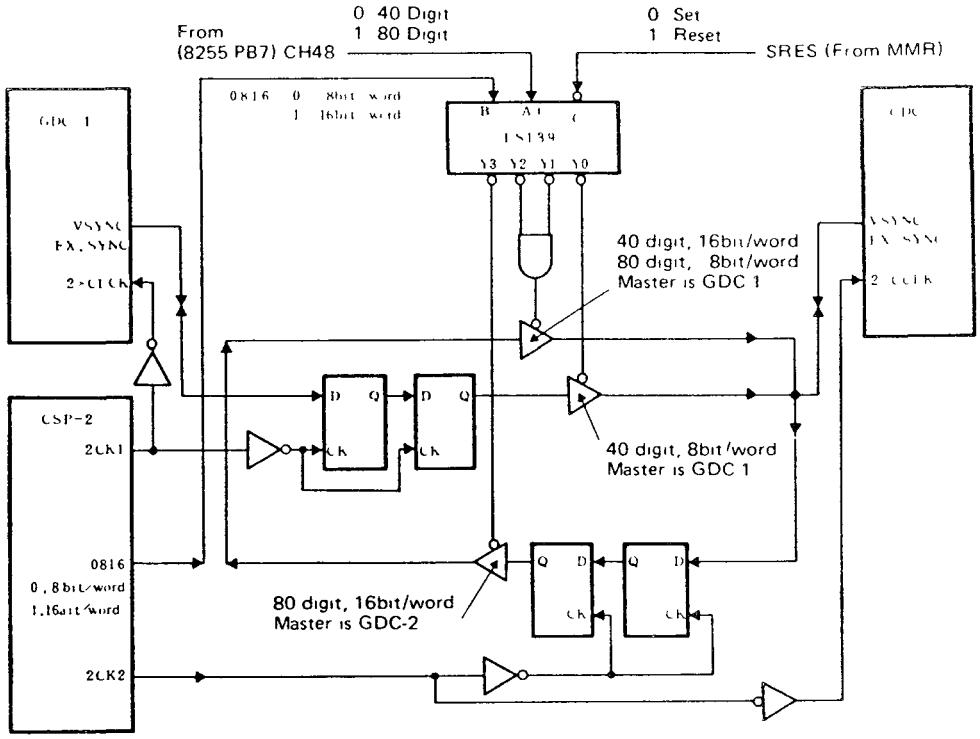
The character genrerator (CG) incorporates all character codes used by the 200 raster video display unit of the YX 3500 and by the 400 raster video display unit of the YX 3500 The CG address select circuit is therefore used to select those modes

[Operational description]

1 When the 400 raster CRT is in use, RA40 is set to high level which sets A12 of the CG to high level at all times, so that the CG address above 1000 is selected Also, gate (1) opened so that LC3 is input to A3 of the CG At the same time, gate (3) is opened so that the gate of the LS240 is closed every 16 bytes

2 When the 200 raster CRT is in use, RA40 is set turned to low level which sets A12 of the CG to low level continuously, so that the CG address 0000 0FFF is selected Also, gate (2) is opened so that the CPU

4-9. VSYNC



[Circuit description]

When more than two UPD7220 GDC's are to be operated in parallel, one must be assigned to the master and the other to the slave in order to mantain synchronous display timing. The master and the slave are determined according to the table below. The above circuit shoud be used to compare with the table description.

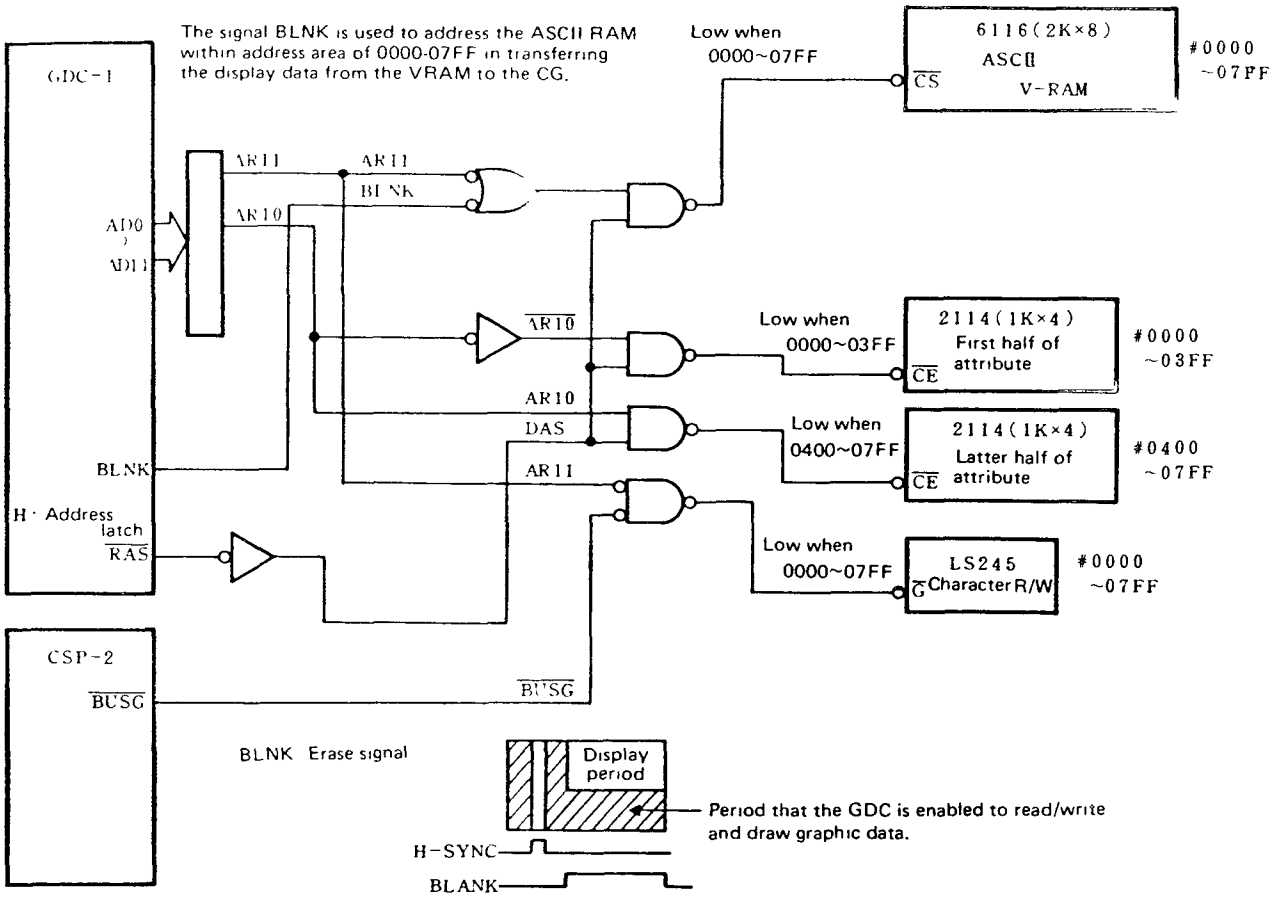
GDC-1 (character) / GDC-2 (graphic)	CH48 = 0 40 digit	CH48 = 1 80 digit
Without VRAM PWB	GDC1 (character) is the master.	GDC 1
8-bit structure [0816=0] (48KB, 200 raster)	GDC 1	GDC 1
16-bit structure [0816=1] (48 96KB, 400 rasters)	GDC 1	GDC2 (Graphic)

The master GDC must be set as indicated above.

[Oprational example]

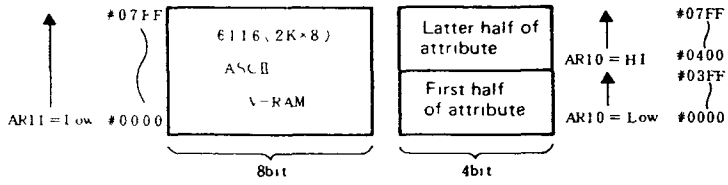
If it was set to 80 digit, 16 bit/word mode SRES will be 0 when CH48 = 1, 0816 = 1 when not in the reset condition. These signals are supplied to terminal A (weight 1), B (weight 2), and G (gate), and set terminal Y3 of the decoder IC LS139 to "0", so that the YSYNC output of the GDC2 is input to terminal EX SYNC of the GDC2.

4-10. Character VRAM select circuit



[Circuit description]

With respect to GCD1, the assignment during read/write of the character VIDEO-ROM is per the table below. The character VRAM select circuit is provided to accomplish this function.

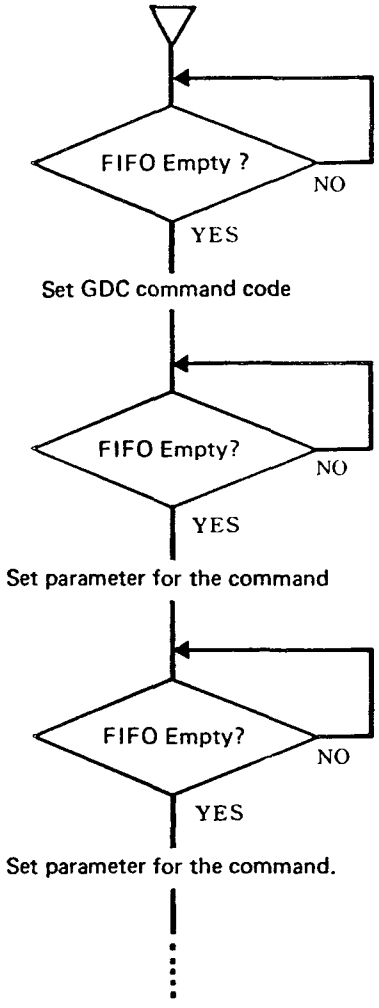


4-12. Read/write from the Z-80 to V-RAM

Read/write of the Model 3500 V-RAM is done via the UPD7220GDC. There are two methods used to read/write data. The method (1) is used for the model 3500.

(1) Read/write via the 16 byte FIFO.
(2) Read/write of V-RAM in the DMA mode without intervention of the FIFO.

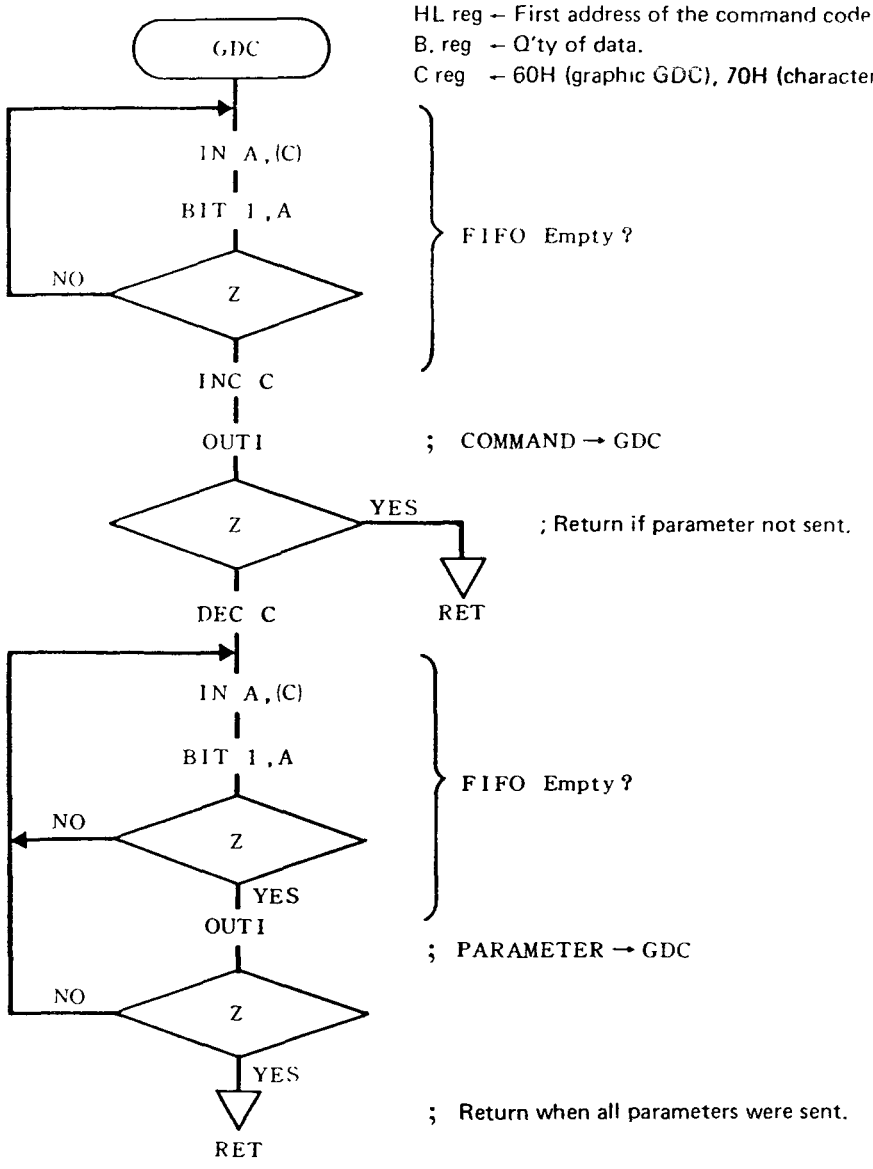
(Outline of the read/write data via the FIFO)



Method used to give a command to the GDC.

Command must be given to the GDC in the same manner.
On next page is the program of the above flowchart.

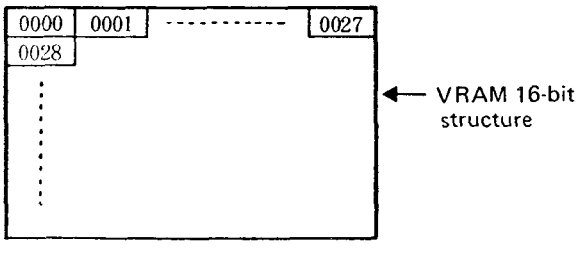
(Subroutine to send command and parameter to the GDC via the FIFO)



HL reg ← First address of the command code parameter table.
B. reg ← Q'ty of data.
C reg ← 60H (graphic GDC), 70H (character GDC)

Example of graphic drawing by GDC

1) Dot display



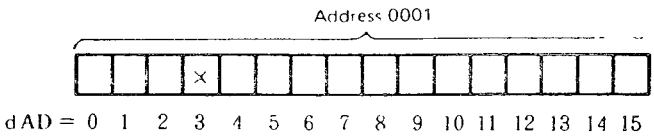
Example to display a dot on the fourth bit of the address

CSRW	C	49H	– COMMAND CODE
	P1	01H	– Low order one byte of the absolute address
	P2	00H	– High order one byte of the absolute address
	P3	30H	– Dot address (dAD)
WRITE	C	23H	– COMMAND CODE
VECTE	C	6CH	– COMMAND CODE

[Explanation]

C – COMMAND CODE
P – PARAMETER
} To A

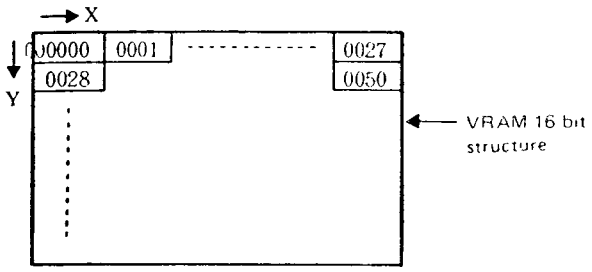
Display dot, specify the display address of the VRAM and the dot address. Set the command code of the SET mode (set mode plus CLEAR, REPLACE, and COMPLEMENT modes using "WRITE", and specify to start with "VECTE". Dot address is structured on the screen in the following manner.



[Dot display program example-1]

```
LD      HL ,5000H
LD      (HL),49H        5000 ← 49 H
INC     L               5001 ← 01 H
LD      (HL),01H        5002 ← 00 H     CSRW data
INC     L               5003 ← 30 H
LD      (HL),00H        5004 ← 23 H  } WRITE data
INC     L               5005 ← 6CH   } VECTE data
LD      (HL) 30H
INC     L
LD      (HL),23H
INC     L
LD      (HL),6CH
        |
LD      C ,60H          ; C – 60H (port address during graphic draw)
LD      B ,4H           ; B – Byte size CSRW data
LD      HL ,5000H       ; HL – Top address of the CSRW data
        |
CALL    GDC             ; Command, parameter of CSRW – GDC
        |
LD      C ,60H
LD      B ,1H           ; B – Byte size of the WRITE data
LD      HL ,5004H       ; HL – Top address of the WRITE data
        |
CALL    GDC             , Command, parameter of WRITE - GDC
        |
LD      C ,60H
LD      B ,1H           ; B – Byte number of the VECTE data
LD      HL ,5005H       ; HL – Top address of the VECTE data
        |
CALL    GDC             ; Command, parameter of the VECTE – GDC
        |
        ▽
```

2) Straight line drawing



Example to draw a straight line from (X, Y) = (3, 1) to (X, Y) = (635, 1).

Coordinates must be changed to absolute addresses.

(3, 1) – absolute address = 0028H

Dot address = 2H

Displacement between two points when the line draw direction is 0A (to the right): X = 635-3 = 632 (=278H), Y=0

Whereas,

```
CSRW    C   49H
        P1  28H  } EAD L, H
        P2  00H  }
        P3  20H    dAD
TEXTW   C   78H
        P1  FF   }
        P2  FF   } Kind of line (solid line)
VECTW   C   4CH
        P1  0AH  } Drawing direction
        P2  78H  }
        P3  02H  } |△X|
        P4  88H  }
        P5  FDH  } 2|△Y| - |△X|
        P6  10H  }
        P7  FBH  } 2|△Y| - 2|△X|
        P8  00H  }
        P9  00H  } 2|△Y|
WRITE   C   23H
VECTE   C   6CH
```

[Explanation]

Specify the kind of line by TEXTW, using C for command code and P for parameter, and specify the line drawing direction using VECTW and above four values using X and Y. The rest will be same the dot display. It is also possible to display a dot using the line drawing method for any line drawing direction using X = Y = 0.

5. MFD INTERFACE

5-1. Outline

Floppy disk is a disk which is made of a mylar sheet whose surface is coated with magnetic particles and set on the device to write and read data on the surface of the disk It will be necessary to know operating priciple of the floppy disk unit and operational description, including recording method and format.

5-2. Floppy disk

As various recording methods and formats are used for floppy disk (F.D.) systems we will discuss some of them

1) Floppy disk nomenclature

Floppy disks called by different names dependng on the manufacturer

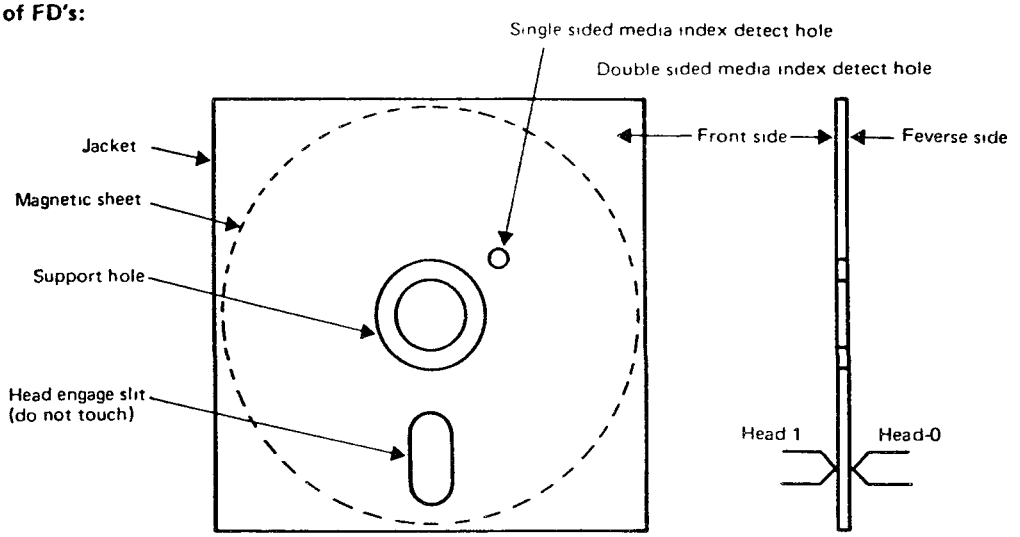
- a) Floppy media (or simply as media)
- b) Diskette
- Floppy disk

2) Types of media

Four types are used at present depending on their storage capacity·

- a) Single sided, double density (floppy disk-1)
- b) Double-sided, double density (floppy disk-2D)

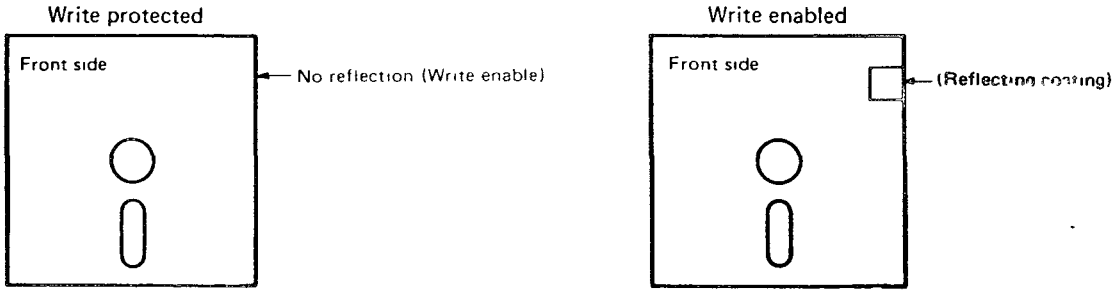
3) Components of FD's:



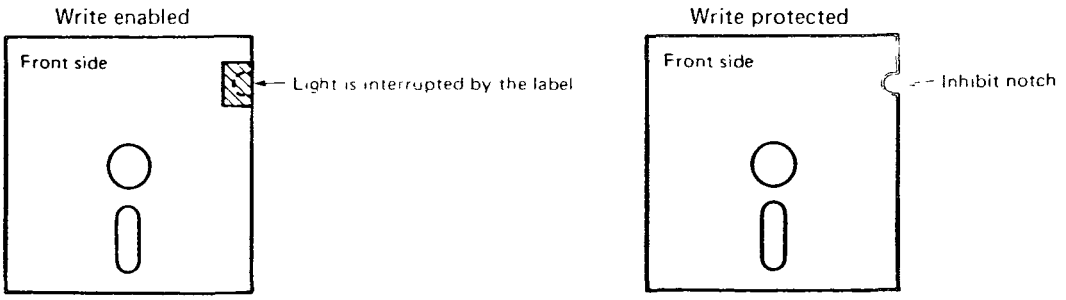
4) Write protect notch

Different write protects are adopted depending on the drive unit used.

Example-1: In the case of the CE331 the presence of light reflection is sensed by the photo coupler and decoded as write protect



Example-2: CE330S (light passing through the notch is sensed and decoded as write protect) (Double side, Double density)



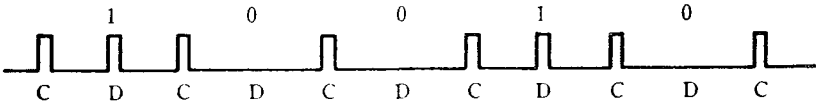
Two types of write protection are used and attention must bepaid to the presience of the label because it may cause a wrong result if the label is used improperly.

5) Media recording methods

Two recording methode are used:

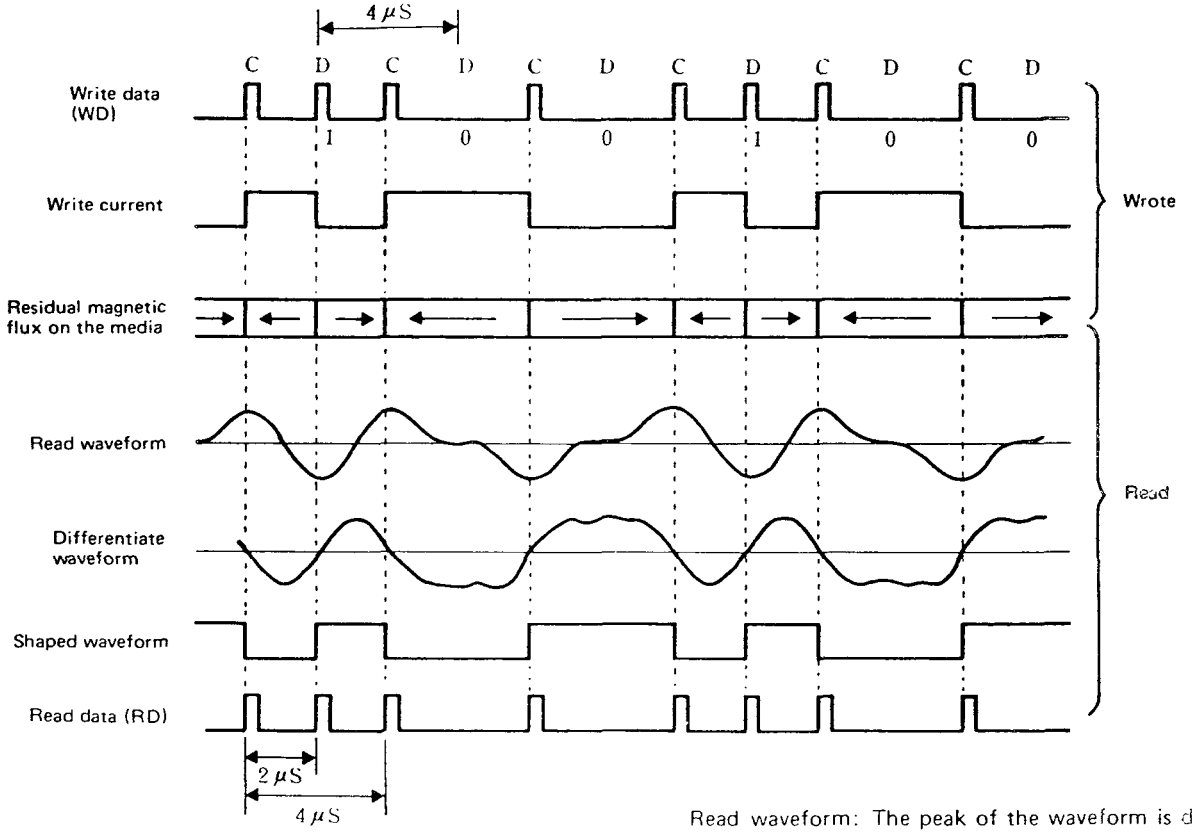
- FM method (Single density)

  This method is called the freqency modulation (FM) or double frequency (DF). Clock and data are written on the media which requires that a clock bit that precede the data.



(C: clock, D: data)

Waveforms of data written or read in the FM mode are shown below.



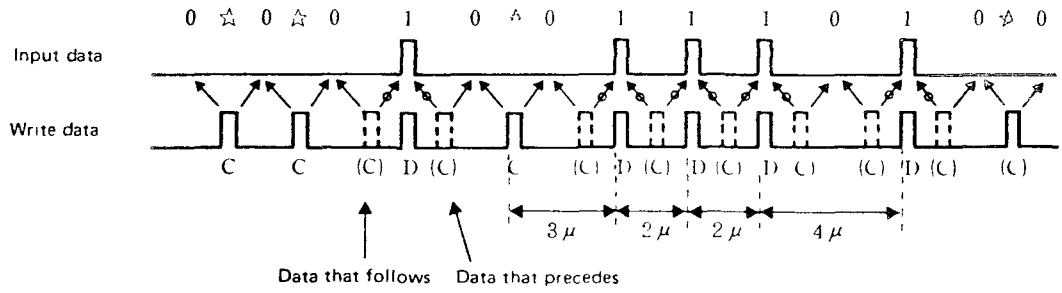
Write current: The write data is input to the flipflop and is inverted each time a pulse is received to change the direction of writing current.

Read waveform: The peak of the waveform is detected at a change of magnetic flux. The waveform is than shaped to obtain read data identical to the write data. Data cycle will be 4μs.

○ MFM method (double density)

The MFM method writes data on the basis of the condi tion metntioned below, and it yields a data density two times the data density of the MFM mode (The unneces sary clock pulse is eliminated using this method)

(Condition) Clock is written only when there is no data



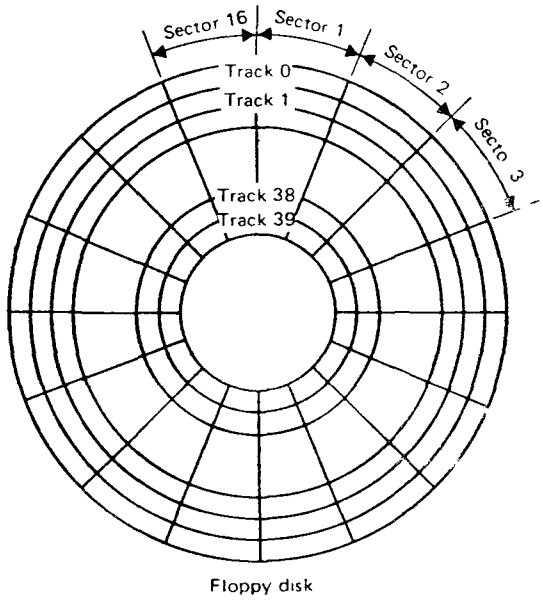
The clock pulse (C) will be eliminated in above illustra tion as there is no data preceding or following the clock Because the data rate is 2μs for this method, it is possible to obtain twice the density of the FM method (4μs).

NOTE Three types of write data cycle (2μ 3μ 4μs) are used The read/write waveform is identical to FM method

6) Media recording format

Media is formatted according to the IBM format

For Double side media, data is written on the front side (head-1) and the reverse side (head-00)



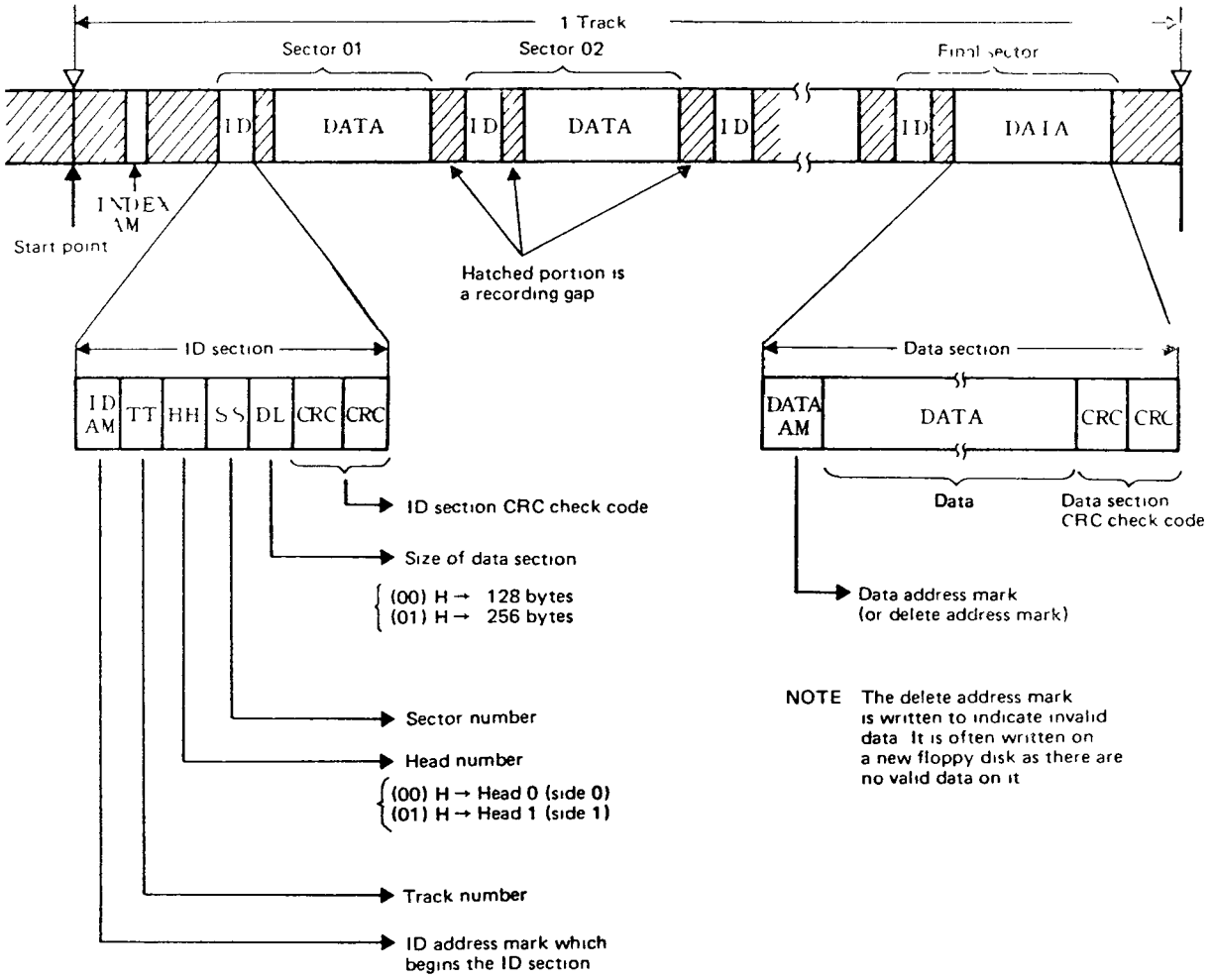
Floppy disk

Tracks. consists of 40 tracks, 00-39. (May also be called cylinders)

Sector. 01-16

Recording density: 256 bytes/sector

Shown below is an enlarged view of data format sequence Writing starts as soon as the index hole comes through the index detect hole



NOTE The delete address mark is written to indicate invalid data It is often written on a new floppy disk as there are no valid data on it

7) Formatting

To write the above format (ID section, data section, gap) on an entire surface of a new floppy disk is called formatting

Note 1 Formatting may also be called initialization. The word "initialize" is also used as a software term to clear the data section or to partition data area. Keep the difference between formatting and initializing in mind.

Note 2 Unless formatting has been done on a properly adjusted floppy disk drive unit, an erroe may occur on another floppy disk drive unit

8) Data write procedure

Described next is the procedure to write data on the FD.

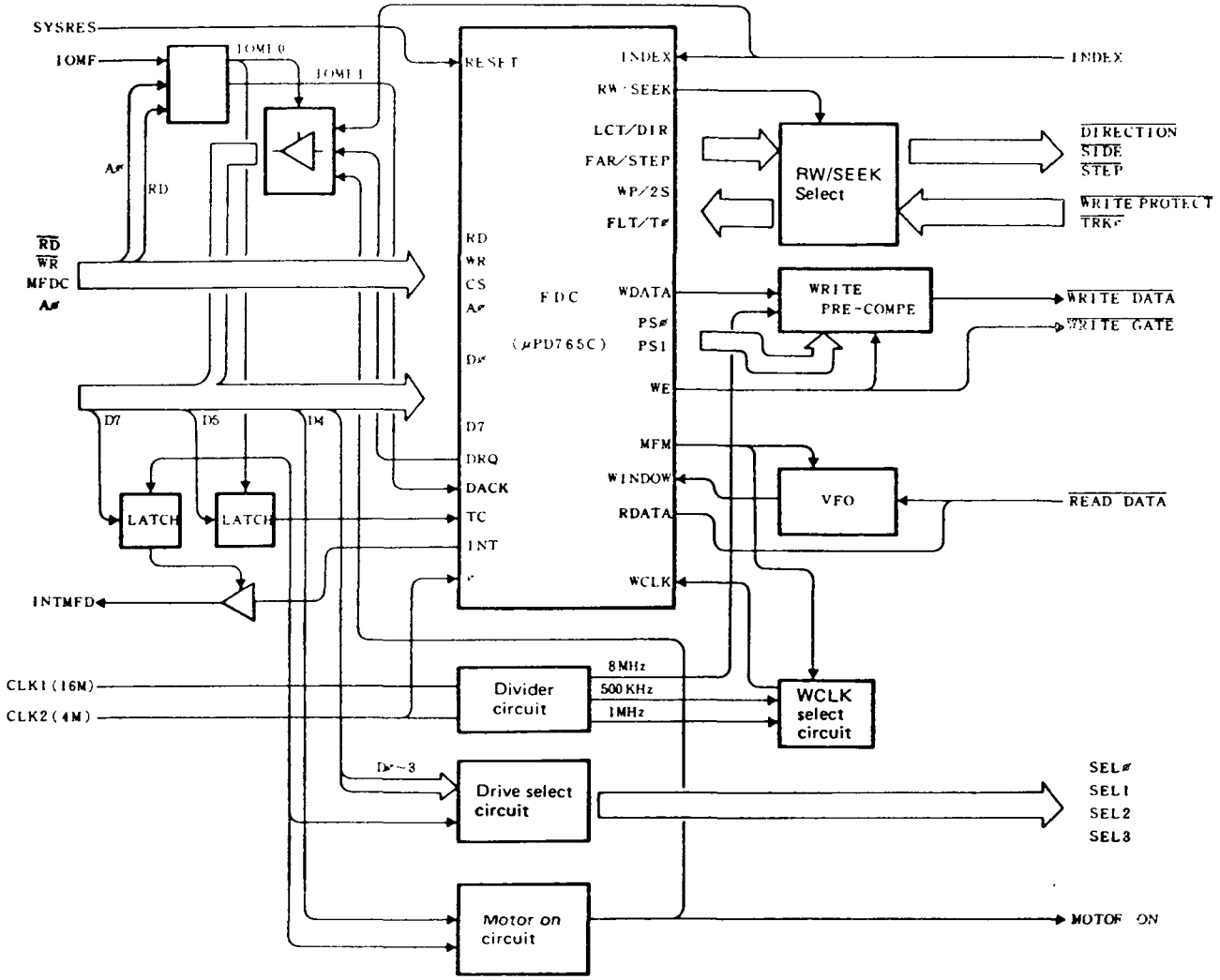
(1) The head is moved over the track to be written.
(2) The head is loaded
(3) ID section is read and repeated until the desired section is reached
(4) When the desired ID section is found, data is written on that area (DATA AM is also written)
(5) The data thus written is now checked if it was written correctly (read after write) The respective ID section is read while the media makes a full turn
(6) The sector of the identical ID is read and verified with the write data Because of this read after write capability the possibility of an error in the written data is quite low

9) Data read procedure

Described next is the procedure to read data from the FD.

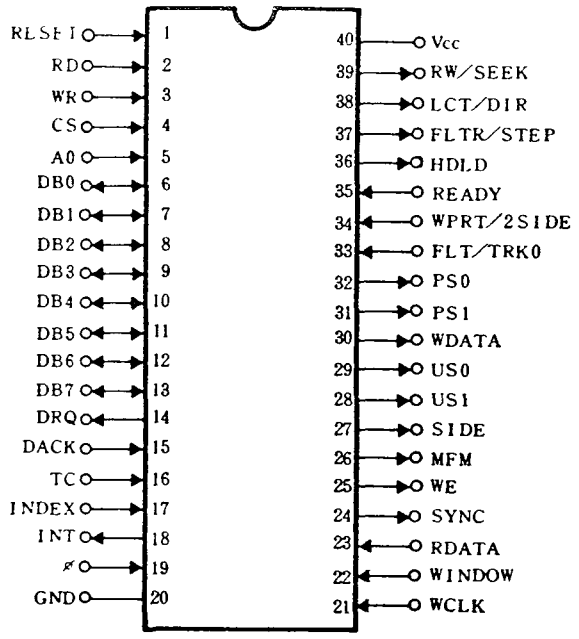
(1) The head is moved over the track to be read
(2) The head is loaded
(3) The ID section is read and repeated until the desired sector is reached
(4) When the identical IDsection is found, the data in that data section is then read

5-3. MFD interface block diagram

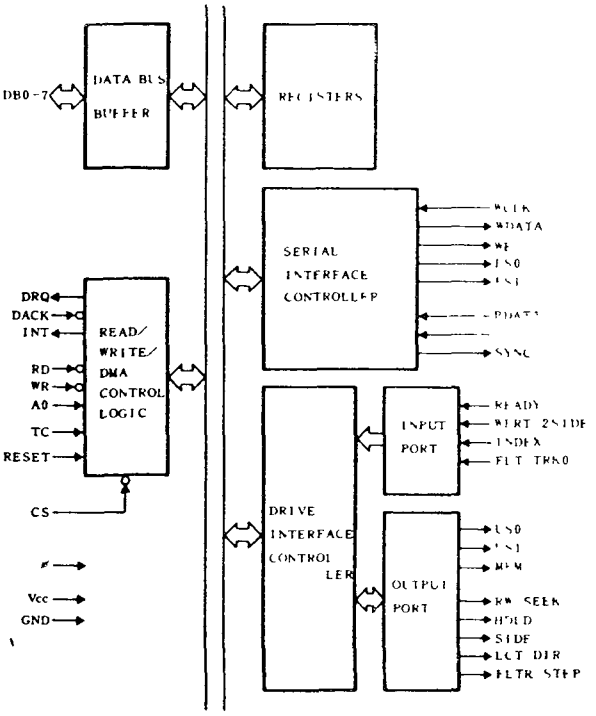


5-4. FDC (UPD765)

UPD765 pin configuration (top view)



UPD765 block diagram



RESET : Reset
RD : Read
WR : Write
CS : Chip Select
A0 : A0
DB0 - 7 : Data Bus
DRQ : DMA Request
DACK : DMA Acknowledge
TC : Terminal Count
INDEX : Index
INT : Interrupt Request
0 : Clock
GND : Ground
WCLK : Write Clock
WINDOW : Data Window
RDATA : Read Data
SYNC : VFO Synchronize
WE : Write Enable

MFM : MFM Mode
SIDE : Side Select
US0, 1 : Unit Select
WDATA : Write Data
PS0, 1 : Pre Shift
FLT : Fault
TRK0 : Track 0
WPRT : Write Protected
2 SIDE : Two Side
READY : Ready
HDLD : Head Load
FLTR : Fault Reset
STEP : Step
LCT : Low Current
DIR : Direction
RW/SEEK : Read Write/Seek

UPD765 signal description

Pin No.	Signal name	I/O	Function
40	Vcc	–	+5V
20	GND	–	0V
19	0	I	Single phase, TTL level clock
1	RESET	I	Set the FDC into an idle state, and all drive unit interface outputs, except PS0, 1, and WDATA (don't care), are set to low level In addition, INT and DRW outputs are set to low level DB goes into an input state.
4	CS	I	Validates RD and WR signals
13 ~ 6	DB7 ~ DB0	I/O	Bidirectional, tri-state data bus
3	WR	I	Control signal to write data to the FDC via the data bus
2	RD	I	Control signal to read data from the FDC via the data bus
18	INT	O	The signal used to indicate a service request from the FDC It is issued at every byte in the non-DMA mode, or upon completion execution of a command in the DMA mode
5	A0	I	The signal used to select the status register or data register of the FDC for access via the data bus. When 0, it selects the status register When 1, it selects the data register.
14	DRQ	O	FDC to memory data transfer request signal in the DMA mode
15	DACK	I	The signal that indicates use of the DMA cycle During the DMA cycle, it functions identically to CS.
29, 28	US0, 1	O	Drive unit select signal, with which up to four drive units can be selected.
26	MFM	O	The signal used to designate the operation mode of the VFO circuit When 0, the MFM mode is assigned. When 1, the FM mode is assigned
24	SYNC	O	The signal used to designate the operation mode of the VFO circuit When 1, it permits reading operation. When 0, it prohibits reading operation
39	RW/SEEK	O	Signal used to discriminate the read/write signal from the seek signal that used for drive unit interfacing signal. When 0, it indicates RW When 1, it indicates
36	HDLD	O	Signal used to load the read/write head
27	SIDE	O	Signal used to select head #0 and head #1 for the double-sided floppy disk drive unit. When 0, it selects head 0. When 1, it selects head 1.
38	LCT/DIR	O	When the RW/seek signal is operating as RW, the signal works as LCT which indicates that the read/write head is selecting the cylinder above 43. When the RW/SEEK is operating as SEEK, it works as DIR which indicate seek direction When 0, seek is made towards outer side When 1, seek is made towards inner side
37	FLTR/STEP	O	When the RW/SEEK signal functions as RW, it works as FLTR which resets any fault condition as the seek step signal.
35	READY	I	Signal used to indicate that the drive unit is ready for operation
34	WPRT/2 SIDE	I	When the RW/SEEK signal is operating as RW, it function as WPRT which indicates that the drive unit or the floppy disk is write protected. When the RW/SEEK is function as the SEEK signal produces 2 SIDE which indicates that a double sided media is in use.
17	INDEX	I	Signal to indicate the physical start point of the track.
33	FLT/TRK0	I	When the RW/SEEK signal is operating as RW, it works as FLT which indicates that the drive unit is in a fault condition. When the RW/SEEK is operating as SEEK, it works as TRK0 which indicates that the read/write head is on cylinder 0.
16	TC	I	Signal used to indicate the termination of a read or write operation
30	WDATA	O	Data written on the floppy disk consists of clock bits and data bits
25	WE	O	Signal to indicate write enable to the drive unit
21	WCLK	I	Data write timing signal which is 250kHz in the FM mode or 500kHz in the MFM mode

<table>
<tr><th>Pin No</th><th>Signal name</th><th>I/O</th><th>Function</th></tr>
<tr><td>32, 31</td><td>PS0, 1</td><td>O</td><td>Signal used to either advance or delay the write data in writing under the MFM mode, to obtain timing adjustment for reading. The WDATA signal is controlled as shown in the table below
<table>
<tr><th>PS0</th><th>PS1</th><th>FM</th><th>MFM</th></tr>
<tr><td>0</td><td>0</td><td>Not changed</td><td>Not changed</td></tr>
<tr><td>0</td><td>1</td><td>–</td><td>LATE 225~250ns</td></tr>
<tr><td>1</td><td>0</td><td>–</td><td>EARLY 225~250ns</td></tr>
<tr><td>1</td><td>1</td><td>–</td><td>–</td></tr>
</table></td></tr>
<tr><td>23</td><td>RDATA</td><td>I</td><td>Read data from the drive unit consists of clock bits and data bits.</td></tr>
<tr><td>22</td><td>WINDOW</td><td>I</td><td>Signal created in the VFO circuit which is used to sample RDATA. Phase syncronization carried out in the FDC for RDATA data bits and WINDOW.</td></tr>
</table>

5-5. Data recording method

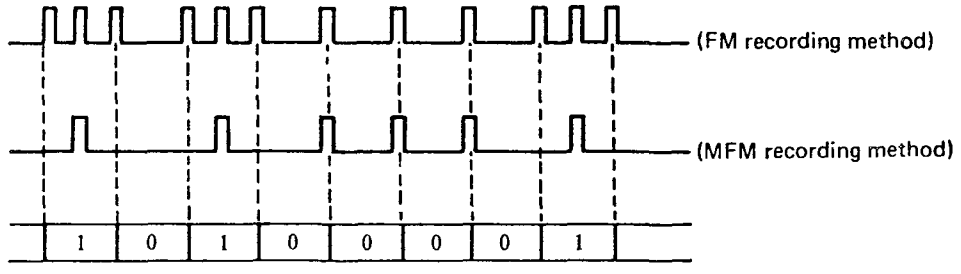
There are two ways of recording data; FM recording method and MFM recording method.

1) MF recording method

(1) Clock bit indicates a bit cell.
(2) Data bit is placed in a middle of a bit cell. (See Fig. 1.)

2) MFM recording method

(1) Data bit is placed in a middle of a bit cell.
(2) When the data bit is "0", a clock bit is placed before the current bit cell. (See Fig. 1)



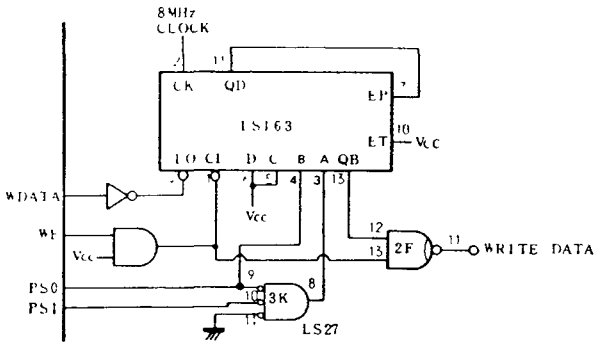
As seen from the above illustration, bit density of the MFM recording method is twice the FM recording method. In other words, data density of the MFM recording method doubles that of the FM recording method. For the Model 3500, only side 0 of track 0 (128 bytes/sector) is written in the FM mode and rest of other tracks are recorded in the MFM mode.

5-6. I/O port in the MFD interface

I/O port used in the MFD interface is as follows.

	D-BUS	I/O		
IOMF#F9·A0		OUT	$\overline{\text{DACK}}$	Used for data transfer between the CPU and the FDC.
IOMF#F8·$\overline{\text{A0}}$	D7	OUT	ME	INT from the FDC is output enabled on INTFD.
	D6		SCTRL	FDD select signal output is enabled.
	D5		TC	TC to FDC.
	D4		TRIG	Trigger (motor on) of the timer (555)
	D3		SEL3	Selects FDD 3
	D2		SEL2	Selects FDD 2
	D1		SEL1	Selects FDD 1
	D0		SEL0	Selects FDD 0
	D2	IN	M.ON	ON/OFF state of the motor
	D1		INDEX	INDEX signal from the motor
	D0		DRQ	DRO from the FDC.

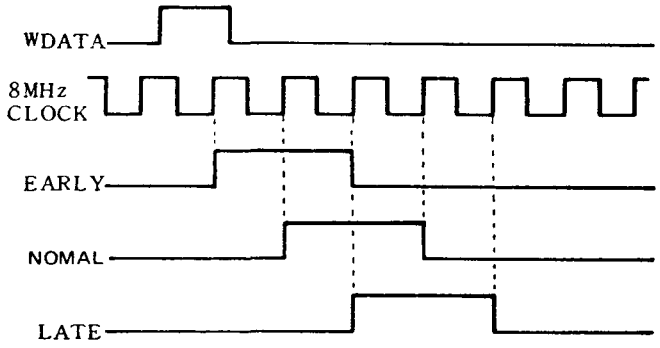
5-7. Precompensate Circuit



(Fig. 2)

PS0	PS1	FM	MFM	Value of LS163
0	0	Not changed	Not changed	1101
0	1	–	LATE(125μs)	1100
1	0	–	EARLY(125μs)	1110
1	1	–	–	–

(Table 1)

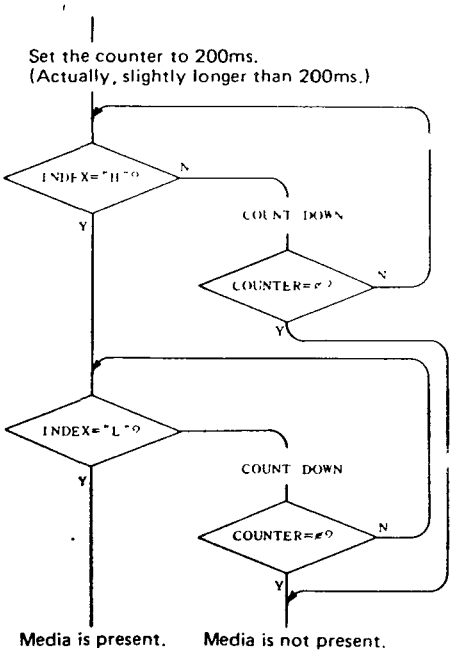


(Fig. 3)

The precompensate circuit is used to compensate the peak shift before writing.
The FDC sends out the compensation rate to PS0 and PS1 and the data bit location is shifted according to this signal. With issuance of WDATA, the value dependent on PS0 and PS1 is set in the LS163. (See Table 1.) For instance, when both PS0 and PS1 are low, it will set "1101(D)" to the LS163, counted up by the 8MHz clock, and QB is sent out When it becomes "1110, 1111". When in EARLY (PS0= "H", PS1="L"), the value "1110(E)" will be set to the LS163 so that the output is issued 125ns earier than "not changed". The QB output, however, will be supplied for a period of two clock cycles.

5-8. Media detection

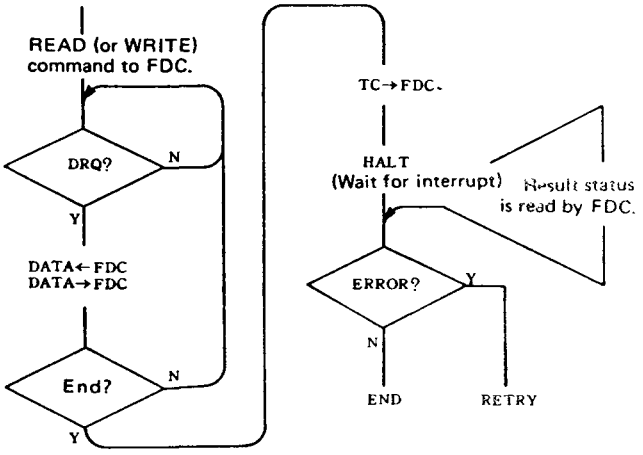
Insertion of a media on the MFD is detected via the signal INDEX from the MFD. Since it takes 200ms for the media to make a full turn, "NO MEDIA" is detected signal INDEX does not appear within 200ms.



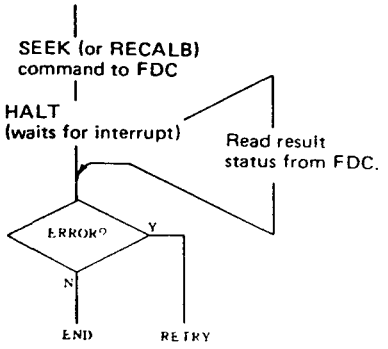
5-9. Controls during read, write, seek, and recalibrate

Above operations are all controlled via the FDC.

1) Control during read and write

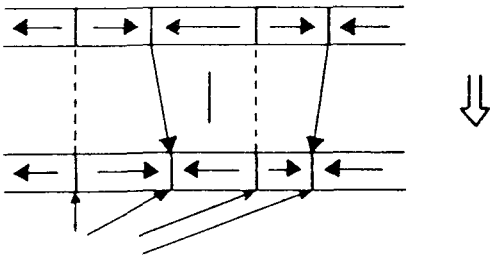


2) Control during seek and recalibration

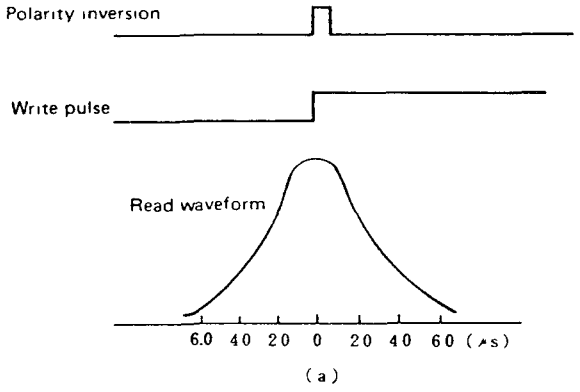


In the case of the MFM method, need to trace cycle fluctuation is further increased, as a peak shift is apt to occur because there are three write data cycles.

(Peak shift). Data read cycles fluctuate as the flux change point is moved forwards or backwards.

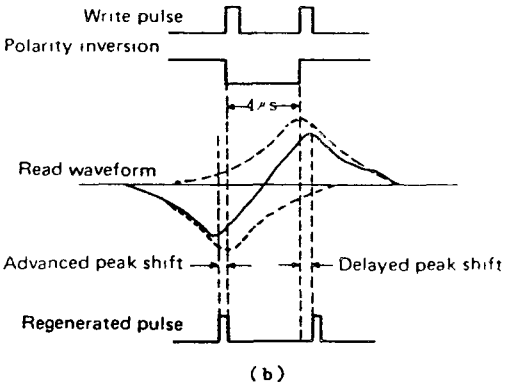


(VFO circuit): Variable frequency oscillator

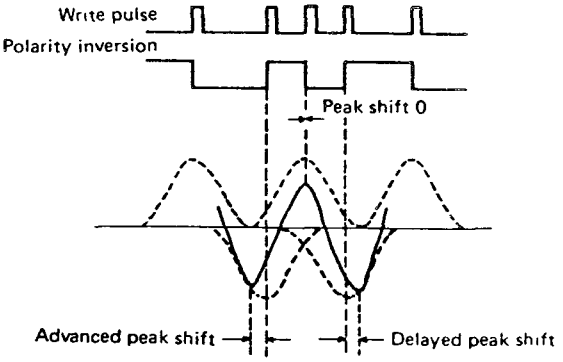


(a)

When the output waveform is observed after writing a single pluse on the floppy disk, the waveform show in (a) appears. Shown in (b) is two pluses of 4μs interval.



(b)

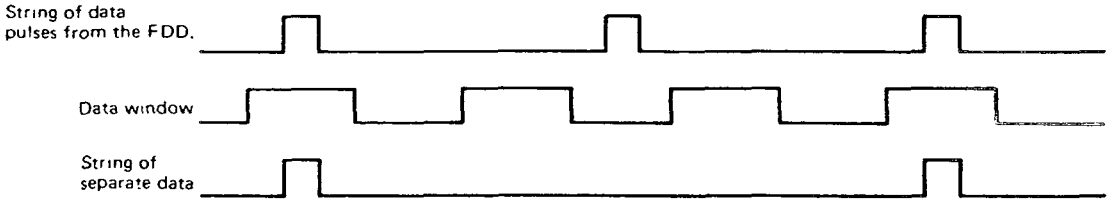


(c)

Deviation in the peak point is called peak shift. Since pluse intervals of the MFD in actual operation are 4μs, 6μs, and 8μs, the largest shift takes place when a pluse appears 8μs before or after 4μs, as shown in (c).

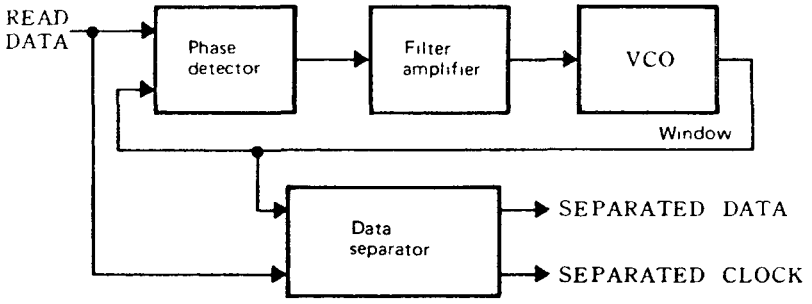
5-10. VFO circuit

1) Purpose



Data from the clock or data portion must be differentiated when read from the FDD. For this purpose a window pulse is used. In order to increase read tolerance, the VFO circuit carses the window to trace phase changes in the read data that take place during a floppy disk drive motor speed change.

2) VFO circuit configuration



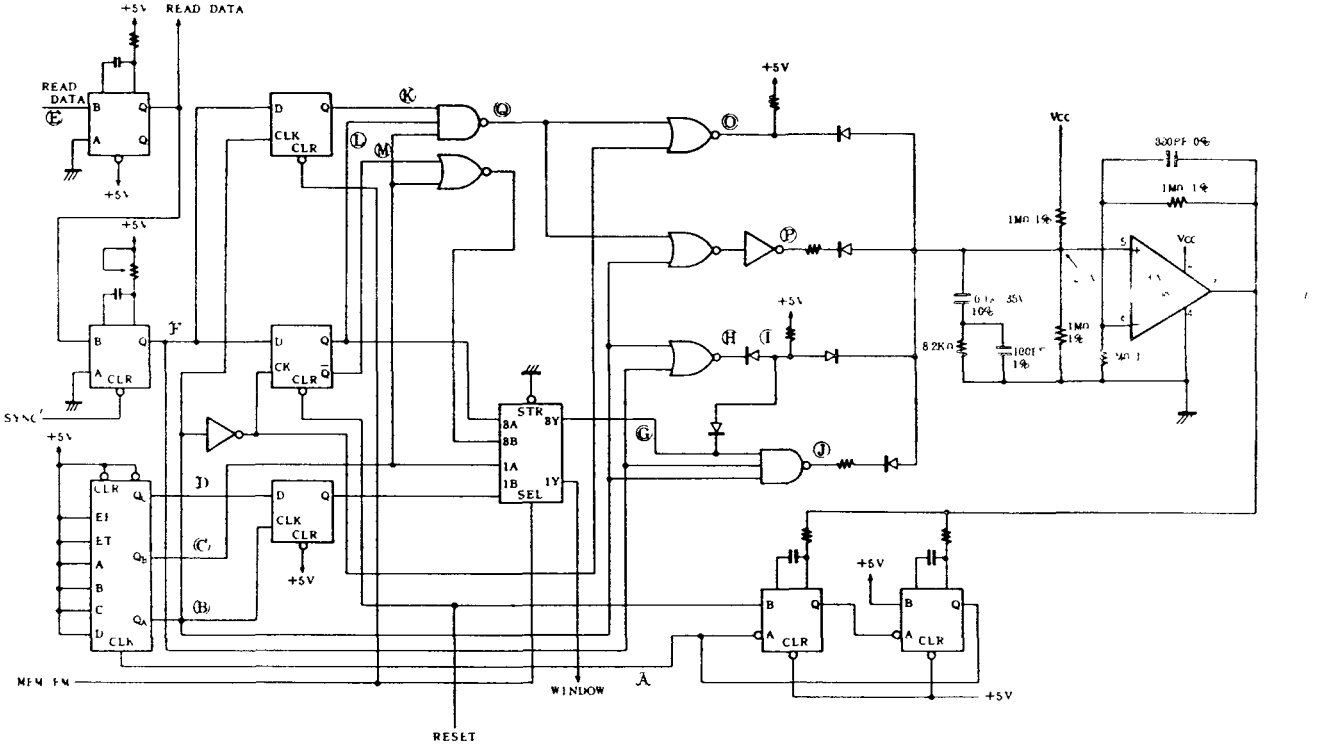
The VFO circuit has the following capabilities.

(1) Two modes: MFM and FM.

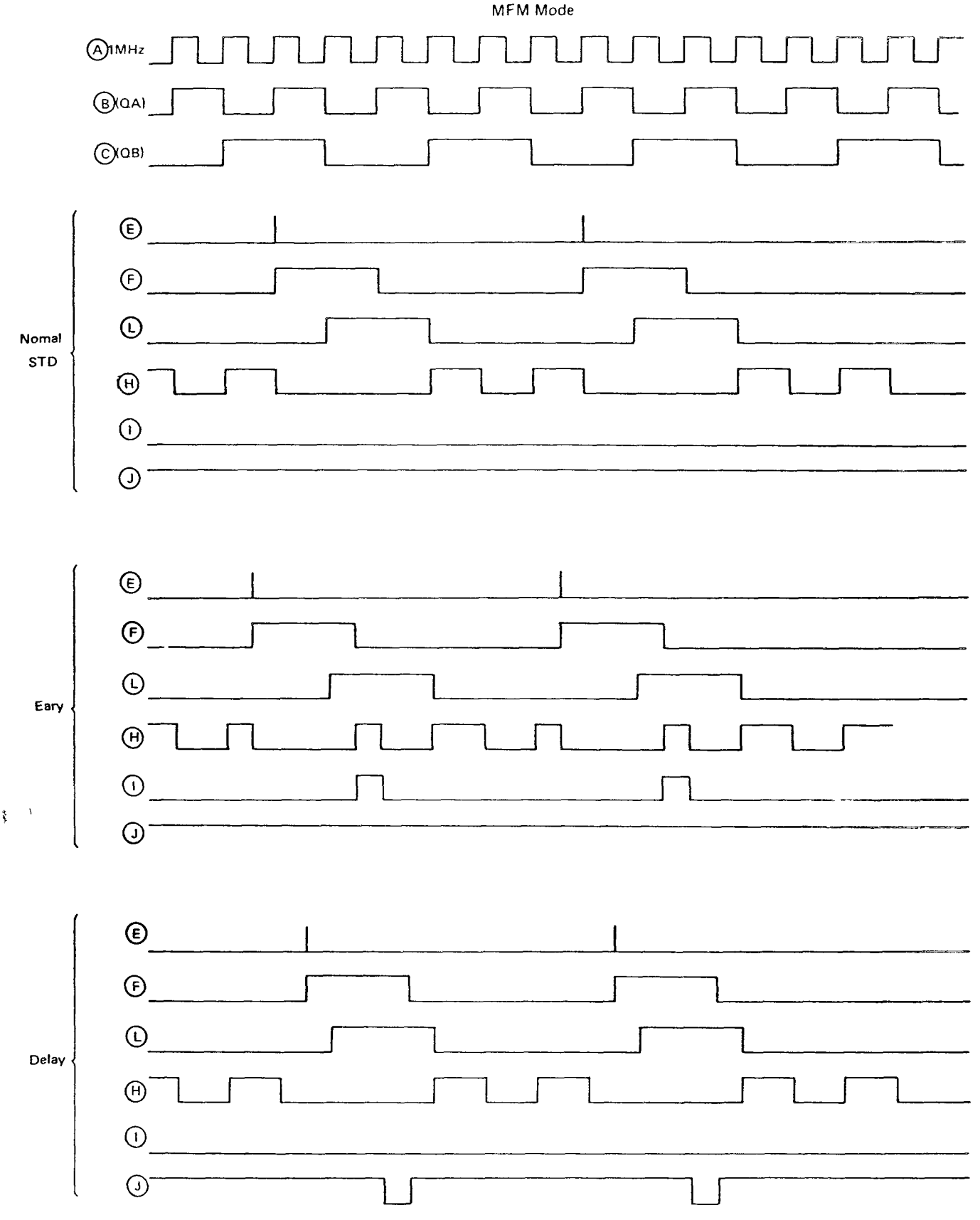
(2) The VFO circuit operation is suspended during the SYNC field located before the ID field and data field.

(3) After suspention, the VFO circuit will synchronize with the read data (timing is affected by a speed change in the FDD). Fluctuations in an individual bit that may be seen (peak shift are ignored.

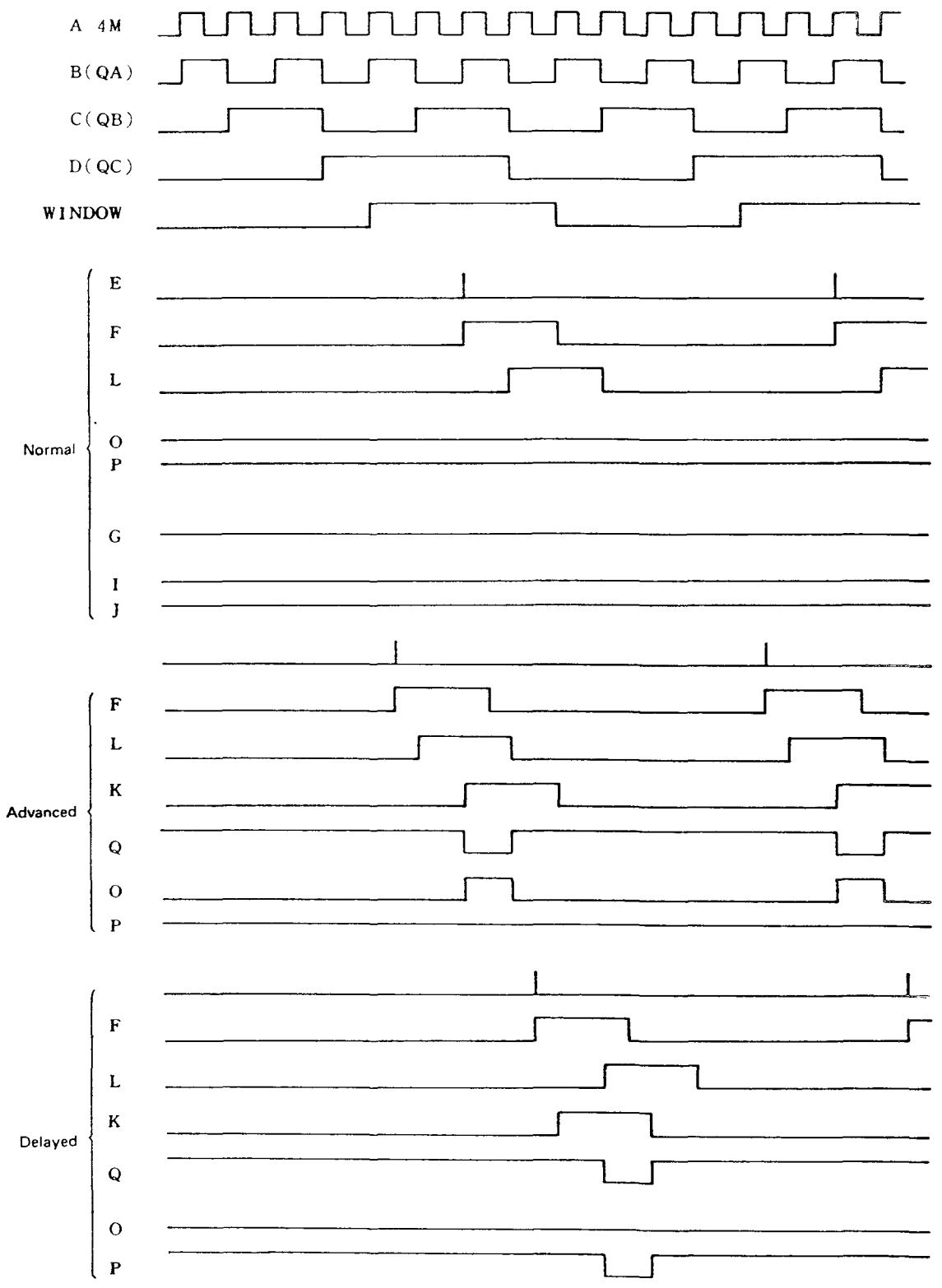
VFO circuit



MFM Mode



FM mode timing chart



Does not trace ±1μs.

5-11. Media format

0 track

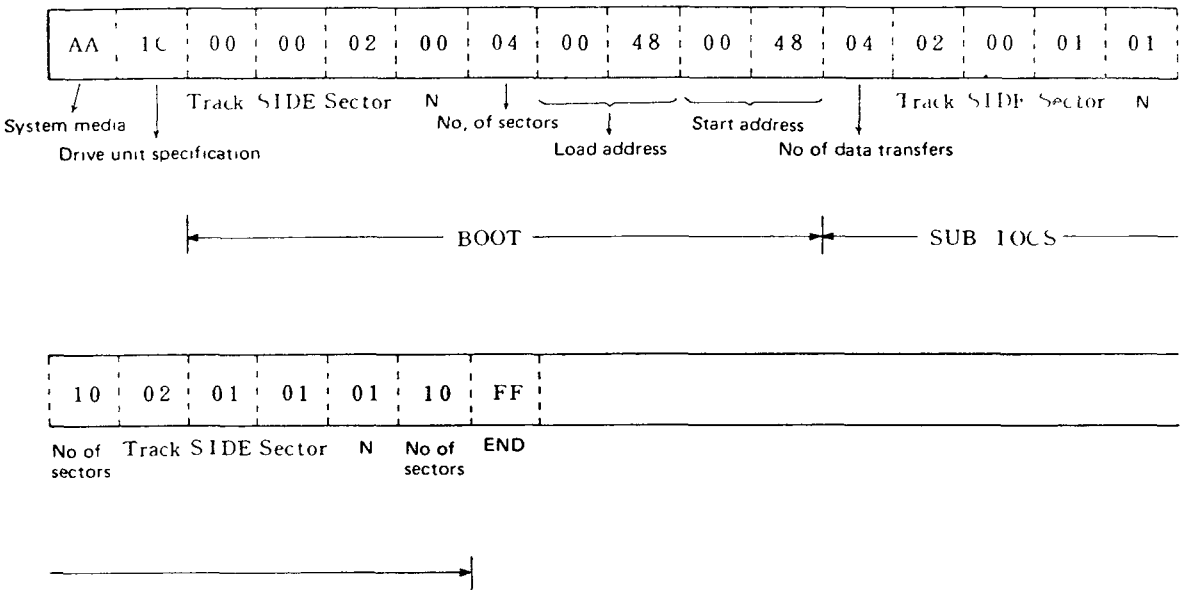
Sector	MASTER	BLANK MEDIA
1	Boot, OS information (See Fig 1)	00
2	BOOT	00
3	BOOT	00
4	BOOT	00
5	C5 , D9 , D4 , C1 , D7 , 40	40
6	00	
7	E5 , D6 , D3 , F1 , E2 , C8 , C1 , D9 , D7 , 40 ～ 40 , D4 (40onone side), 40～F1	
8		
9	MAP: Nine sectors for the media of 34 tracks	MAP FF
10	Area. 10th sector is also a MAP area for the media of 40 tracks	Area FF
16	FF	
1	E5	
2	E5	
15	E5	
16	E5	

Single density

Reverse side

Double density

Track 0, sector 1 information (SBACIS) (Fig 1)

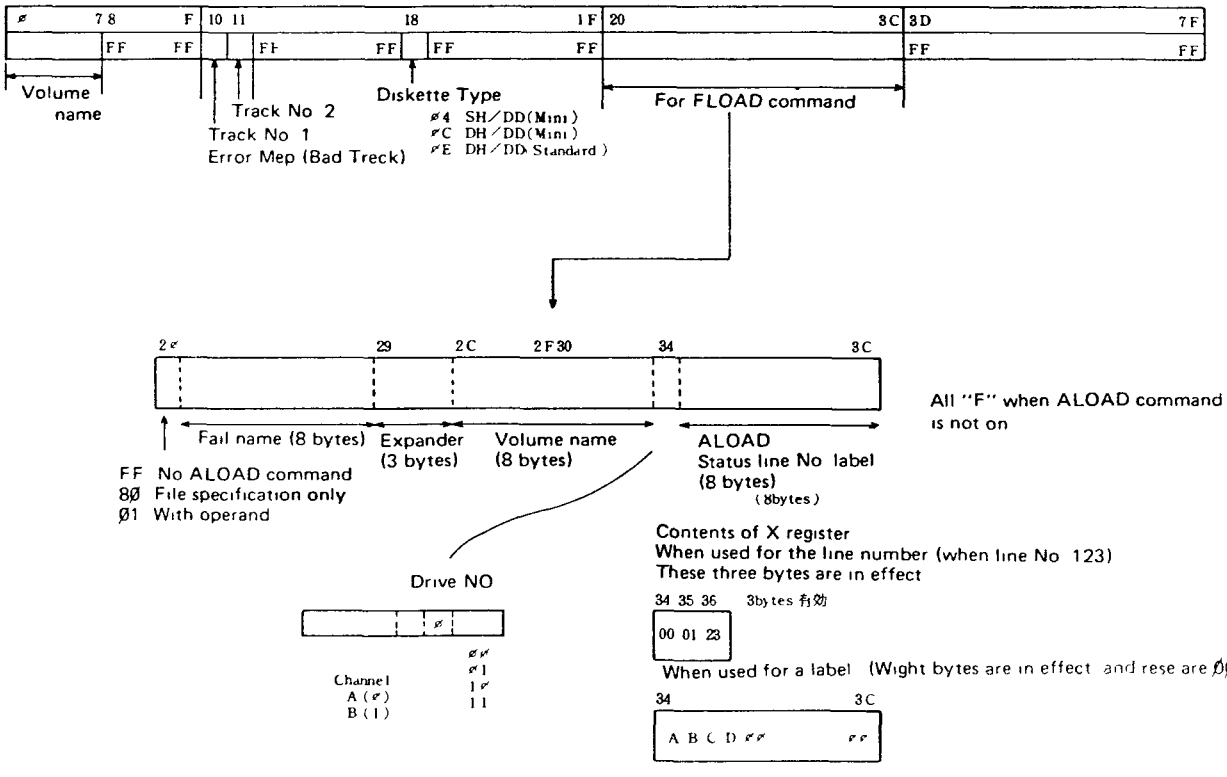


N = { 0 . Single density, other than front side, track 0.
1 . Double density, other than front side, track 0.

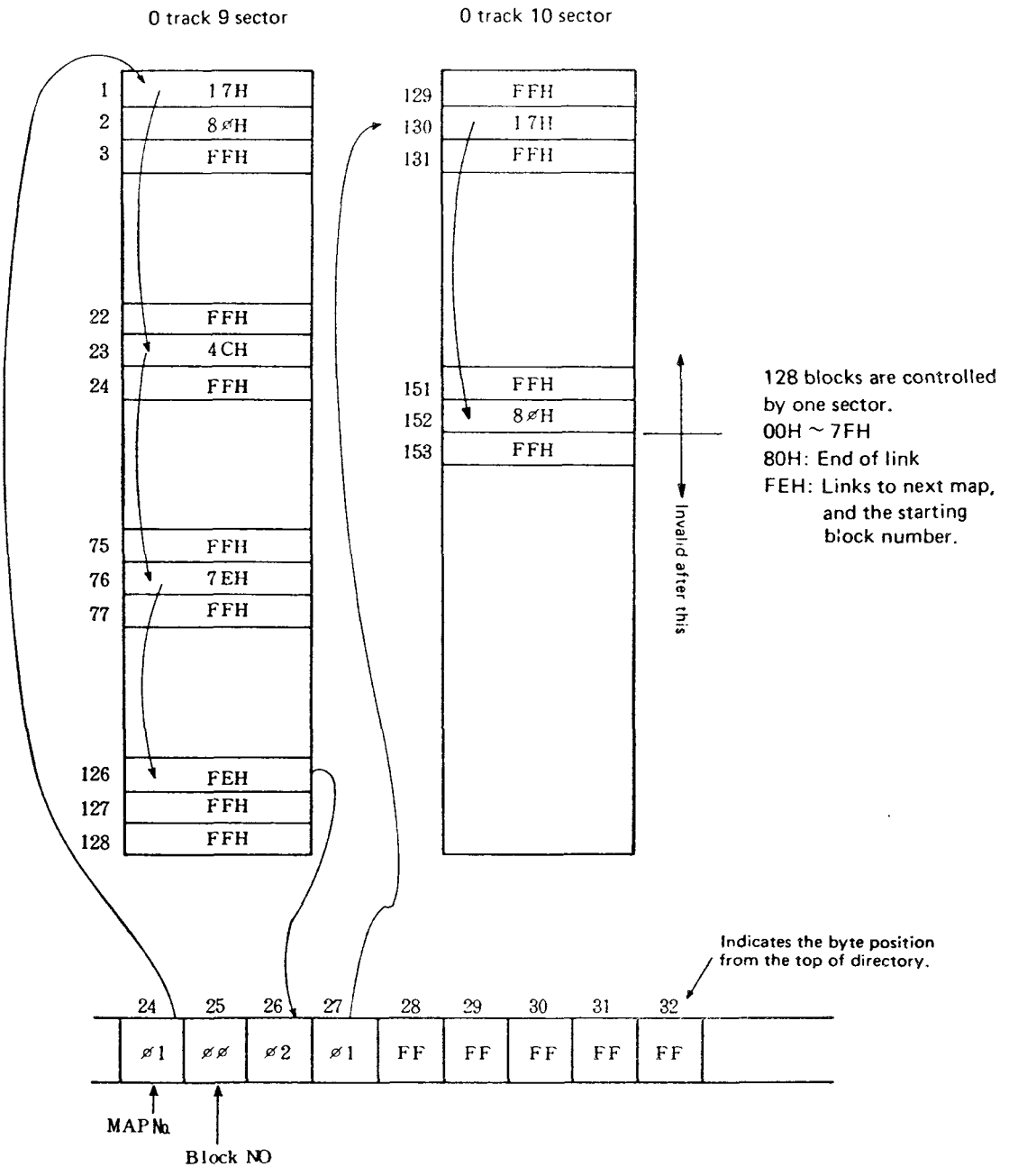
SIDE = { 0 . Side 0 (front side)
1 Side 1 (reverse side)

No of data transfers INT=[IOCS capacity/1k] + 1

0 track 8 sector



○ Map information



Starting block number (directory)

○ Block number allocation

The program and data areas are located after Track 2

1 block = 2K bytes (8 sector)

(Double side)

track	Block No			
	Front		Reverse	
2	B0	B1	B2	B3
3	B4	B5	B6	B7
⌇				
38	B144	B145	B146	B147
39	B148	B149	B150	B151

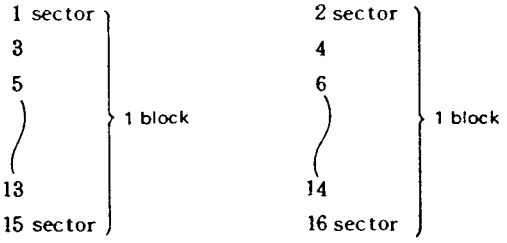
(2K × 152 = 304K)

(Single sided)

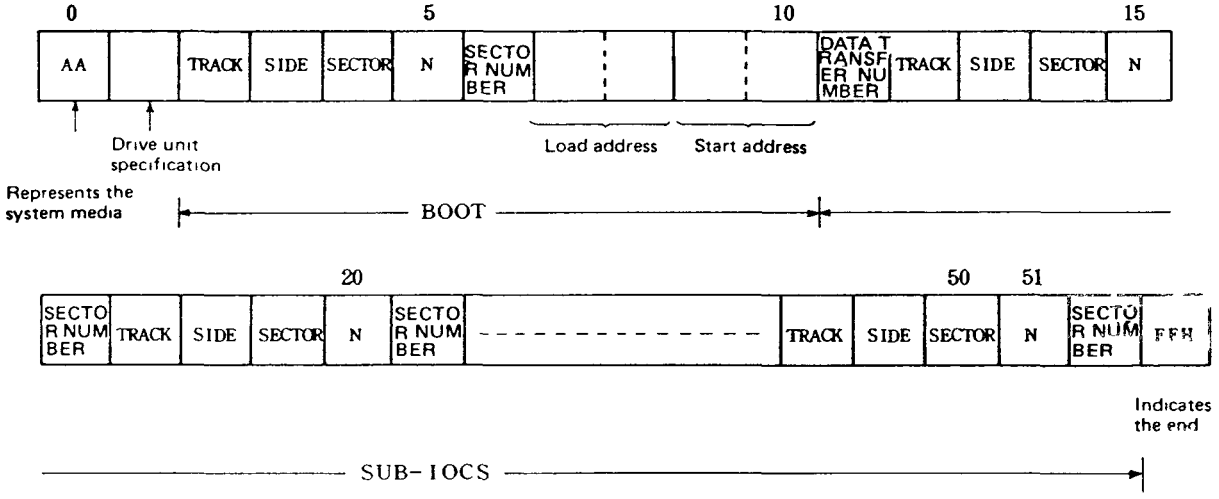
track	Block No	
	Front	
2	B0	B1
3	B2	B3
⌇		
38	B72	B73
39	B74	B75

(2K × 76 = 152K)

Each track is blocked in the following manner:



○ Track 1, Sector 1 information (CP/M)



N = 0 Single density (front, Track 0)
1 Double density (other than front, Track 0)

SIDE = 0 Side 0 (front)
1 Side 1 (reverse)

Nos of data transfers = INT [IOCS capacity/1K] + 1

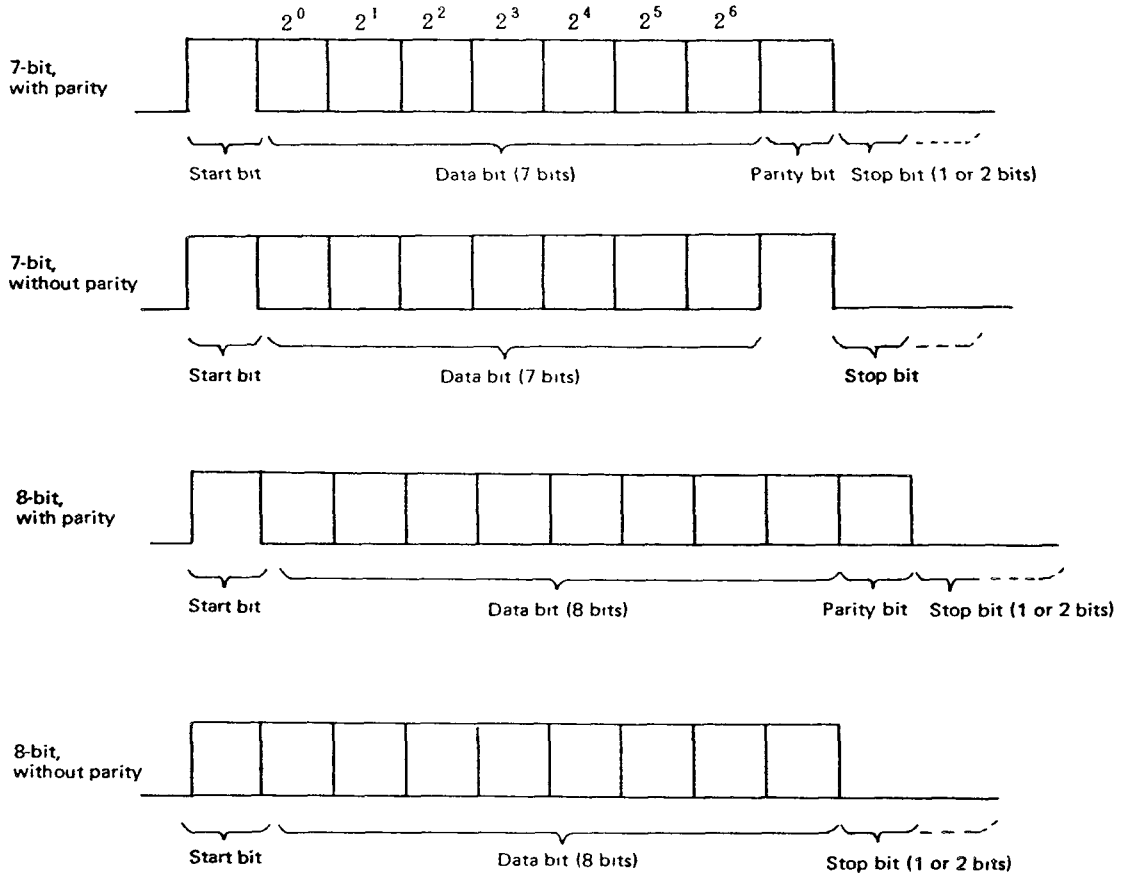
- Sub IOCS can be divided into either blocks If divided to less than eight blocks, the block that follows

6. R232C INTERFACE

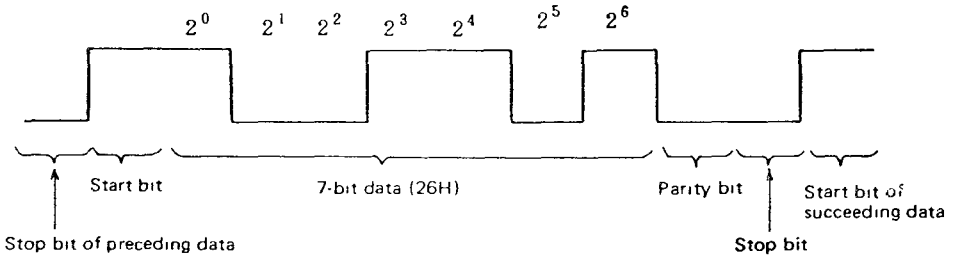
6-1. General specification

Input/output format	RS-232C bit serial input/output
No of channels	1 channel
Code used	JIS 7-channel/JIS 8 channel
Baud rate	110 to 9600 bits/sec
Transmission system	Half-duplex
Synchronization method	Start-stop
Communication control procedure	Non-procedure
Data format	Stop bit: 1/1.5/2, with or without even or odd parity.
LSI used	8251AC or 8253C-5 (Programmable Interval Timer)

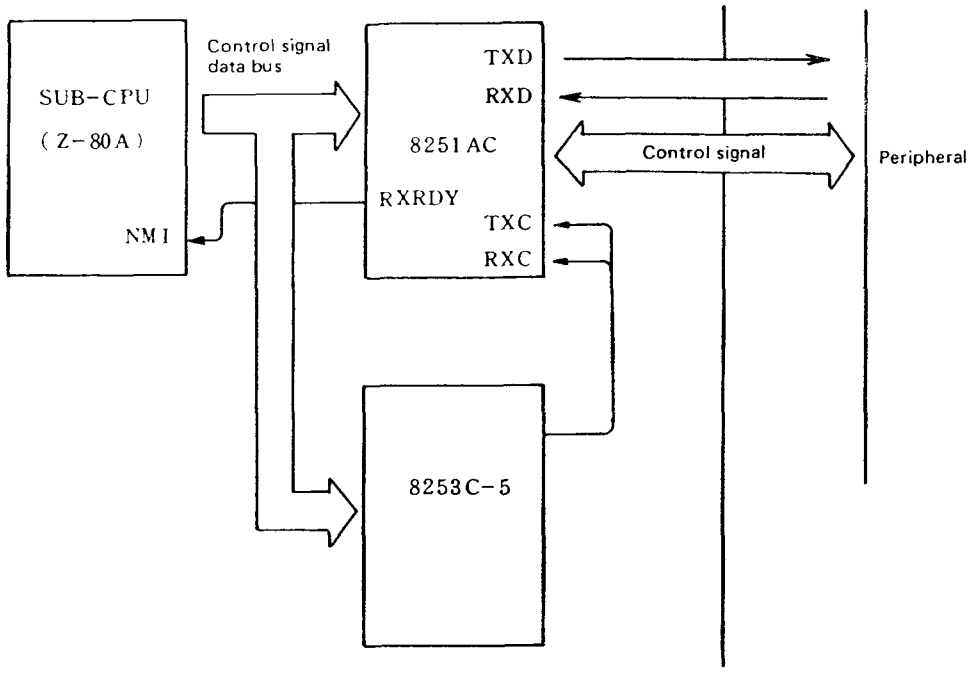
6-2. Data transmission format



Example: 7-bits, even parity, 1 stop bit



6-3. Block diagram of the interface



6-4. System switch functions

	ON	OFF
SW5	Causes an error when the ER signal is low or open during data output.	ER signal is disabled.
SW6	Always high when power is on to the main unit.	The CD signal is set high while data output, but would not be set high when the echo-back function is selected for the host computer.
SW7	Causes on error when the PO signal is high during data output.	Polarity is inverted.

6-5. 8251AC controls

There are two control words for the 8251AC.

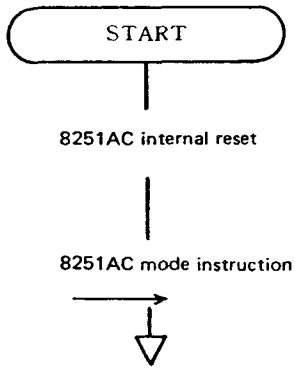
(1) Mode instruction: Defining general operational parameters, such as unit, stop bit, etc.

(2) Command instruction: Defining status words used for actual operation, such as send/receive enable, etc.

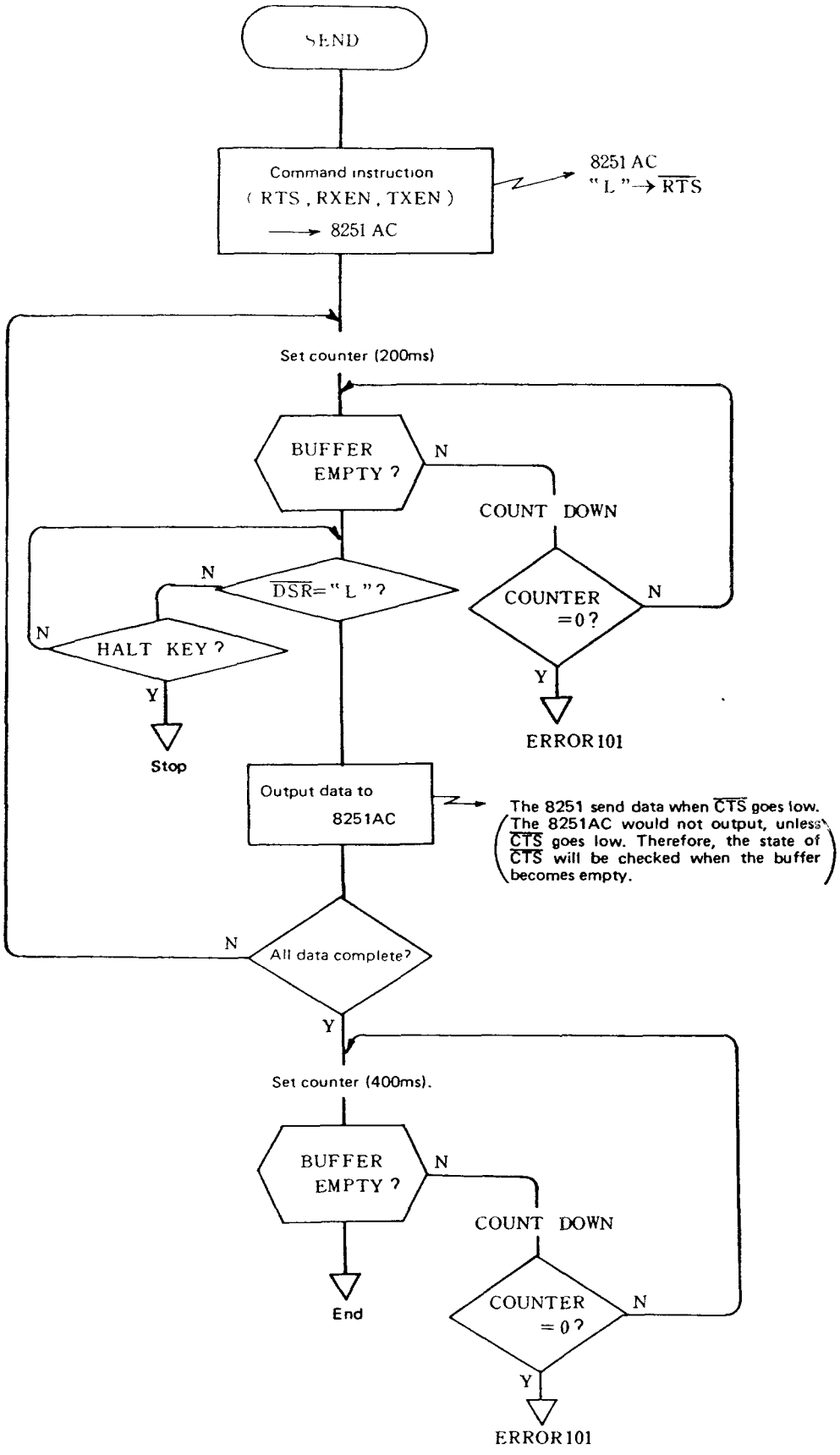
1) Definition of generation operational parameters

- Baud rate
- Character size
- Even/odd/off parity assignment
- Stop bit size

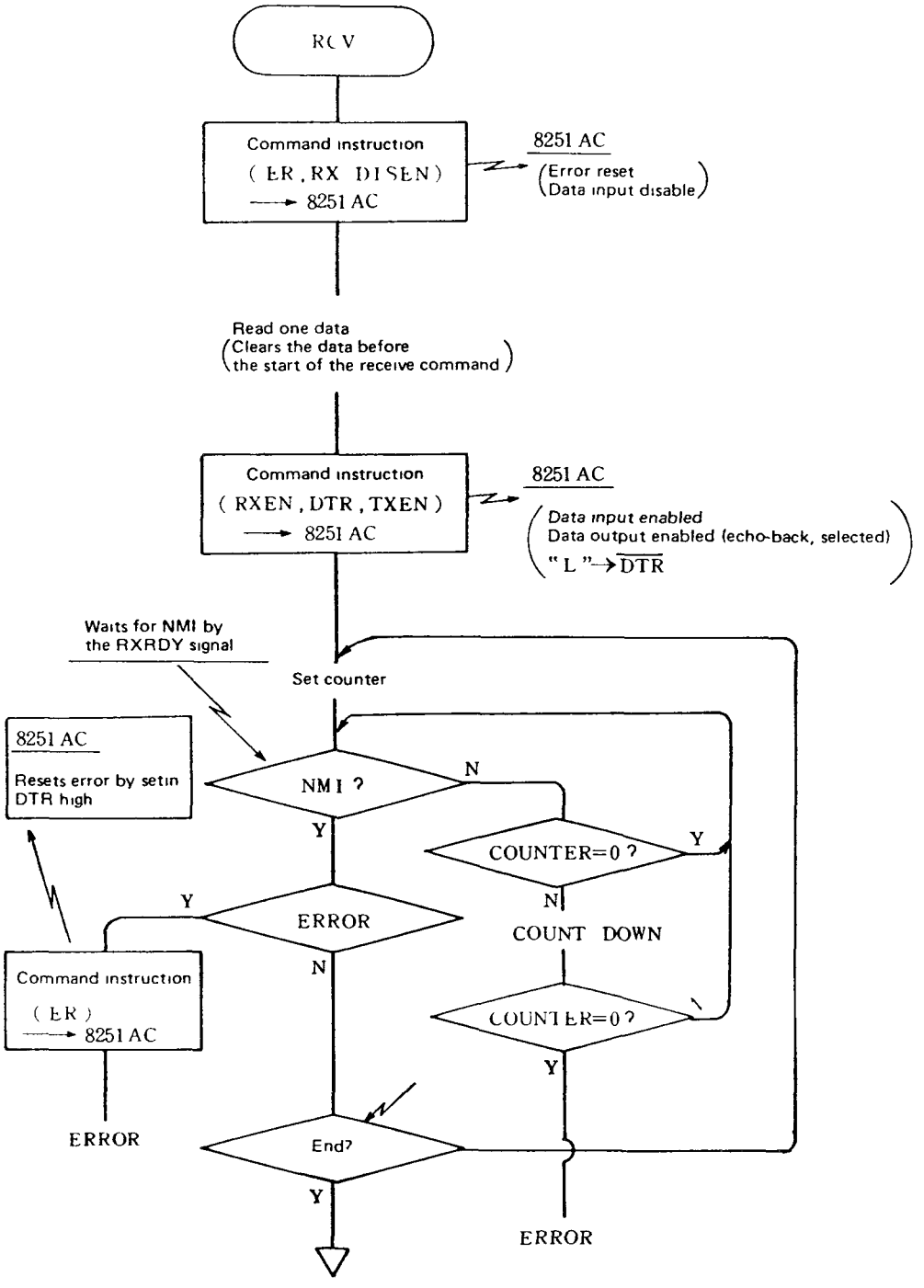
*Corresponds to channel command of BASIC.



2) Data output control



3) Data input control



6-6. 8253 Controls

Baud rate of this interface will be determined by the clock output of the 8253. The 8251 is configured such that its baud rate is 1/16 of the input clock and has the following relation between the 8253 output clock and the baud rate:

Baud rate	8253 Output frequency	8253 Parameter
110 ± —	1760Hz	13963 6
300	4800	512
600	9600	256
1200	19200	128
2400	38400	64
4800	76800	32
9600	153600	16

8253 input frequency: 2457.6kHz
8253 Mode set: Mode 3(rectangle waveform rate generator)

Control signals

Signal name	Symbol	IN/OUT	Function
Transmission enabled	CS	→ Peripheral	When high, data input from a peripheral is enabled. When low, data input from a peripheral is disabled.
Data set ready	DR	→ Peripheral	Goes high when power is on to the interface unit.
Carrier detect	CD	→ Peripheral	(SW6-ON) High at all times when power is on to the interface unit. (SW6-OFF) Goes high only when data is on output.
Ready	READY	← Peripheral	Data output from the interface is enabled. (ON) Data is output from the interface. (OFF) Waits for data output. NOTE: A maximum of two bytes are output after the signal goes from high to low state.
Equipment ready	ER	← Peripheral	Indicates that the peripheral is ready. It results in an error if low or open when data is sent from the interface. This signal will be invalidated when the SW5 is turned off.
Paper out	PO	← Peripheral	(SW7-ON) Causes an error if set high during data output. (SW7-OFF) Causes an error if set low during data output.

6-7. Description of LSI's

1) UPD8251AC (Programmable Communication Interface)

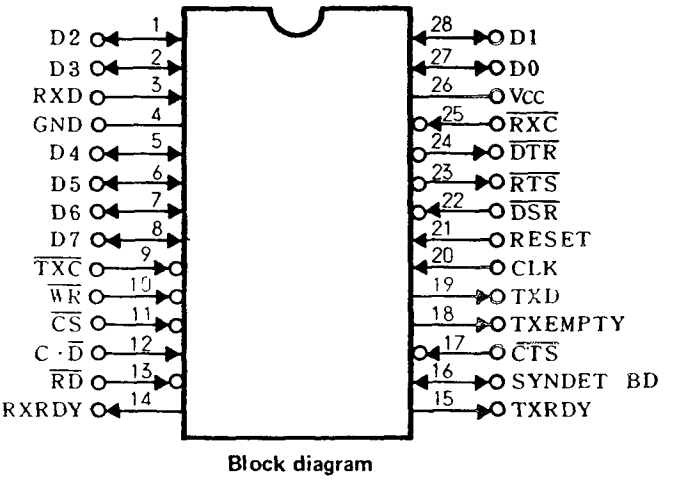
The UPD8251A is a USART (Universal Synchronous/Asynchronous Receiver/Transmitter that was specifically designed for data communication.

The USART receives parallel data from the CPU and converts it into serial data before transmitting. Also, serial data is received from an external circuit and transferred to the CPU after converting it into parallel. The CPU can monitor the current state of the USART at any time (data transfer error, and control signal of SYNDET and TXEMPTY.

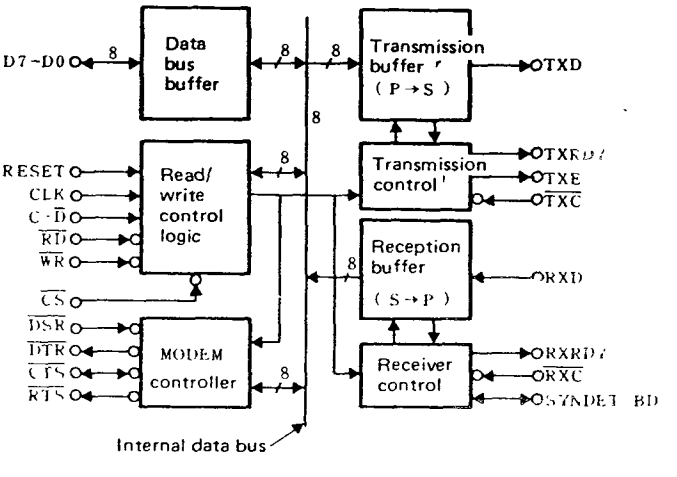
Features

- 8080A/8085A compatible
- Synchronous/asychronous operation
- Synchronous operation
  5 – 8 bits character
  Clock rate: baud rate x 1, x16, x64
  BREAK character generation
  Stop bit: 1, 1.5, 2 bits
  Error start bit detection
  Automatic break detection and operation.
- Baud rate: DC – 64K baud
- Full-duplex
  Double buffer type transmitter/receiver
- Error detect
  Parity, overrun, framing
- Input/output TTL compatible
- N-channel MOS
- Single +5V supply
- Single phase TTL level clock
- 28-pin, plastic DIP
- Intel 8251A compatible

Pin configuration (Top View)



Block diagram



D0~D7	Data Bas
RXD	Receive Data (IN/OUT)
WR	Write (IN)
RD	Read (IN)
C/D	Control/Data (IN/OUT)
CS	Chip Select (IN)
DSR	Data Set Ready (IN)
DTR	Data Terminal Ready (OUT)
RTS	Request to Send (OUT)
CTS	Clear to Send (IN)
TXRDY	. Transmitter Ready (OUT)
TXC	Transmitter Clock (IN)
TXE	. Transmitter Empty (OUT)
RXC	. Receiver Clock (IN)
SYNET/BD	: SYNC Detect/Break Detect (IN/OUT)

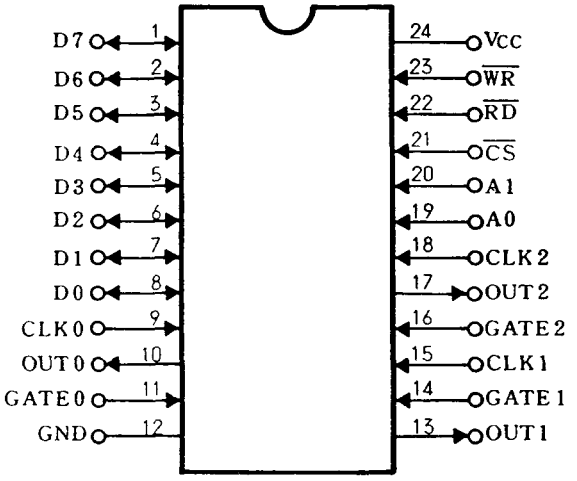
2) UPD8253C-5 (Programmable Interval Timer)

The UPD8253-5 is a programmable counter/timer specifically designed for the 8-bit microcomputer system. It consists of three sets of 16-bit counters that operate under a maximum counter rate of 4MHz. Timer and six operational modes are programmed to be used for a wide range of microcomputer system timing control.

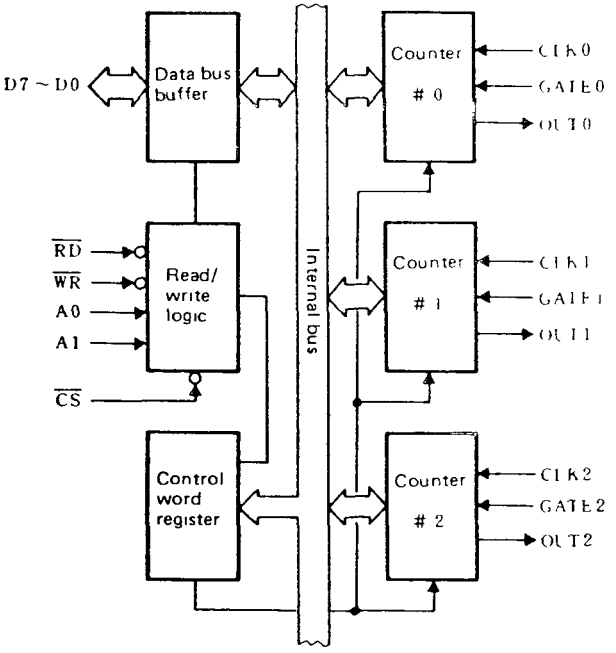
Features

- Z-80 compatible
- Three sets of 16-bit counters
- DC-4MHz of count rate
- Programmable six operational modes and timer duration
- Choice of binary counter/BCD counter
- N-channel MOS, input/output TTL compatible
- Single +5V supply, 24-pin DIP
- Intel 8253-5 compatible

Pin configuration (Top View)



Block diagram



D7~D0	Data Bus (8 bit)
CLKN	Counter Clock Inputs
GATEN	Counter Gate Inputs
OUTN	Counter Outputs
RD	. Read Counter
WR	Write Command or Data
CS	Chip Select
A1~A0	: Counter Select
Vcc	. +5 Volts
GND	. Ground

8251

8251 chip address[0001/xxxx] IN / OUT } #1X	CLK	IN	2.45MHz clock
	$\overline{DSR}$	IN	DATA SET READY ... READY
	$\overline{DTR}$	OUT	DATA TERMINAL READY ... CS
	$\overline{CTS}$	IN	CLEAR TO SEND ... PO (MPER SUT), ER
	$\overline{RTS}$	OUT	REQUEST TO SEND ... CD
	TXD	OUT	TRANSMITTER DATA ... RD
	TXRDY	N.C.	
	TXE	N.C.	
	$\overline{TXC}$	IN	TRANSMITTER CLOCK ... OUT 0 of 8253
	RXD	IN	RECEIVE DATA ... SD
	RXRDY	OUT	RECEIVER READY ... To sub-CPU of $\overline{NMI}$
	$\overline{RXC}$	IN	RECEIVE CLOCK ... 8253 OUT
	SYN/BD	N.C.	

8253

8253 chip address[0010/xxxx] IN # / OUT # } 2XH	CLK0	IN	2.45MHz
	GATE0	IN	Vcc
	OUT0	OUT	To $\overline{TXC}$, $\overline{RXC}$ of the 8251
	CLK1	IN	2.45MHz
	GATE1	IN	From OUT2
	OUT1	OUT	MUSIC
	CLK2	IN	2.45MHz
	GATE2	IN	Vcc
	OUT2	OUT	To GATE 1

$\overline{INT0}$ TO MAIN FROM SUB

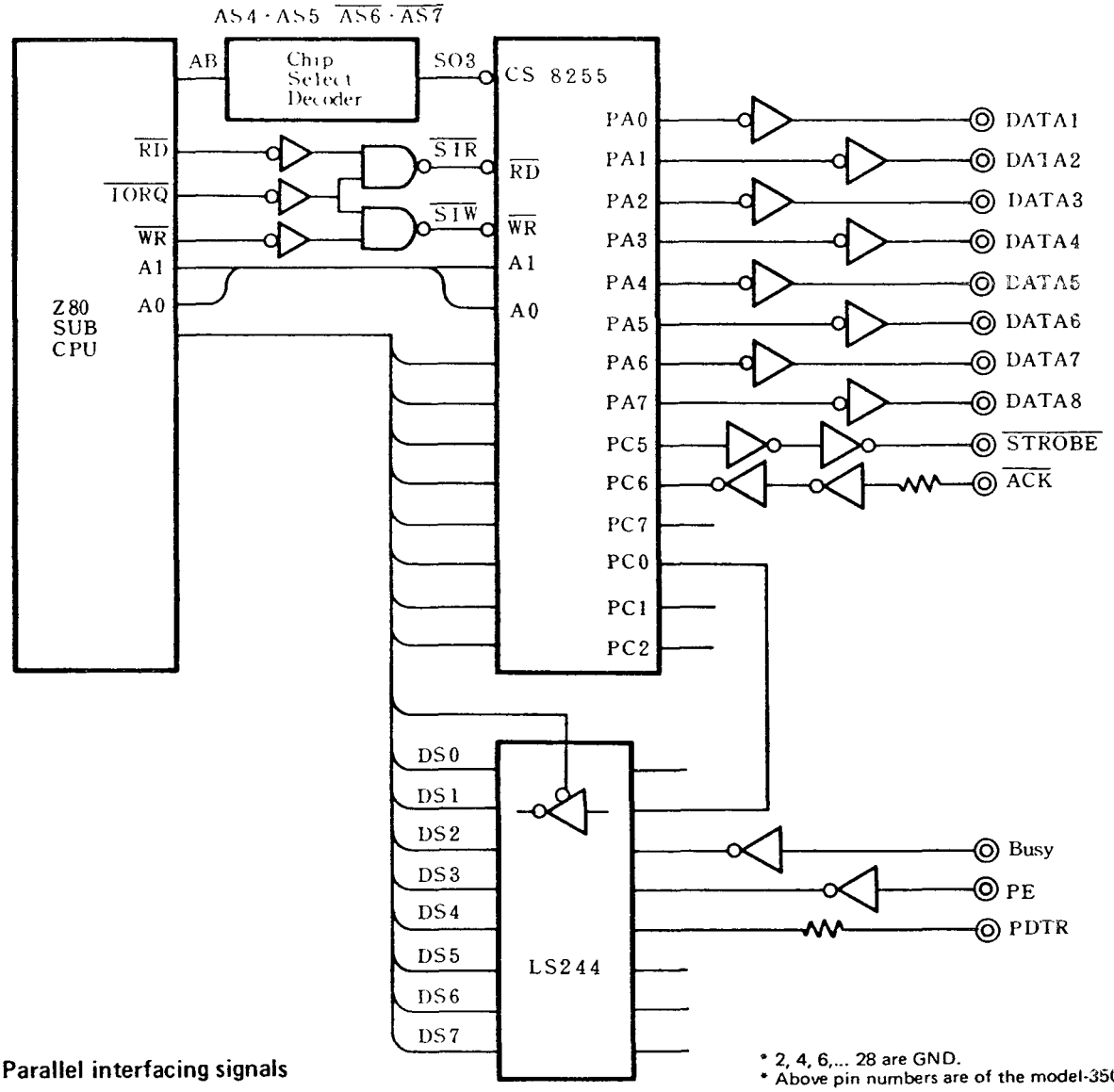
	$\overline{INT0}$
POWER ON RESET	H
SO0 · SIW($\overline{IORQ}$ · $\overline{WR}$ of SUB)	L
$\overline{INTR}$ = L (FROM MAIN)	H

$\overline{INT}$ TO SUB FROM KEY

STK = (L)

7. PRINTER INTERFACE

7-1. Printer interfacing circuit



7-2. Parallel interfacing signals

* 2, 4, 6,... 28 are GND.
* Above pin numbers are of the model-3500 main unit.

Pin No.	Signal name	IN/OUT	Function
1	$\overline{\text{STROB}}$	→ PRINTER	Data is transfered to printer when $\overline{\text{STROB}}$ is high.
3	DATA 1	→ PRINTER	Data output to the printer
5	DATA 2		
7	DATA 3		
9	DATA 4		
11	DATA 5		
13	DATA 6		
15	DATA 7		
17	DATA 8		
19	$\overline{\text{ACK}}$	→ PRINTER	Indicates the end of character input or function input
21	BUSY	← PRINTER	When high, it enables to receive data
23	PE	← PRINTER	When high, it indicates paper empty
25	PDTR	← PRINTER	When high, it indicates the SELECT mode (receive enabled).
27	SYSRES	→ PRINTER	Reset signal, normally high

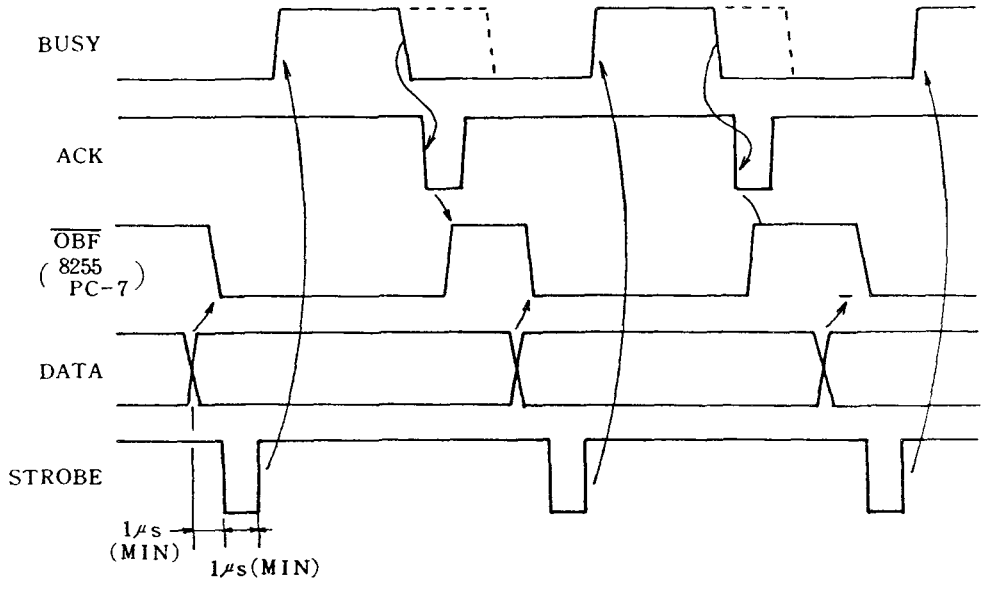
7-3. General description of the parallel interface

The 8255 is used for the LSI to control the parallel interface. The 8255 can be set in the following mode.

PORT A: MODE 0
PORT B: MODE 1
PORT C: Output

Because it is not possible to directly sense the ACK signal as it uses interrupt for key processing and RS232C input, the ACK signal is latched by means of the OBF pin function

7-4. Data transfer timing

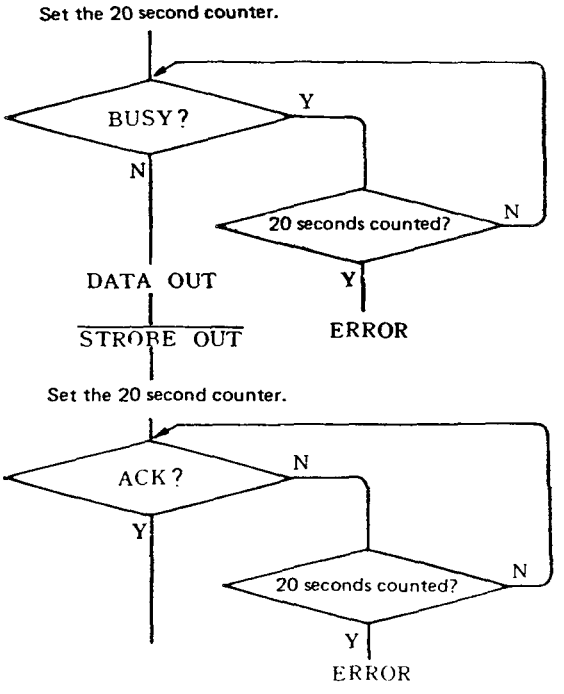


PRINTER: MZ-1P02, MZ-1P03 CE-330P, 331P, 332P

*Broken line in the above figure represents timing for the CE-330P and 331P.

*For detail of timing, refer to Manual provided with printer.

7-5. General description of control software



7-6. I/O port map

8255 ON SUB CPU BUS

IN / OUT #3X 8255 chip address[0011/xxxx] Group A: Mode 1 Group B: Mode 0	Group A	PA7	Output	DATA8	Printer
		PA6		DATA7	
		PA5		DATA6	
		PA4		DATA5	
		PA3		DATA4	
		PA2		DATA3	
		PA1		DATA2	
		PA0		DATA1	
		PC7	OBF output	ACK でSET	
		PC6	ACK input	ACK	
		PC5		STROBE	
		PC4		MUSIC, sustain	
		PC3	INTR	NOT USE	
	Group B	PC2	Output	ACKC	Keyboard
		PC1		STC	
		PC0		DC	
		PB7		P/M	CG selection
		PB6		SRDY	Sub CPU READY
		PB5		CLK	Clock
		PB4		Din	
		PB3		C2	
		PB2		C1	
		PB1		C0	
		PB0		STRB	

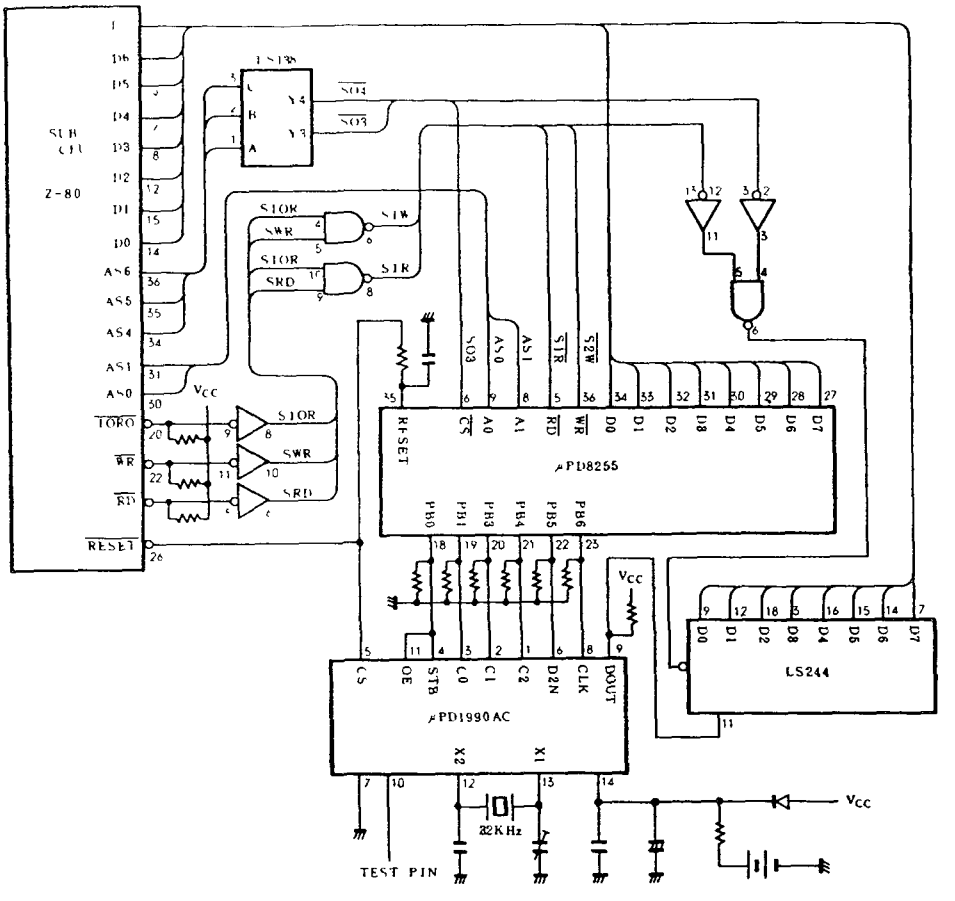
INPUT PORT〔74LS244〕

74LS244 port address[0100/xxxx] IN / OUT #4X	〔DS7〕	HLT KEY	
	〔DS6〕	STK	Keyboard
	〔DS5〕	DK	
	〔DS4〕	PDTR	Printer
	〔DS3〕	PE	
	〔DS2〕	BUSY	
	〔DS1〕	Reads the 8255 OBF (PC7)	
	〔DS0〕	output or timer output.	

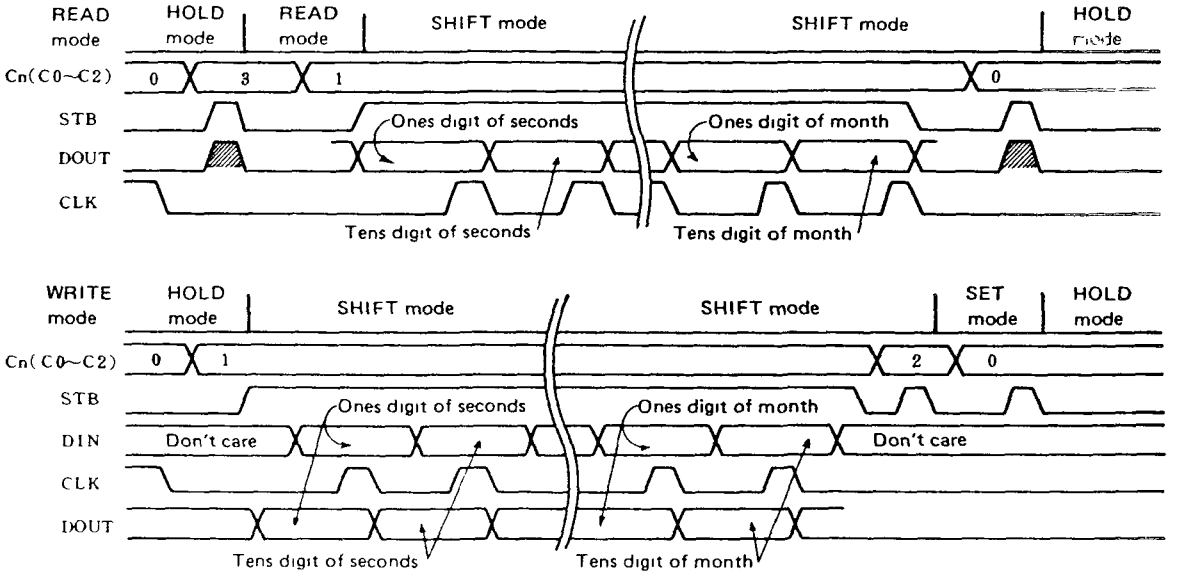
8. OTHER INTERFACES

8-1. Clock circuit

1) Schematic

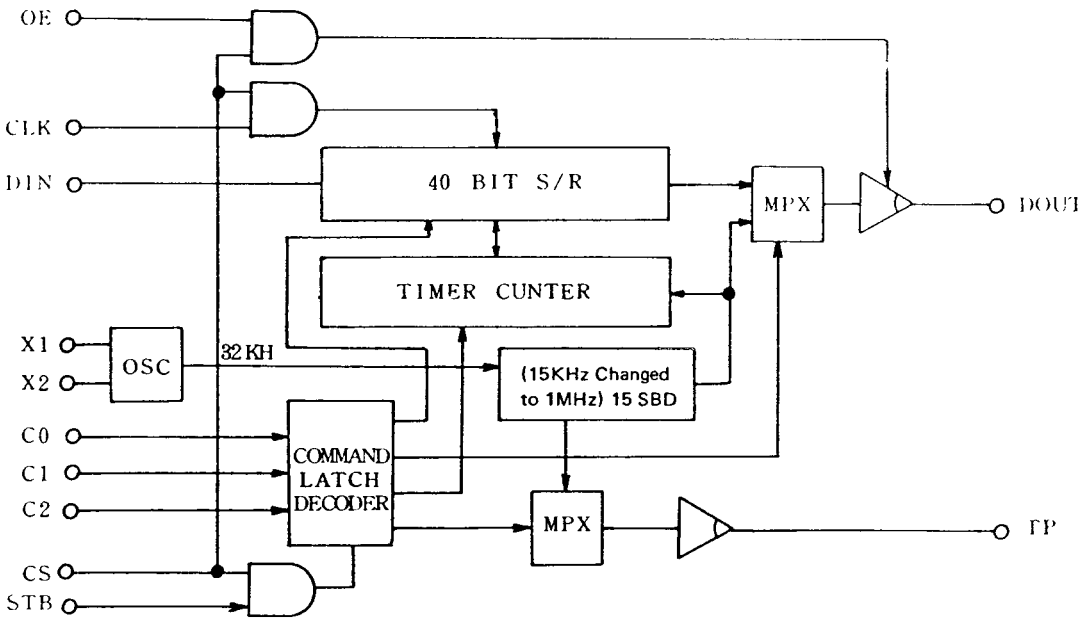


2) Clock timing



3) μPD1990AC

Block diagram

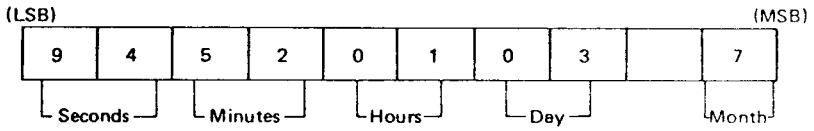


Command specification

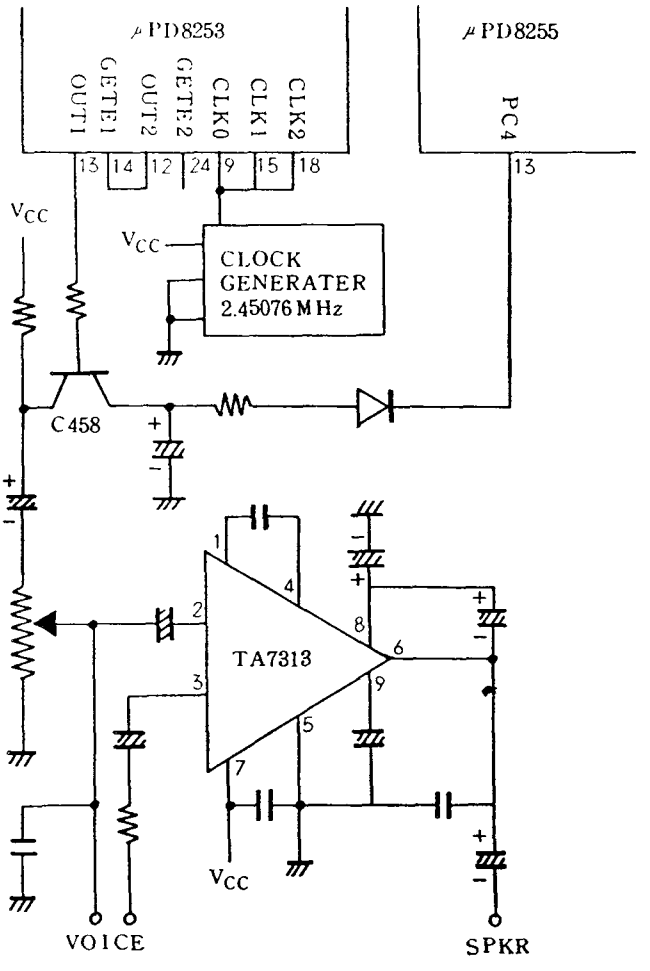
C2	C1	C0	Command	Description	DOUT	Data Shift	Note
0	0	0	Register hold	Holds 40-bit S/R	1Hz	Not possible	Data retention
0	0	1	Register shift	Data input/output	[LSB] Output of LSB	Possible	Shifts in synchronization with the clock
0	1	0	Time set	Data of the 40-bit S/R is preset to the time counter.	[LSB] Output	Not possible	
0	1	1	Time read	Data in the time counter is read to the 40-bit S/R.	[LSB] Output	Not possible	

Input/output format

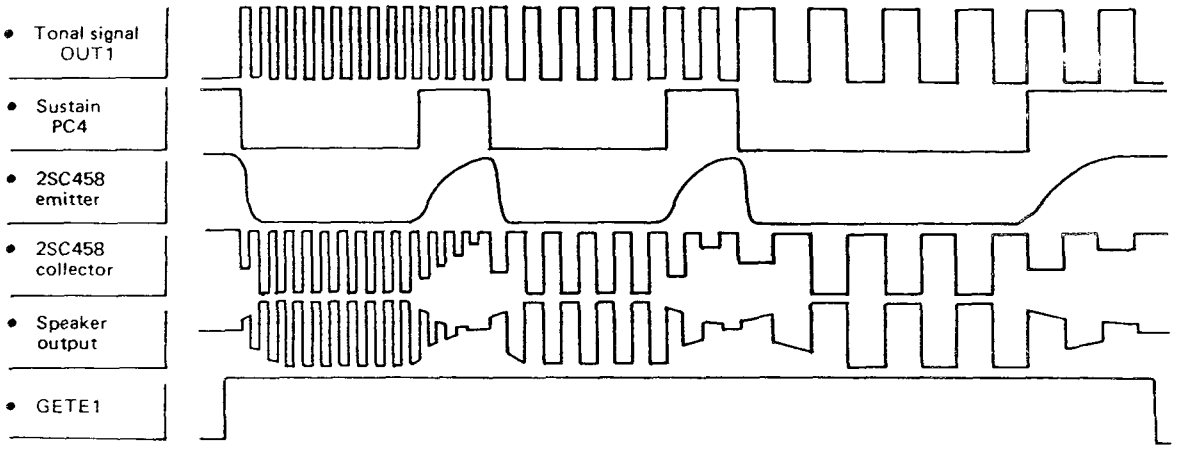
Example: In the case of 10 o'clock, 25 minutes, 49 seconds, July 30th.



8-2. Voice input/output circuit



Music output waveform



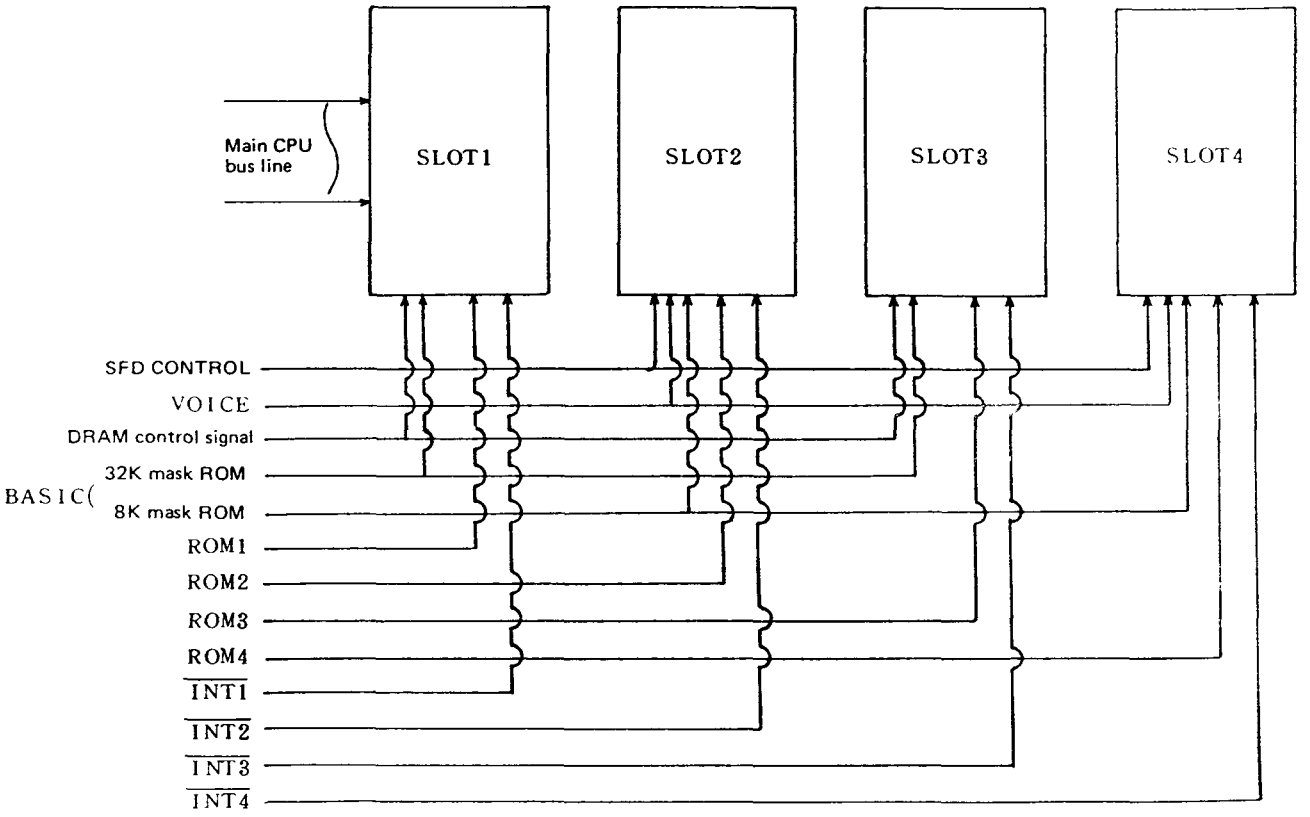
8-3. Expansion and interrupt (See 3-(2)-4 for interrupt)

1) Options and expansion units

Options not requiring expansion unit			
MZ 1K01	JIS keyboard	MZ-1E01	RS232C 1/F Ⓘ
1D01	14" medium resolution color CRT	-1E02	GP I/O Ⓟ
1D02	12" high resolution green CRT	-1E03	SFD 1/F
-1D03	12" high resolution color CRT	-1F05	SFD unit
-1S01	14" CRT tilt stand	-1R06	RAM
-1S02	12" CRT tilt stand		
-1X02	Light pen		
-1P02	80-character printe		
-1P03			
-1P04	Color injket printer		
CE-330P	80-character printer		
-333P	136-character printer		
-331M	Optional MFD drive unit		
-330X	Plotter		
MZ-1F02	Optional MFD drive unit		
-1F03	Optional MFD drive unit (single deck)		
-1R03	Graphic board		
-1R05			

2) Expansion unit

Signal assignment by slot



8 4 System SW1 (DIP SW) (User operative through the cabinet bottom)

No	Signal name	Function	Position	Polarity	Description	
1	SW1	Printer select	ON	L	SW2 ON, SW1 ON: CE332P SW2 OFF, SW1 ON: MZ1P02 SW2 ON, SW1 OFF: IO2824 SW2 OFF, SW1 OFF: –	#47 pin of MMR
			OFF	H		
2	SW2		ON	L		#48 pin of MMR
			OFF	H		
3	SW3	CRT select	ON	L	High resolution CRT (MZ1D02, MZ1D03)	#51 pin of MMR
			OFF	H	Medium resolution CRT (MZ1D01, MZ1D06)	
4	SW4	Choice of decimal point output format	ON	L	A period is output for a decimal point	#52 pin of MMR
			OFF	H	A comma is outputted for a decimal point	
5	SW5	RS232C assign	ON	L	Low state or open ER signal during data output will result in an error	To $\overline{CTS}$, $\overline{DSR}$ of the 8251
			OFF	H	The signal ER becomes invalid	
6	SW6		ON	L	CD is high as long as power is on to the main unit	
			OFF	H	CD goes high only during data output However, it would not go high if the echo back function is on the host side	
7	SW7		ON	L	An error is cause when the PO signal is high during data output	To $\overline{CTS}$ of the 8251
			OFF	H	Polarity is inverted for the above	
8	FD1 (SW8)	Key shift mode setup	ON	L	Normally in capital letter, but in small letter when shifted	#54 pin of MMR (FD1)
			OFF	H	Normally small leter and in capital letter when shifted	
9	P/M (SW9)	Choice of CG for display	ON	L	3500 CG will be assigned when the 200 raster CRT is in use	P/M signal (To A3 CG)
			OFF	H	2000 CG will be assigned when the 200 raster CRT is in use	
10						N C

Dip switches (A) and (B) located on the PWB are used for servicing the MFD or for other machine service and there fore the user is not supposed to use these switches In addition, these switch must be used when either the CE 330M or 331M is used as the expansion MFD

DIP SW (A)

No	Signal name	
1	SEC (SW1A)	44 pin of MMR
2	FD2 (SW2A)	56 pin of MMR
3	FD3 (SW3A)	58 pin of MMR
4	SRQ (SW4A)	Bus request to sub-CPU

1	2	3	
OFF	OFF	OFF	When SH in use
ON	OFF	OFF	When DH in use
OFF	ON	OFF	–
ON	ON	OFF	–
OFF	OFF	ON	Use of the CE330M as an expansion unit
ON	OFF	ON	Use of the CE331M as an expansion unit
OFF	ON	ON	Check mode *1
ON	ON	ON	Check mode *2

*1 Test program is loaded and executed

*2 Provided for the test of the MFD interface The read/write test is carried out for the expansion unit

DIP SW (B)

No	Signal name	
1	SRES (SW1B)	SUB CPU reset signal
2	SW2B	SUB CPU BUS select signal

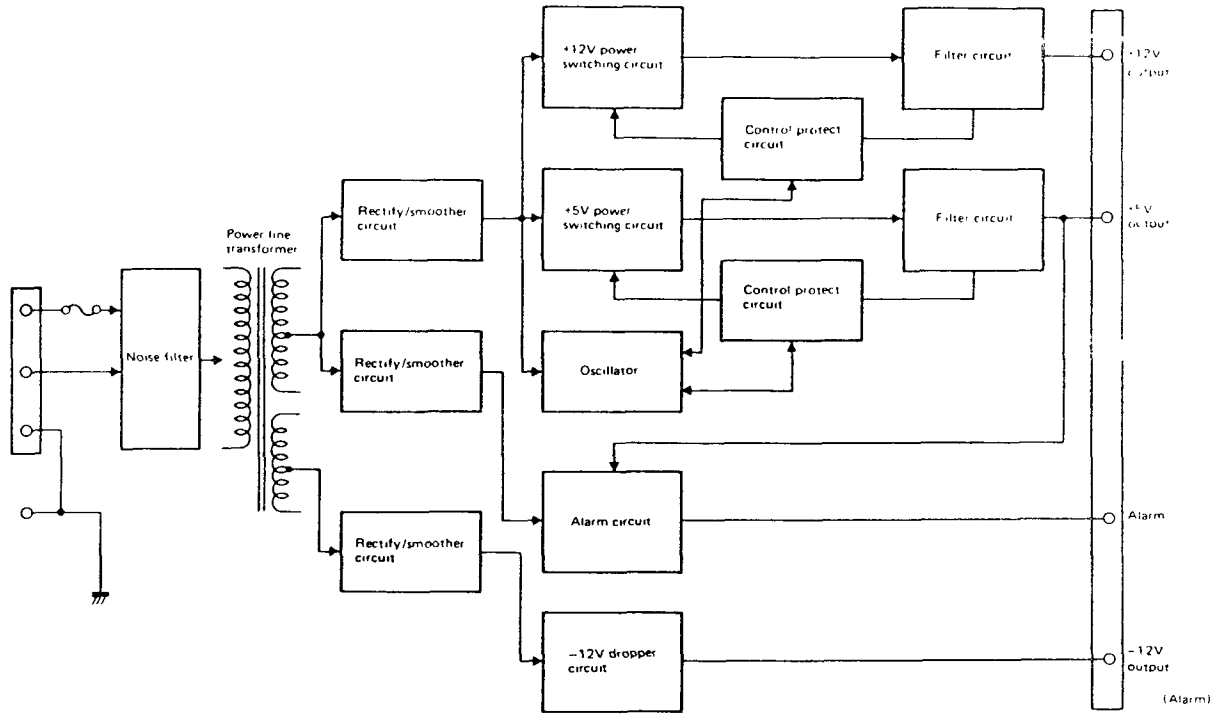
Used for an individual test of the CPU PWB When these three switches are turned off altogether, it makes the sub CPU operated independently To be used in th ON condition under a normal situation

DIP SW(A)				DIP SW(B)		
1	2	3	4	1	2	
OFF	OFF	OFF	ON	ON	ON	Switches are set in this manner before shipment of machines this us the single-sided minifloppy disk drive.
ON	OFF	OFF	ON	ON	ON	Switches are set in this manner before shipment of machines that use the double-sided minifloppy disk drive. (MZ3530, PC3541 MZ3540, YX3541
OFF	OFF	ON	ON	ON	ON	Switches are set in this manner when the SH is used for the optional MFD
ON	OFF	ON	ON	ON	ON	Switches are set in this manner when the DH is used for the optional MFD
OFF	ON	ON	ON	ON	ON	Test mode *1
ON	ON	ON	ON	ON	ON	Test mode *2
☒	☒	☒	OFF	OFF	OFF	Individual CPU PWB test

☒ Can be in either state

9. POWER CIRCUIT DESCRIPTION

1. BLOCK DIAGRAM



(Block diagram)

A. +5V and +12V supplies

1. Functions

a. Supply voltage is first rectified in the rectifier circuit and sent out to the switching regulator via the overcurrent detector provided in the overcurrent protect circuit.

b. Next, the voltage is converted to the +5/+12V output in the switching regulator and sent out to the noise filter.

c. Change in the switching regulator output voltage is sensed by the control circuit and is fed back to the switching regulator after being amplified in the amplifier located in the control circuit, for maintaining the output voltage to a constant level.

d. The signal from the oscillator is supplied to the switching regulator through the control circuit for driving the switching regulator.

e. For prevention of overcurrent, the protect circuit is used for stopping the oscillator when an overcurrent is met, and it makes the switching regulator to halt in order to shut off +12V/+5V supply.

2. Description of each block

a. Overcurrent protect (control/protect) circuit

When an overcurrent is met in the +5V/+12V circuit, it causes to increase the voltage at both ends of the overcurrent detector resistor R1, which in turn causes to increase the Q3 collector current, for, there arises larger voltage difference between the emitter and base of the transistor Q3. This makes the gate voltage of the thyristor increased owing to activation of SR. With activation of SR it makes the oscillator voltage dropped to the GND level at the point "a" to stop oscillation, which also makes the switching regulator stopped by the deactivation of the transistor Q5 oscillation. This causes the transistor Q5 inactive, and it shuts off the +5V/+12V supply.

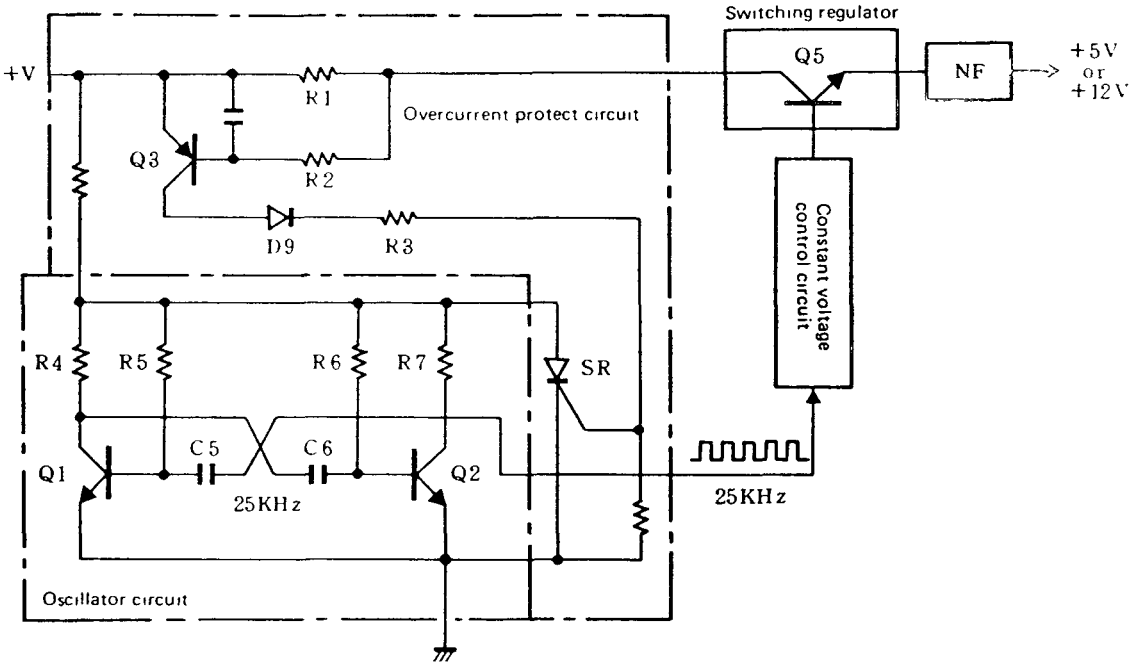
b. Oscillation circuit

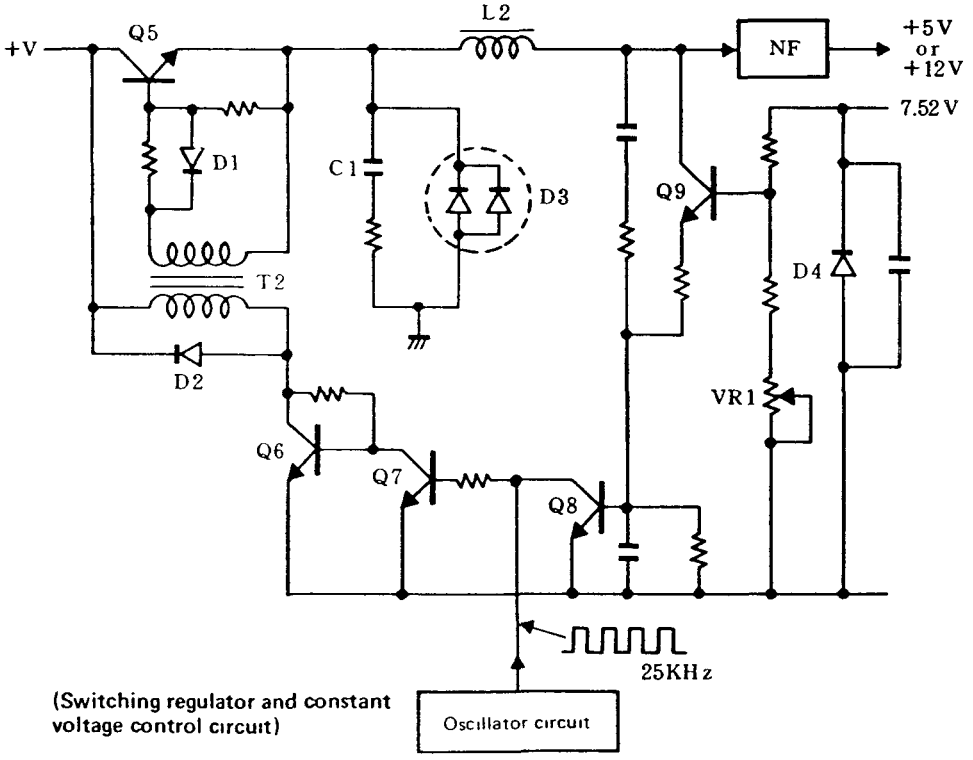
As the Q1 emitter voltage is at almost GND level when the transistor Q1 is active, the Q2 base voltage temporarily drops close to the GND level by means of C6, which in turn makes Q2 inactive and the Q2 emitter voltage increases.

Then, the Q2 base voltage comes to rise as C6 begins to be charged through R6, and the transistor Q2 starts to activate again. With activation of the transistor Q2, the Q2 emitter voltage starts to drop and the Q1 base voltage is temporarily dropped by means of C5, to shut off the transistor Q1, which causes to increase the transistor Q1 emitter voltage.

Next, as C5 is charged by R5, it makes the Q1 base voltage increased which puts the transistor Q1 into activation. In this manner, transistors Q1 and Q2 are alternately turned on and off to keep oscillating.

C5 and C6 are charged through R5 and R6 by on/off action of the Q1 and Q2, and discharged through Q1 and Q2.





(Switching regulator and constant voltage control circuit)

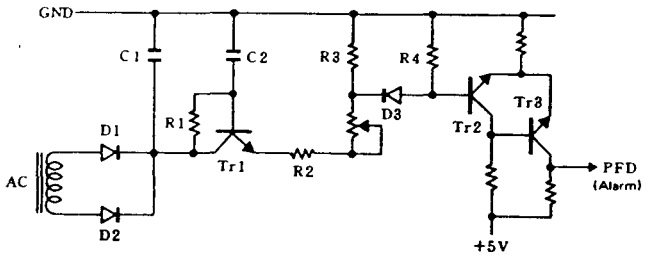
- VR is the +5V or +12V adjusting VR.
- D_3 is provided to discharge current from C_1 after power off.

c. Power switching circuit

As the signal from the oscillator is amplified through Q7 to Q6 to change current to the transformer T2, it causes voltage to appear on the base of Q5 (one of components is cut by D1), so that the transistor Q5 begins to perform switching operation in synchronization with the oscillation frequency. As Q2 is switched, current is supplied to the emitter side of the transistor Q5, which produces smoothed voltage through the capacitor C1 and the coil L2. The circuit composed of D4 and VR1 is the reference voltage for the +5 or +12V supply, which is used to control the emitter current flowing to the transistor Q9. The current supplied from Q9 is used to create Tr3 inactive by the delayed C1 and C2 voltages which supplied from Tr1-R2-VR1-D3. It goes high with deactivation of Tr3.

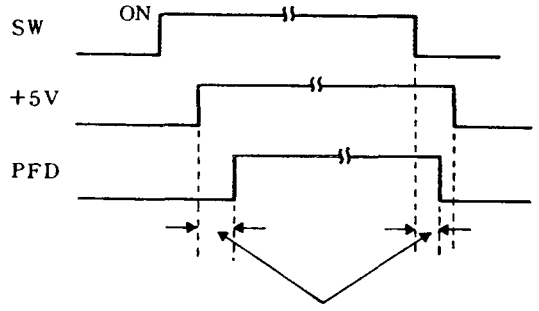
3. Alarm circuit

(Alarm generation circuit)



When power turns off, the voltage accumulated in C1 and C2 are supplied to the base of Tr2 via Tr1 ... and D3, so that Tr2 is kept active and Tr3 inactive for sometimes after power off.

Timing chart



10. MZ1K01 KEYBOARD CONTROLLER CIRCUIT DESCRIPTION

10-1. Specification of keyboard control

1) Input Buffer

Capacity: 64 bytes

- Key-in data is written to the input buffer first, and is supplied to the CPU, byte by byte.
- When an overflow is detected, the overflow code is affired to the key-in data already sent, before being sent to the CPU.

2) Rollover

- 2 key rollover (exemption in the CTRL mode)
  (Entry of the second key depression can be accepted even if more than one key is pressed at same time.)
- Simultaneous depression of more than three keys is ingnored.

3) Key bounce

15msec (Key spec is 5-10msec)
(Indicates unstable state as shown in Fig. 3-2 that key signal does not turn off immediately after releasing of finger from the key.)

4) Key

5msec (norma), 20msec (max),
15msec (allows for key bounce)

5) DEF Key

Twenty definable keys are available in combination with the CTRL key.

DFK1~DFK10 ——— (DEF1A~DEF10A)
DEF1-DFK10 in conjunction with the CTRL key
--- (DEFIB-DEF10B) —— (DEF1B~DBF10B)

6) Handling of functional symbols and graphic symbols

See the code table.

7) Use of the CTRL key to discriminate RUN and CONT of the DEB key.

Push the DEB in conjunction with the CTRL key to start running.

8) Handling of special codes

COPY command: CTRL [1] (ten key)
ESCape ——— CTRL [CMD]
BRK ——— CTRL [CONT]

9) PRO/OP

Sent to the CPU after power on and when PRO/OP is changed.

10) HOME key

CTRL [HOME] Returns home after clearing the display screen.
[HOME] Only the cursor returns home.

11) One-step commands

CMD 1 ——— DISP
CMD 2 ——— PRINT
CMD 3 ——— INPUT
CMD 4 ——— USING
CMD 5 ——— IMAGE
CMD 6 ——— GOTO
CMD 7 ——— GOSUB
CMD 8 ——— RETURN
CMD 9 ——— LIST
CMD 0 ——— SEND
CMD A ——— AUTO
CMD C ——— CLOSE
CMD D ——— DATA
CMD F ——— RFORMAT#
CMD K ——— KEY IN
CMD L ——— LOAD
CMD O ——— OPEN
CMD R ——— READ
CMD S ——— SAVE
CMD U ——— CURSOR

12) Mode indication on LED

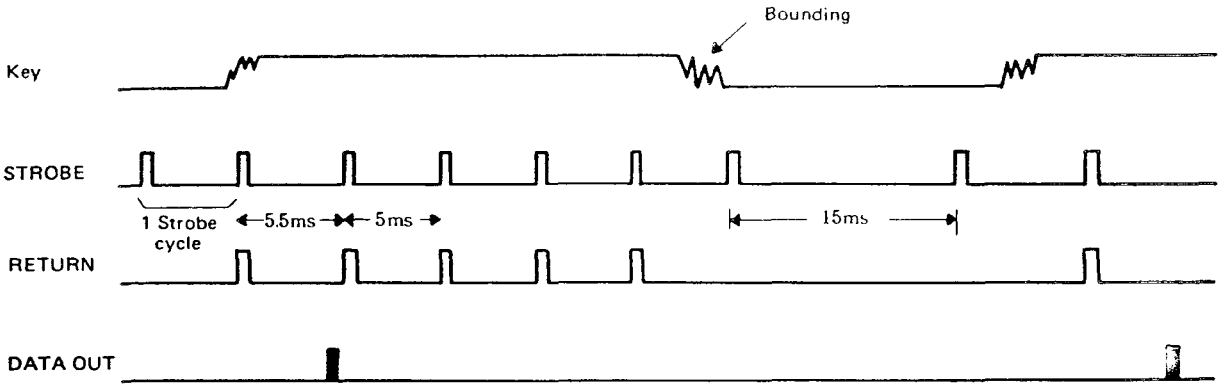
ASCII ——— LOCK

13) REP

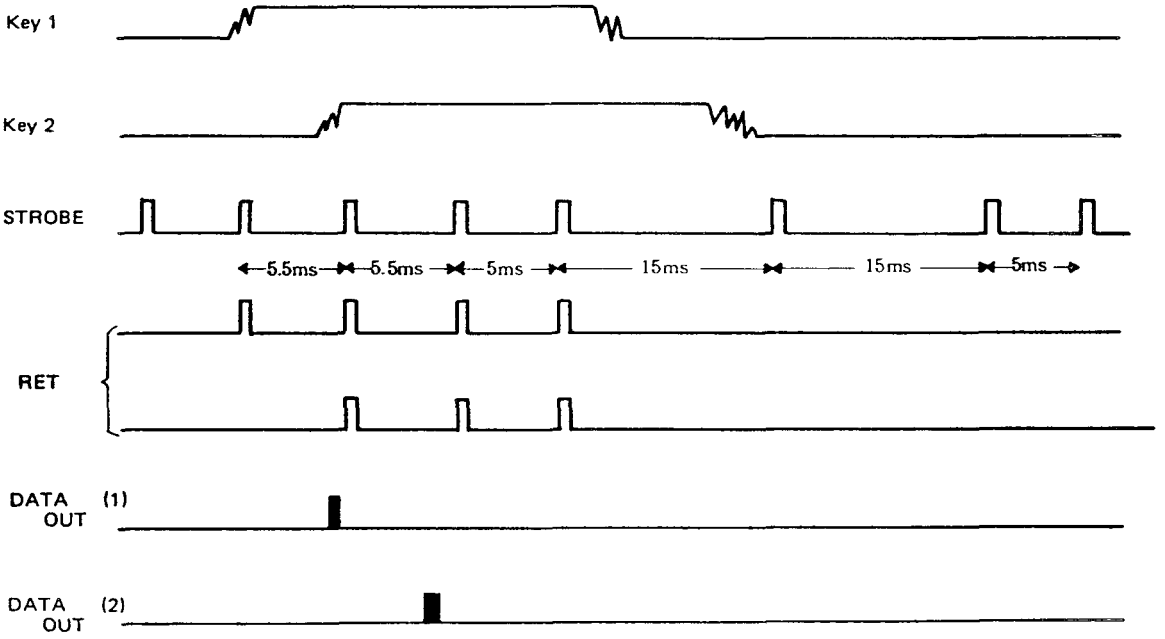
Key repetition will take place when a key depressed for more than 0.64 second. Entry of other keys is permitted during key repetition. When two keys are depressed at the same time, an alternate key entry will not be accepted. This rule does not apply to simultaneous depression of more than three keys.

10-2. Key search timing

Single key entry

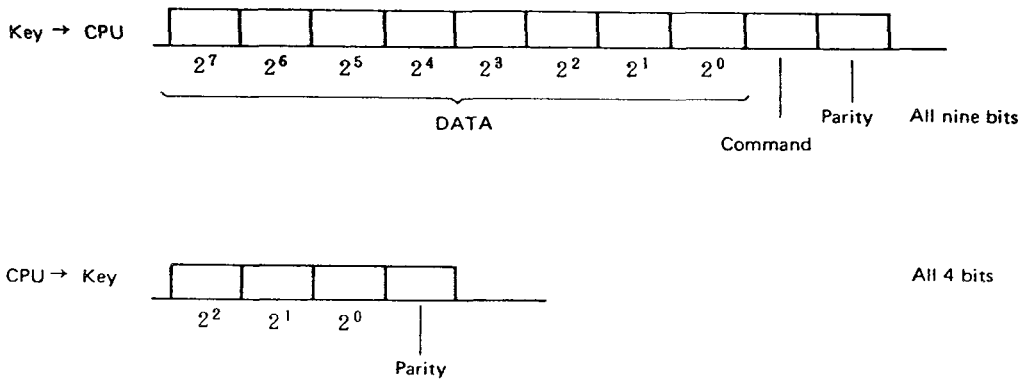


Two key entry



10-3. Key serial transmission procedure

1) Data format



- Command flag: "0" when succeedeing 8 bits are a key data. "1" when it is a command or a graphic control data.
- Data: Positive logic (negative logic on the cable)
- Parity: Odd parity up to 27 bit from the correction flag.

2) Interfacing signals CPU level

- D(K): Output data from the keyboard. Positive logic
- ST(K): D(K) strobe signal. Also use for interrupt to the CPU. Active H
- ACK(C): Acknowledge signal form the CPU. Also use for the data transfer interrupt disable signal. Active H
- D(C): Output data from the CPU. Positive logic
- ST(C): D(C) strobe signal. Also use for interrupt to the keyboard side. Active L

3) Protocol

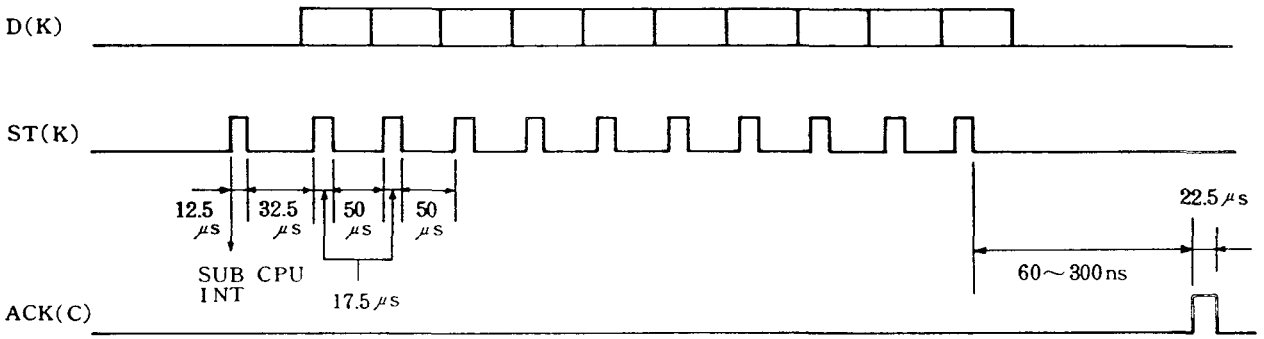
Key to sub CPU

- Keyboard to the sub-CPU data transfer tapes place with interrupt applied at every signal word (STK).
- As the sub-CPU detects a next strobe (STK) after going into the interrupt routine, it read data (K) as far as the final parity bit, and the ACK (C) signal is sent back to the keyboard side when the check-sum is correct.
- If the ACK (C) signal returns with normal timing, the keyboard controller accepts it. Unless the ACK signal was detected, the same data is sent again assuming a transmission error.
- Case when the error data link (sub-CPU not enable to receive data properly) is established.
  1) When parity error is found after the check-sum test.
  2) When the sub-CPU is in execution of the NMI routine or when NMI is applied during data transfer.
  3) When an error is detected in the couting of strobe (STK(K)) due to noise.

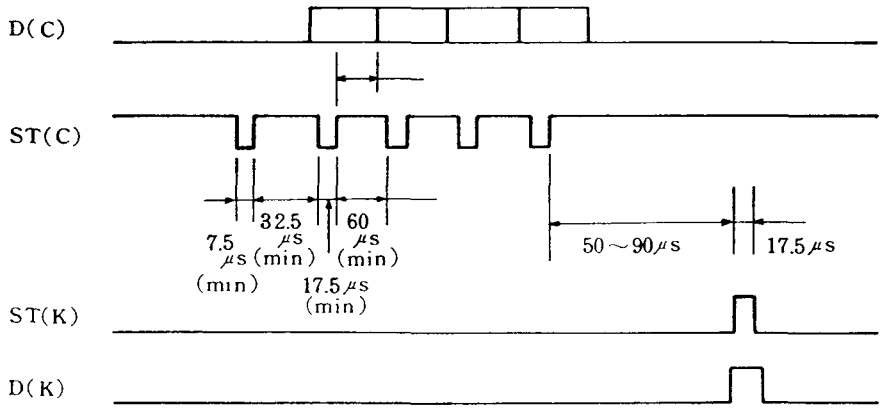
  When one of above conditions is detected, data will be sent again until received correctly. Key entries during this periode are strobe in the key buffer. Should the key buffer overflow, key entry will not be stored in the key buffer.
  - When a key buffer overflow is detected a KBOF error code is inserted in the area vacant immediately after transmission of one key-in data, without clearing key buffer contents.

SUB-CPU TO KEYBOARD

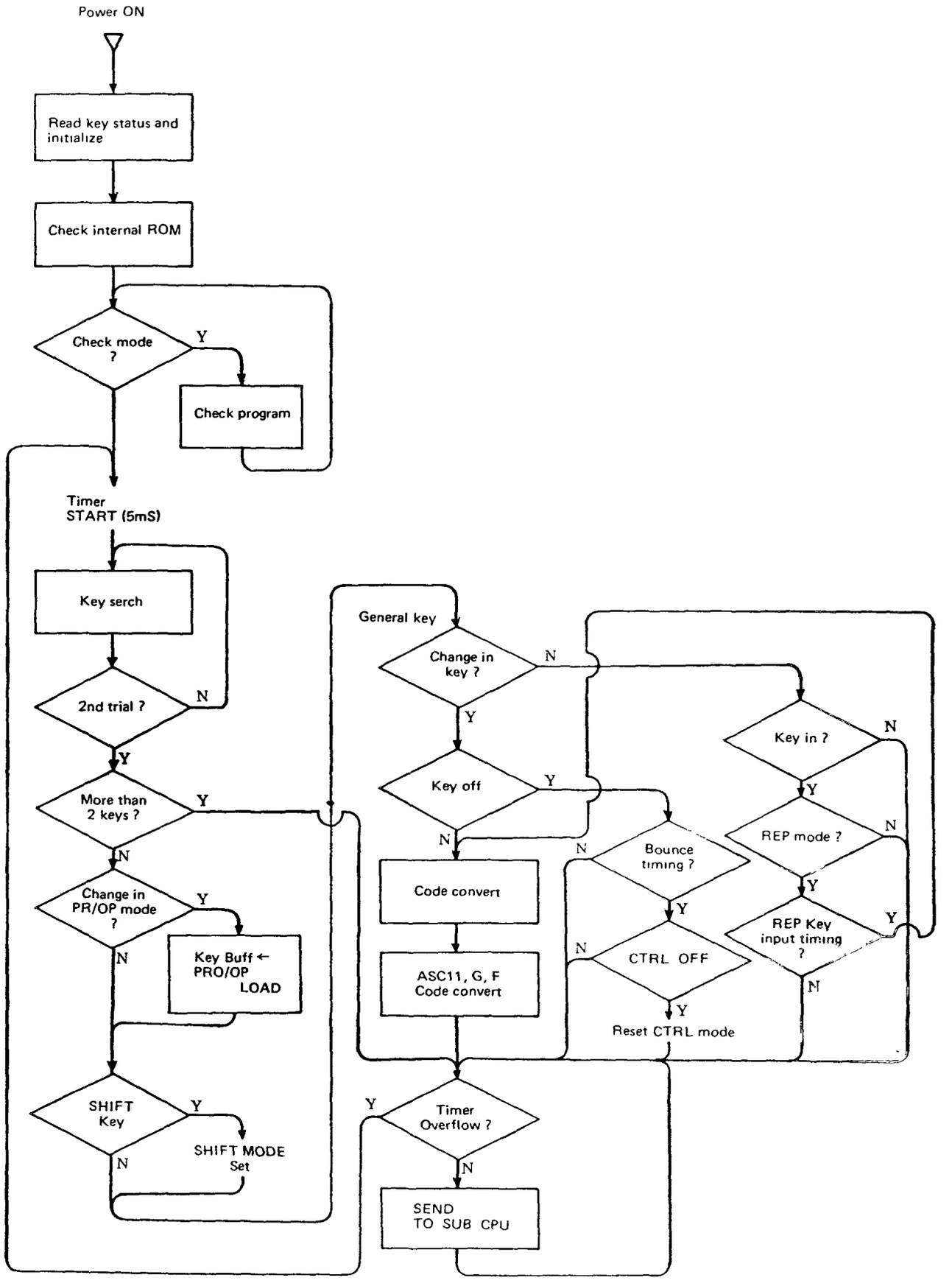
- Basically the same as the above cases.
- Data is 3 bits plus parity bit.
- Return acknowledge pluse: Parity OK . . . STK + DK
  Parity NO . . . STK only
- KEY TO CPU (80C49, Z-80) CPU level



- CPU → KEY



10-4. Keyboard controller basic flow



10-5. keyboard controller signal description

PIN No	Porality signal name	IN/OUT	Function
1	T0	IN	Output data signal from the sub CPU (D(C))
2	XTAL1	IN	Internal clock oscillator crystal input
3	XTAL2	IN	Internal clock oscillator crystal input
4	RESET	IN	Processor initialize
5	SS	IN	+5V
6	INT	IN	Strove of D(C) that also is used for interrupt to the keyboard side (ST(C))
7	EA	IN	GND
8	RD	–	NC
9	PSEN	–	NC
10	WR	–	NC
11	ALE	–	NC
12 ~ 19	DB0 ~ DB7	IN	RETURN signal from the keyboard is input when a key is pushed during key search
20	GND	IN	0V supply
21	P20	OUT	Output data signal from key (D(K))
22	P21	OUT	Strobe of D(K) which also is used for interrupt to the CPU side (ST(K))
23 24	P22 P23	IN	Not used
25	PROG	–	NC
26	V_{DD}	IN	+ 5V
27 ~ 30	P10 ~ P13	OUT	Strobe to the keyboard unit by which a hexadecimal code is sent out for generation shift pulses to terminals X0 X15 of the 4515 decorder during key search
31	P14	–	NC
32 ~ 34	P15 ~ P17	OUT	Pins used to activate the keytop embeded LED #32 pin Alphabets and symbols (LOCK) #33 and #34 are not used
35	P24	IN	Not used
36 ~ 38	P25 ~ P27	IN	Keyboard type identifier pin Keyboard type is identified by mears of KS0, KS1, KS2 of KUC1 an KUS2, whether it is GND or NC
39	T1	IN	Acknowledge input from the CPU (ACK(C)) Sent only when the CPU receives a correct data
40	V_{CC}	IN	+5V supply

11. SELF CHECK FUNCTIONS

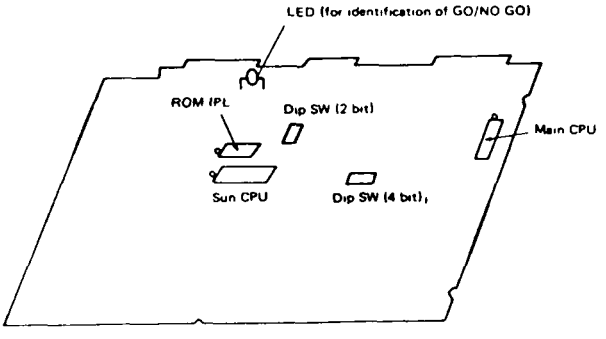
The -3500 performs self-check test during initial program loading of the ROM. 11-1.

Test regarding the main CPU

1) MFD I/F, 128KB RAM, 16KB ROM (for ROM based machine) checks

[Procedure]

1. Turn on all dip switches of the 4 bit switch (located in the middle of the front side of the board) and turn on all dip switches of the 2 bit unit on the front side of the board.
2. Insert a floppy disk into drive unit No 2 (the third drive unit)
3. Turn the power on
4. The LED flickers for a moment then the test program starts During execution of the test program, the LED stays unlit About four seconds later the result is indicsted



(DISPLAY)

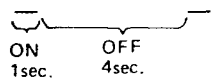
(1) LED comes activated after normal ending of the test

(2) LED flickers after abnormal ending of the test

The kind of error can be known by how the LED is activat ed and flickered

Type of error

① MDF 1/F error



② SD0 read/write error

③ SD0 bank alternation error

④ AD2 bank alternation error

⑤ AD3 bank alternation error

⑥ ROM sum-check error

⑦ Option RAM read/write error
(Indicated even when the option RAM is not in use)

⑧ Option RAM bank alternation error

NOTES:

1. The MFD I/F will not be tested, if there is no MFD I/F connected or when the diskette was not inserted in the slot of the drive unit No.2.
2. ROM test will not be performed, unless it is a ROM based machine.

2) Loacing check program

The test program is loaded from the specified track and sector to start executing the test.

[Procedure]

(1) Set dip switches on of the 4 bit unit located in middle of the front side of the board as illustrated at the right.

No.	1	2	3	4
POSITION	OFF	ON	ON	ON

(2) Set dip switches on of the 2 bit unit located on the front side of the board.

(3) Insert the media into a slot of any diskette drive unit.

(4) Turn the power on

(5) Load the program from the specified track and sector, to start execution of the test program.

[Conditions required for the drive unit and media]

(1) Use the FD-55B for the diskette drive unit.

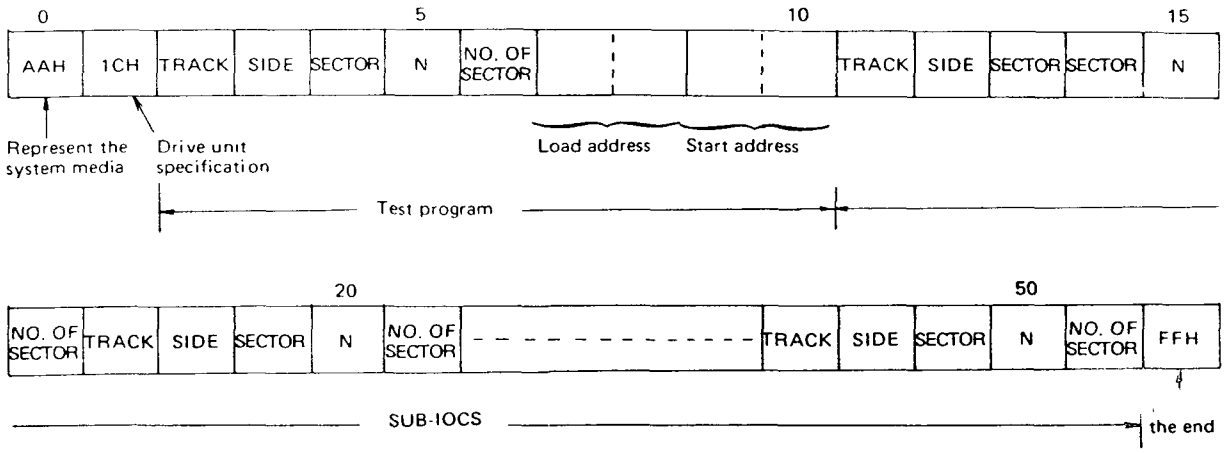
(2) Program may exist in any sector of any track, provided that it is written in continuous sector within a same track.

(Max. 256 bytes x 16 sectors = 4K bytes)

(3) Data descrived next should have been written on Sector 1 of Track 0.

(4) Program loading address must be 4800H and higher

- Sector 1, Track 0 information



N = { 0 Single dencity (Track 0)
1 Double density (other than Track 0)

SIDE = { 0 SIDE 0 (front side)
1 SIDE 1 (reverse side)

No of data transfers = INT [IOCS capacity/1K] + 1

- Sub-IOCS can be divided into eight blocks. If divided to less than eight blocks, the block following to the final block mut be traced by "FFH".

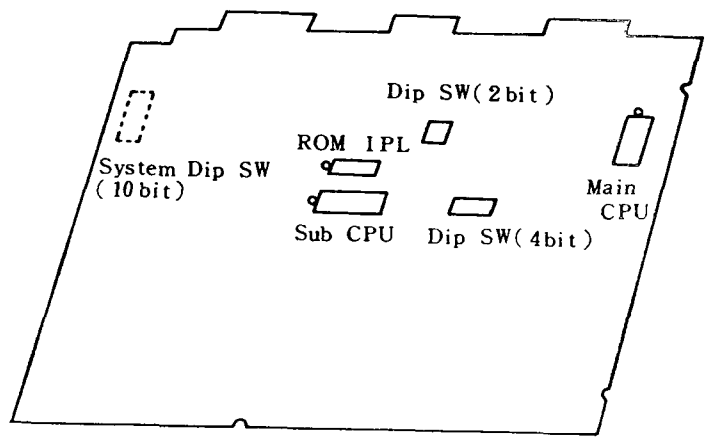
11-2. Sub-CPU side

[Test items]
Memory, VRAM, GDC peripheral, clock, speaker, printer interface, light pen, and RS232C interface.
GO/NO GO of the test must be confirmed on the video screen. Moving from test to test is done by depressing the HALT key.

[Procedure]
(1) Turn OFF all dip switch of the 4 bits unit located in the middle of the front side of the board and turn OFF all dip switches of the 2 bits unit.
(2) Set the system dip switch levers (10 bits) located on the reverse side of the board to the following positions.

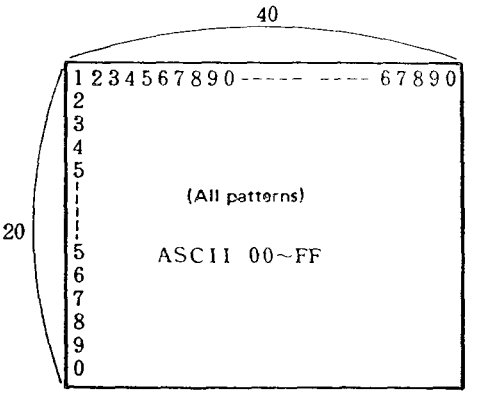
No.	1	2	3	4	5	6	7	8	9	10
POSITION	OFF	ON	ON	ON	ON	OFF	OFF	ON	ON	ON

(3) Turn power on while pushing the HALT siwtch to start the test program. Then, push the HALT switch to step to each test phase.
Result of GO/NO GO will appears on the video screen, except for the CRT interface and speaker tests.

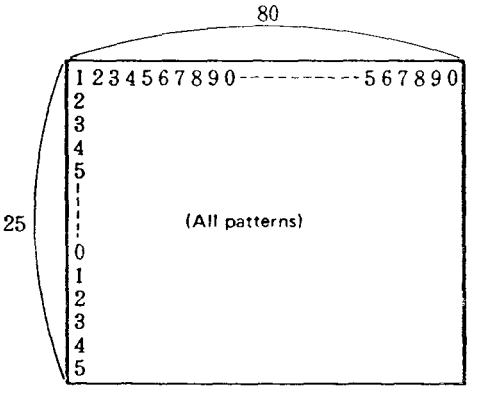


1) Memory test
Sub-IOCS RAM (4000H-5FFF)
Shared RAM (2003H-23FFH)
Shared RAM (2440H-27FFH)
Above are tested.
[Display]
(1) Normal test ending
RA OK: SUB-IOCS RAM
RA OK
RA OK Shared RAM
Above information are displayed on three display lines.
(2) Abnormal test ending
RA ER

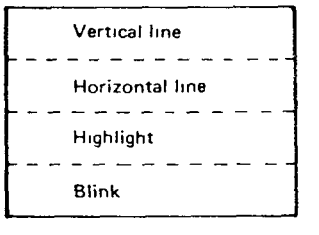
3) CRT inter face test
Performance of the CRT is tested. To move into each test phase, push the HALT switch. Test No.1-No.8 test the 400-raster CRT, and test No.9-No.16 test the 200 rasters CRT.
[Procedure and display]
(Test No.1)
Confirm all patterns on the display screen of 40 digits and 20 lines.



(Test No.2)
Confirm all patterns on the display screen of 80 digits and 25 lines.

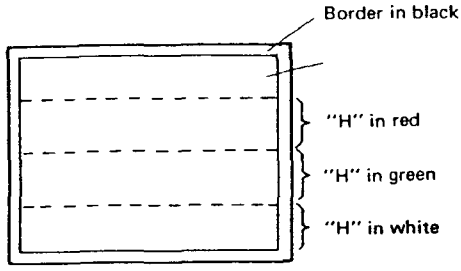


(Test No.3)
(1) Confirm that an entire screen is Filled with "H".
(2) Confirm that attributes are shown as illustrated.

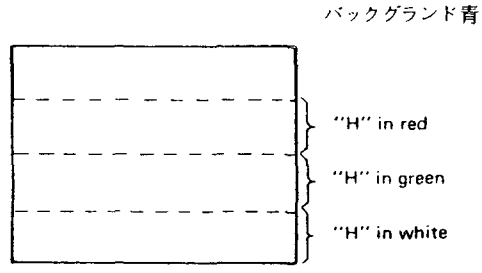


2) VRAM check
Proceed to test for ASCII and atribute VRAM
[Display]
During test periode, display shows under following.
(1) Display reviced "U" for entire screen from top side.
(2) Display blinking "I" with underline for entire screen.
(3) Display entire screen by space.
Test end
1. Normal
VR OK
2. Abnormal
VR ER

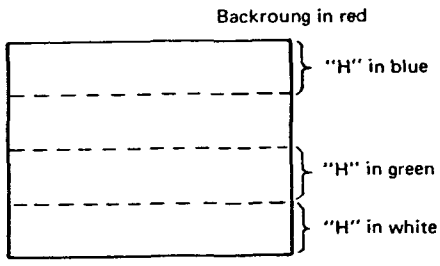
(Check No. 4)



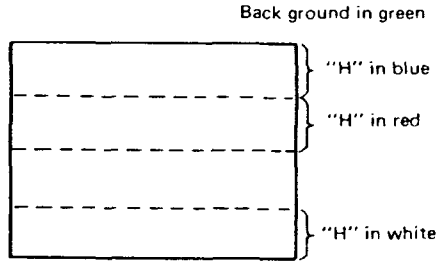
(Check No. 5)



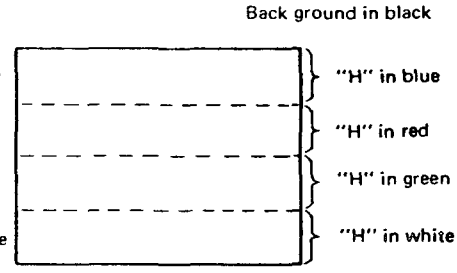
(Check No. 6)



(Check No. 7)



(Check No. 8)



4) Speaker test

Performance of the speaker and the volume control are tested. Listen carefully to detect any abnormal sound or mulfunction. Adjust the volume control to a suitable listening level.

5) Printer interface test

Performance of the printer interface signal lines and action of the 8255 are tested.

[Dispaly]

(1) Normal test ending
PR OK

(2) Abnormal test ending
PR ER

6) Light pen interface test

Performance of light pen interface signal lines and the action of the GDC are tested.

[Display]

On the upper left corner of the screen is displayed character and line.

(1) Normal test ending
LP OK

(2) Abnormal test ending
LP ER

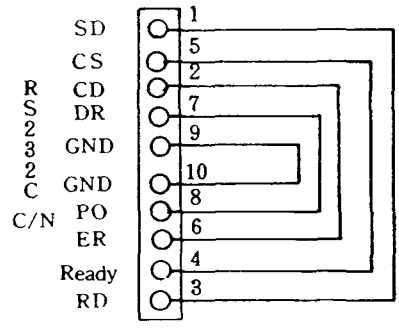
7) RS232C interface test

Performance of RS232C interface signal lines and the action of the 8251 are tested.

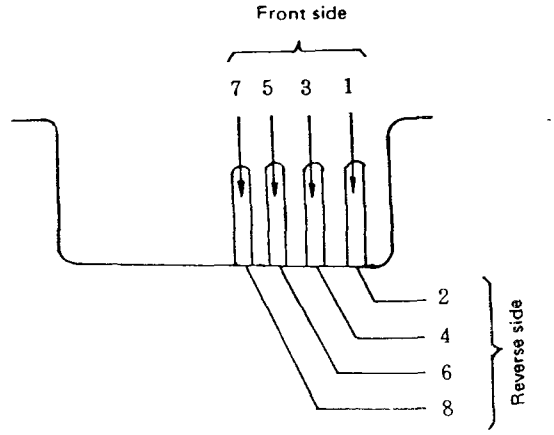
[Display]

(1) Normal test ending
RS OK

(2) Abnormal test ending
RS ER

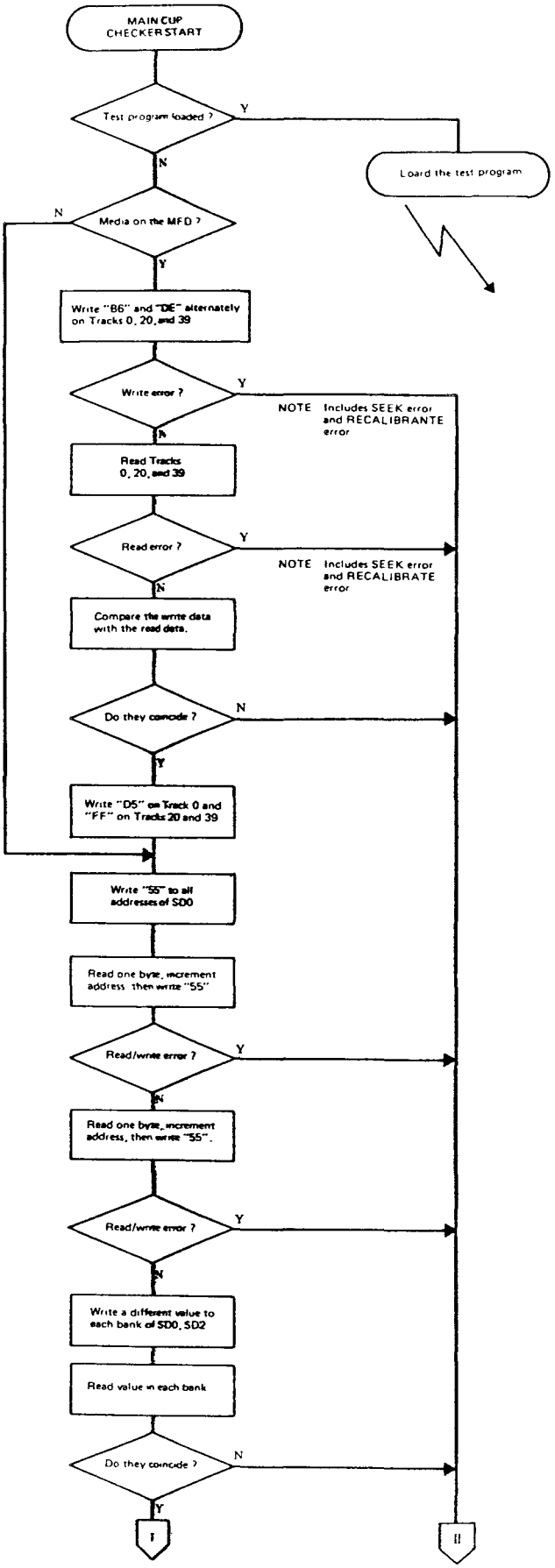


It will need wiring connection as illustrated in the figure in order to test the RS232C interface. Pins of the RS232C interface edge connector must be wired in the following manner:

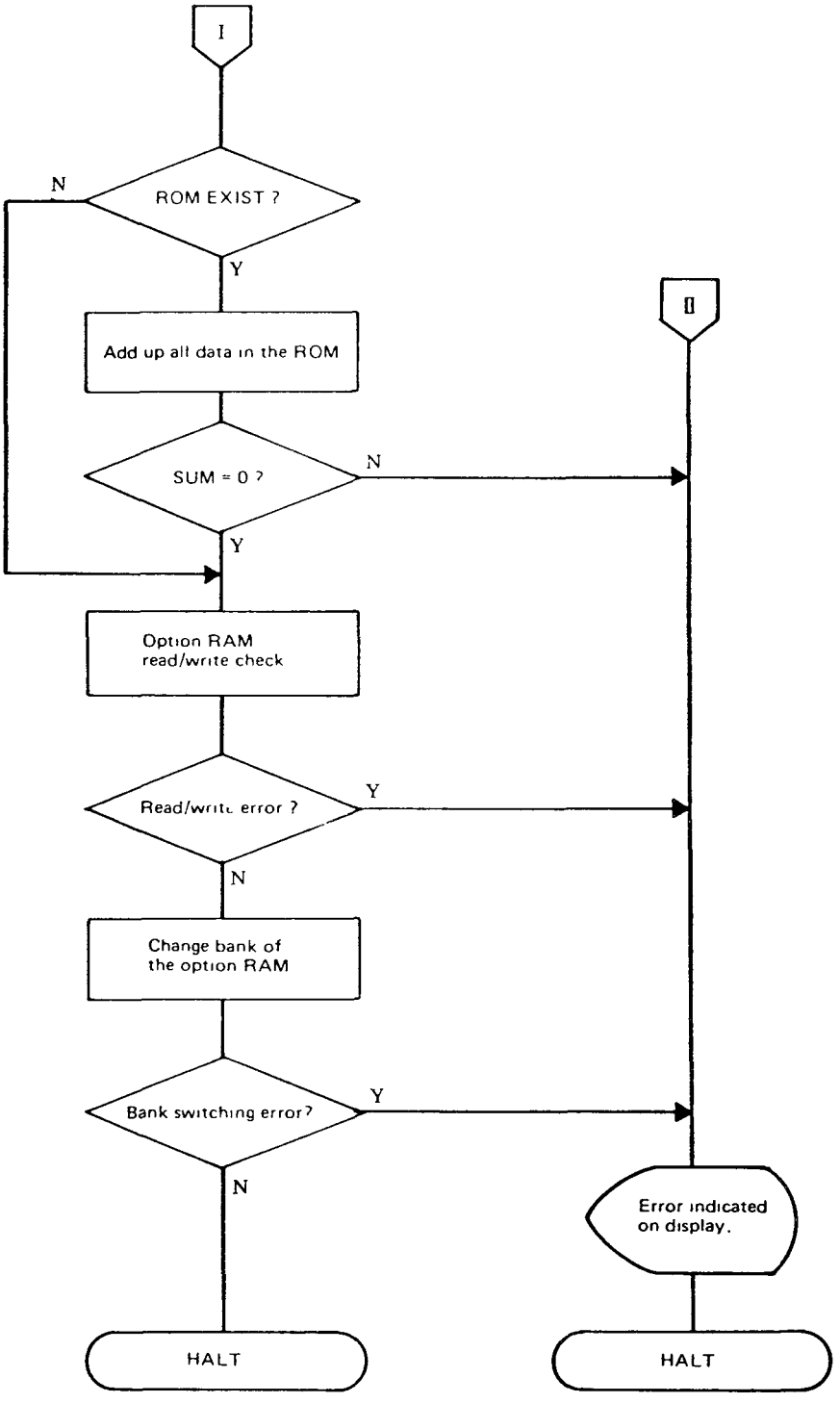


8) ROM-IPL

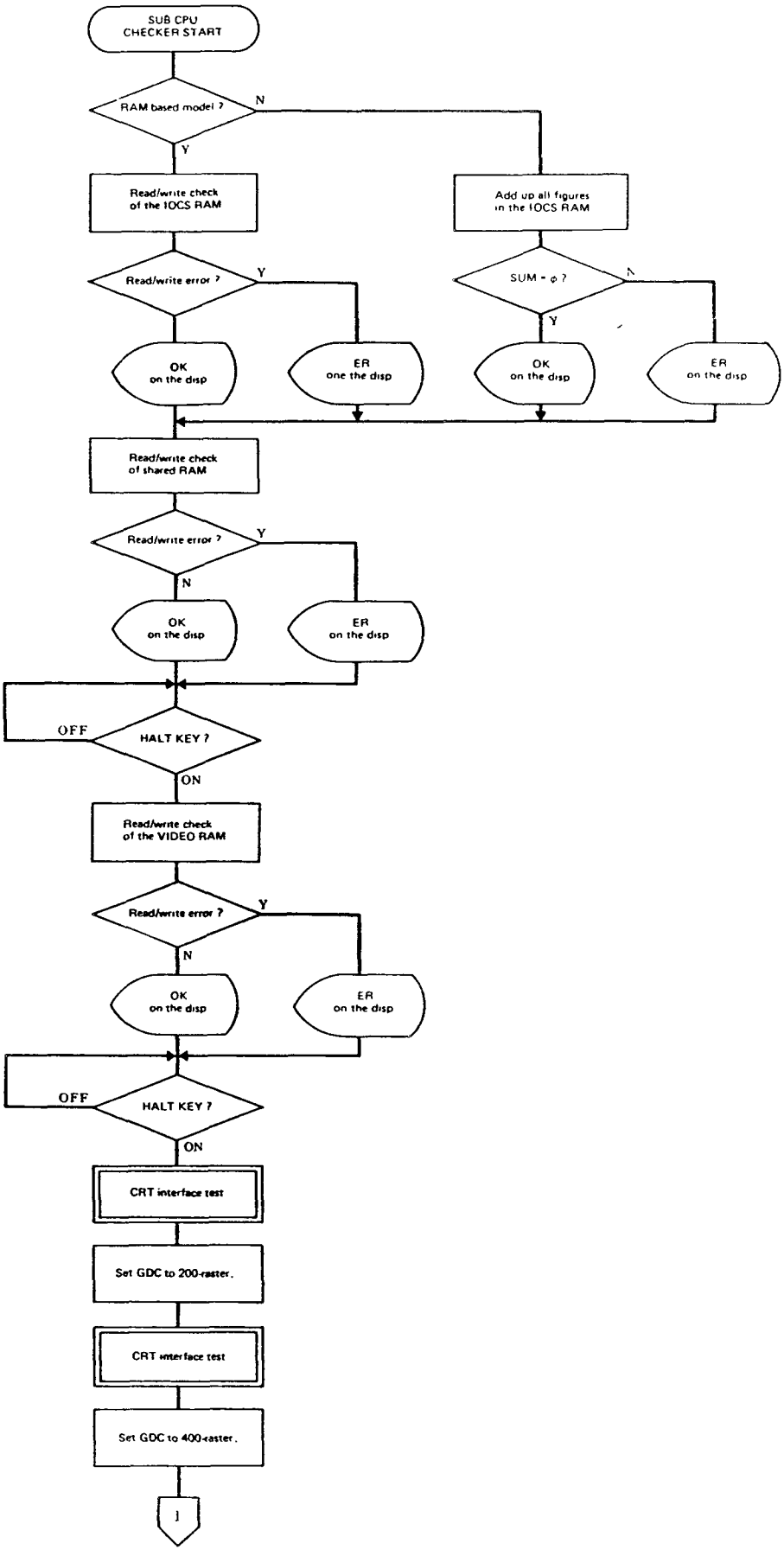
MAIN CPU CHECKER FLOW CHART 1/2



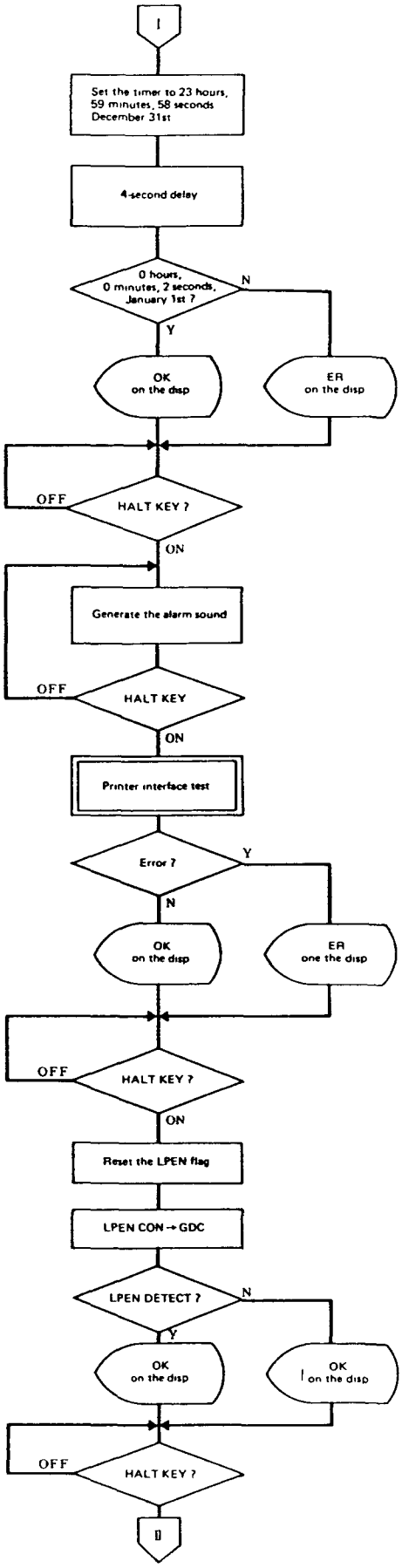
MAIN CPU CHECKER FLOW CHART 1/2



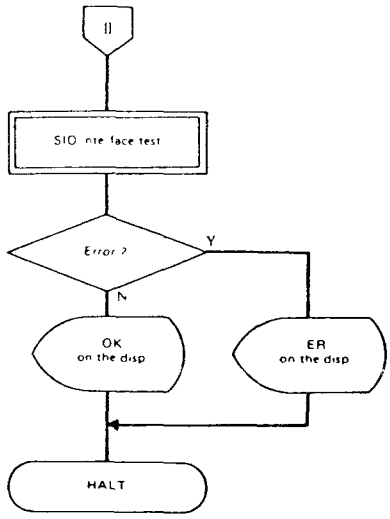
SUB CPU CHECKER FLOW CHART 1/3



SUB CPU CHECKER FLOW CHART 2/3



SUB CPU CHECKER FLOW CHART 3/3



11-3. Keyboard unit test functions

1) Keyboard controller ROM test

(1) After power on in a normal condition, it starts to carry out the ROM self-test.
If the alpha/symbol (LOCK) LED were to turn on, it indicates a failure in KBC. If not, KBC is satisfactory.
Key self check functional specification (simplified check)

2) Keyboard test

(1) As the power is turned on with the "DEB" in depression, it goes into the keyboard self-test mode.

(2) Depress key in a given sequence. If key is depressed in a correct sequence, it makes the alpha/symbol (LOCK) LED activated each time a key is pushed.
If the key was pushed in a wrong sequence or when a failure is met in the key, it makes the LED blinked.

(3) It returns to the normal mode upon completion of testing all keys. With this, the LED goes out.

(4) Observe the following key-in sequence to test.

i) Turn the OP/PRO siwtch to the OP side.

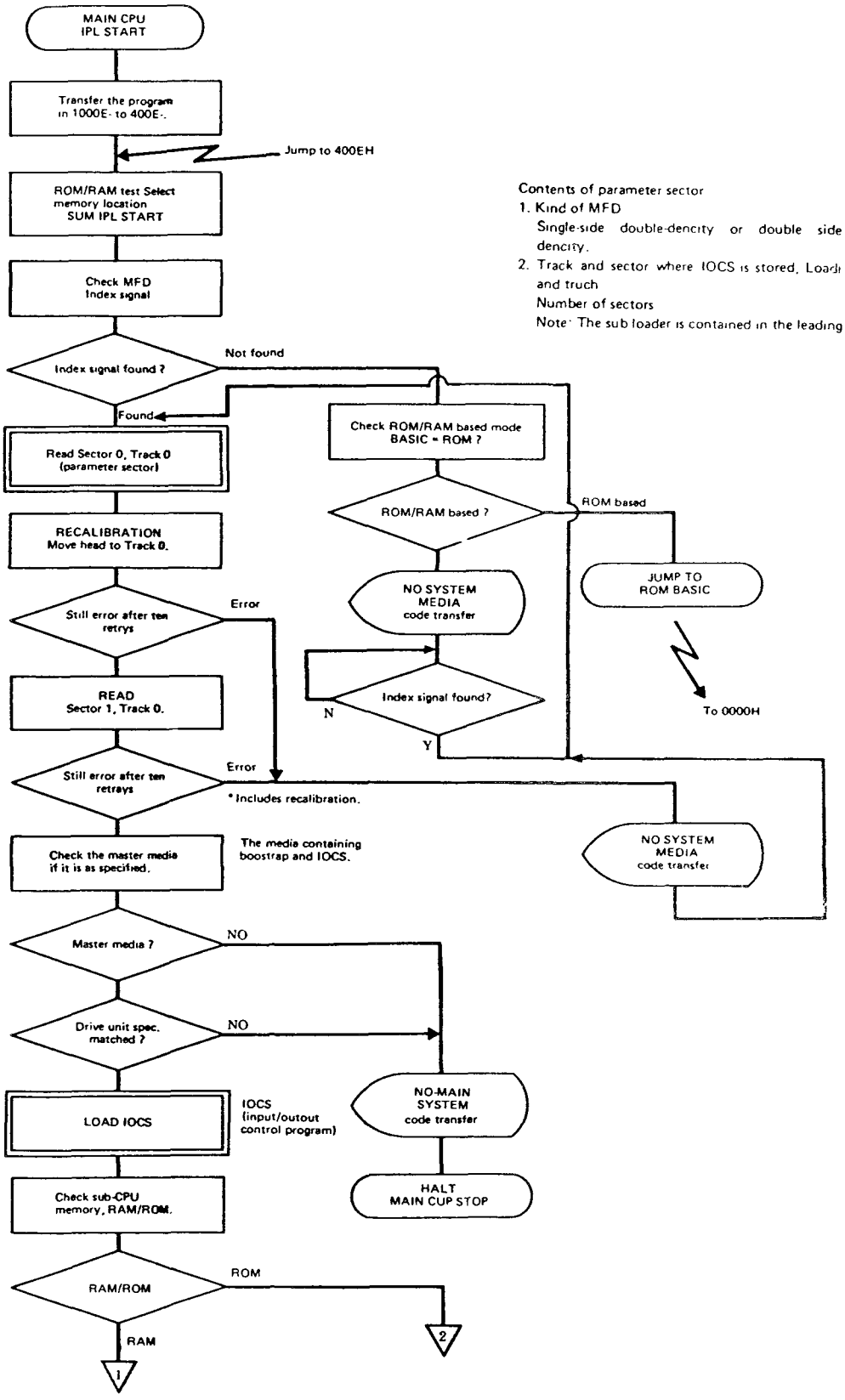
ii) Turn on power while pushing the "DEB" key.

iii) Turn the PO/PRO which to the PRO side.

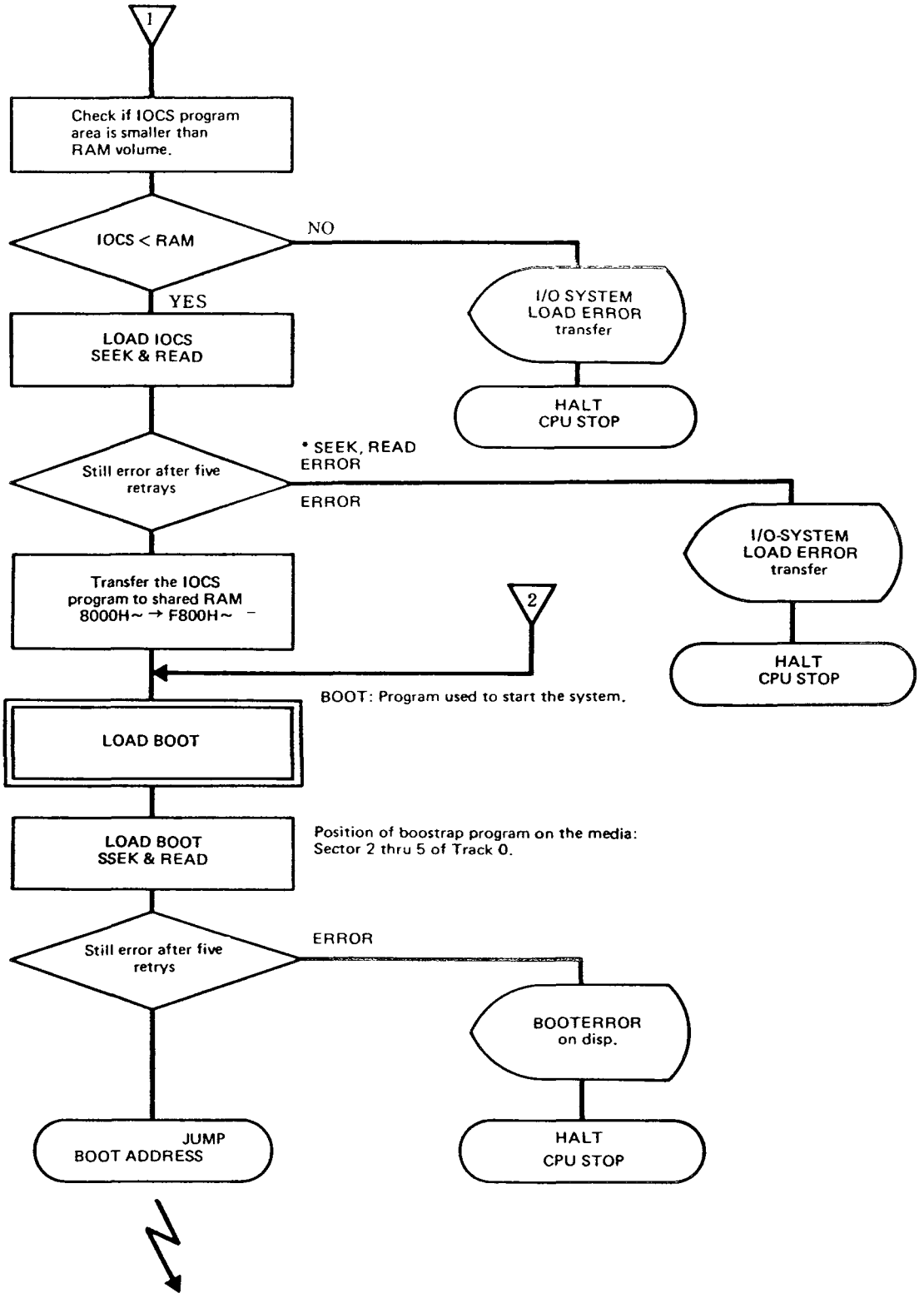
iv) Push a key one at a time in accordance with the given sequence.

12. IPL FLOW CHART

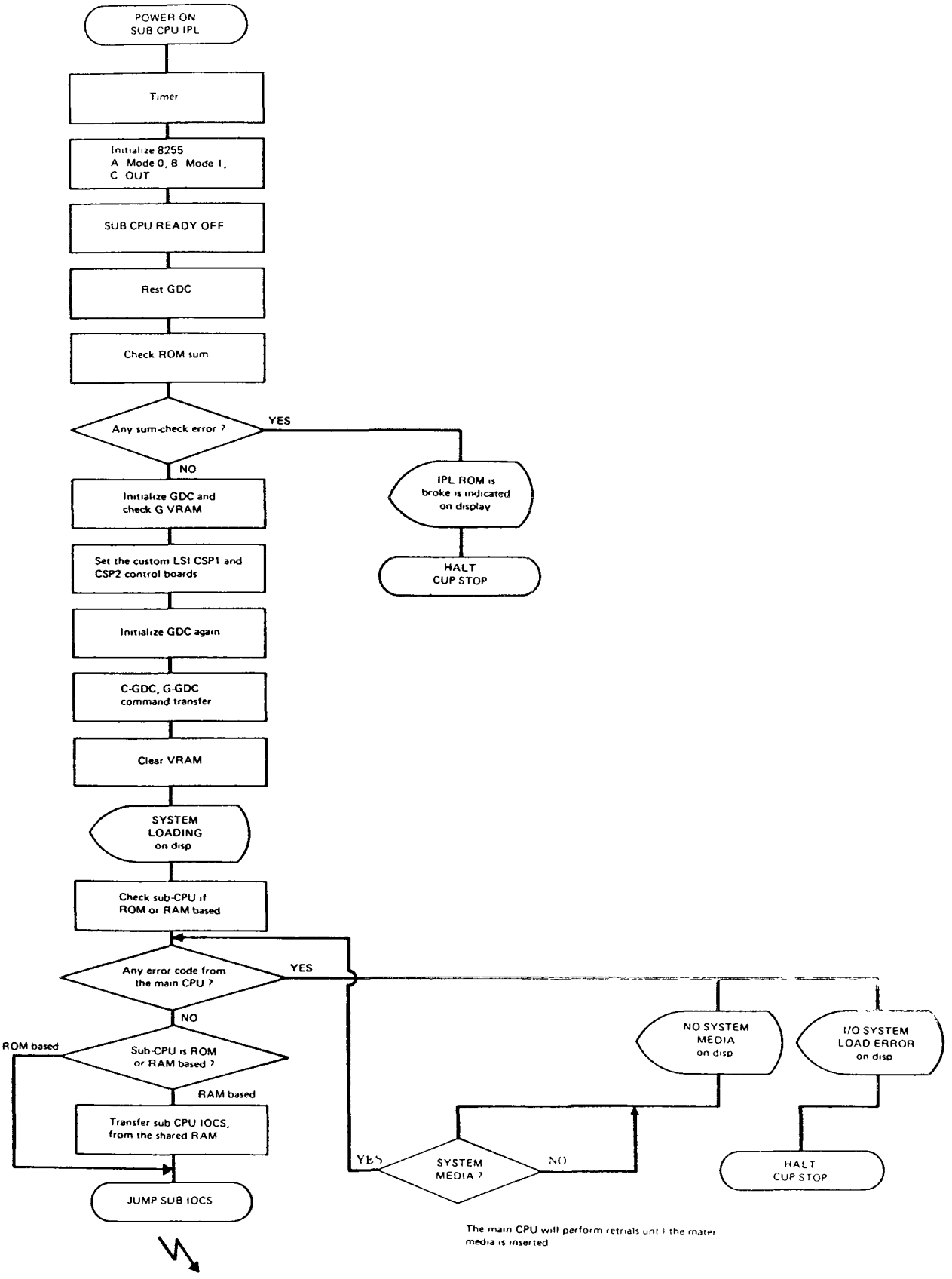
12-1. MAIN CPU IPL FLOW CHART 1/2



MAIN CPU IPL FLOW CHART 2/2

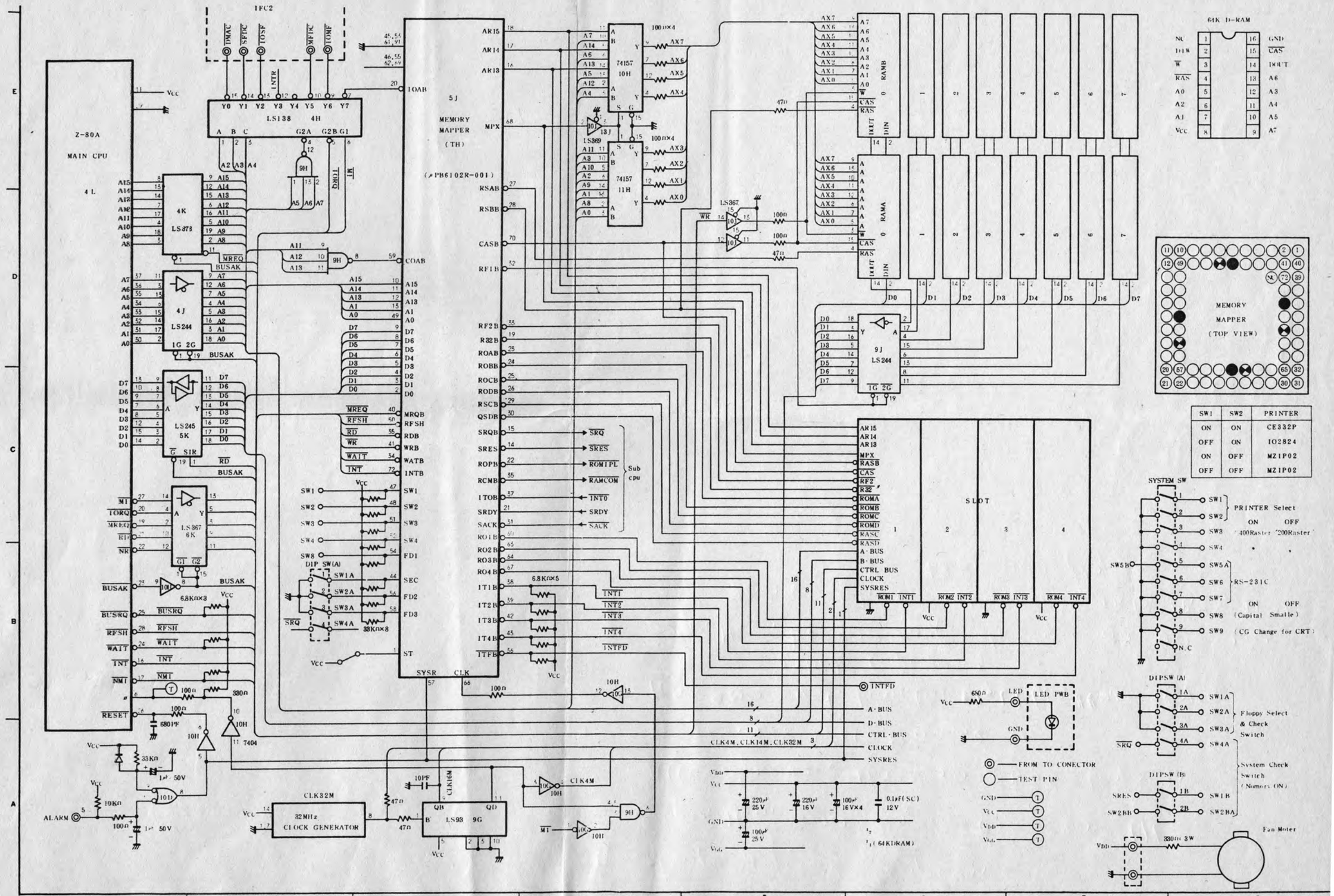


12 2. SUB CPU IPL FLOW CHART



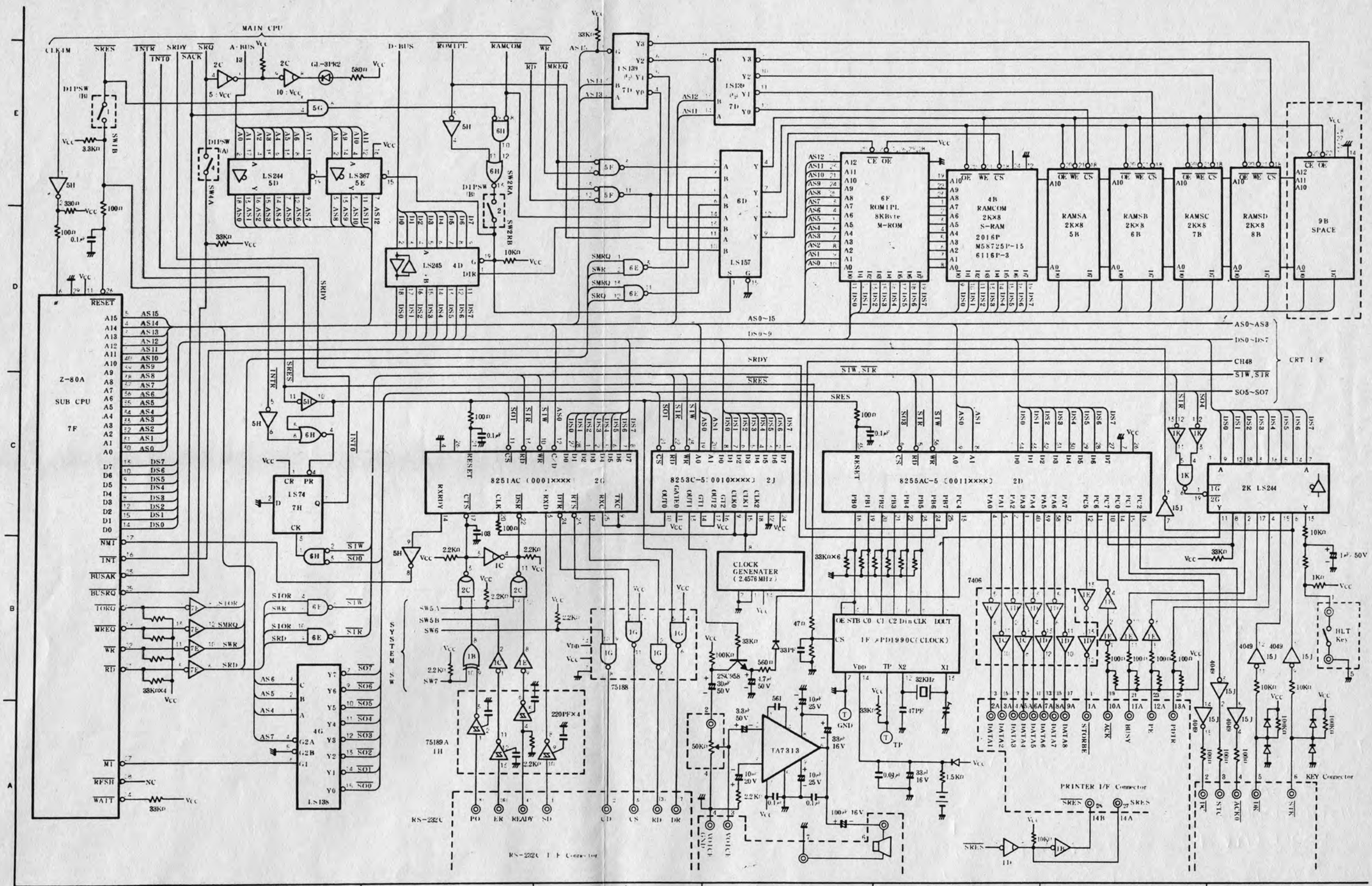
13. CIRCUIT DIAGRAM & P.W.B. LAYOUT

13-1. MAIN CPU & MEMORY CIRCUIT DIAGRAM

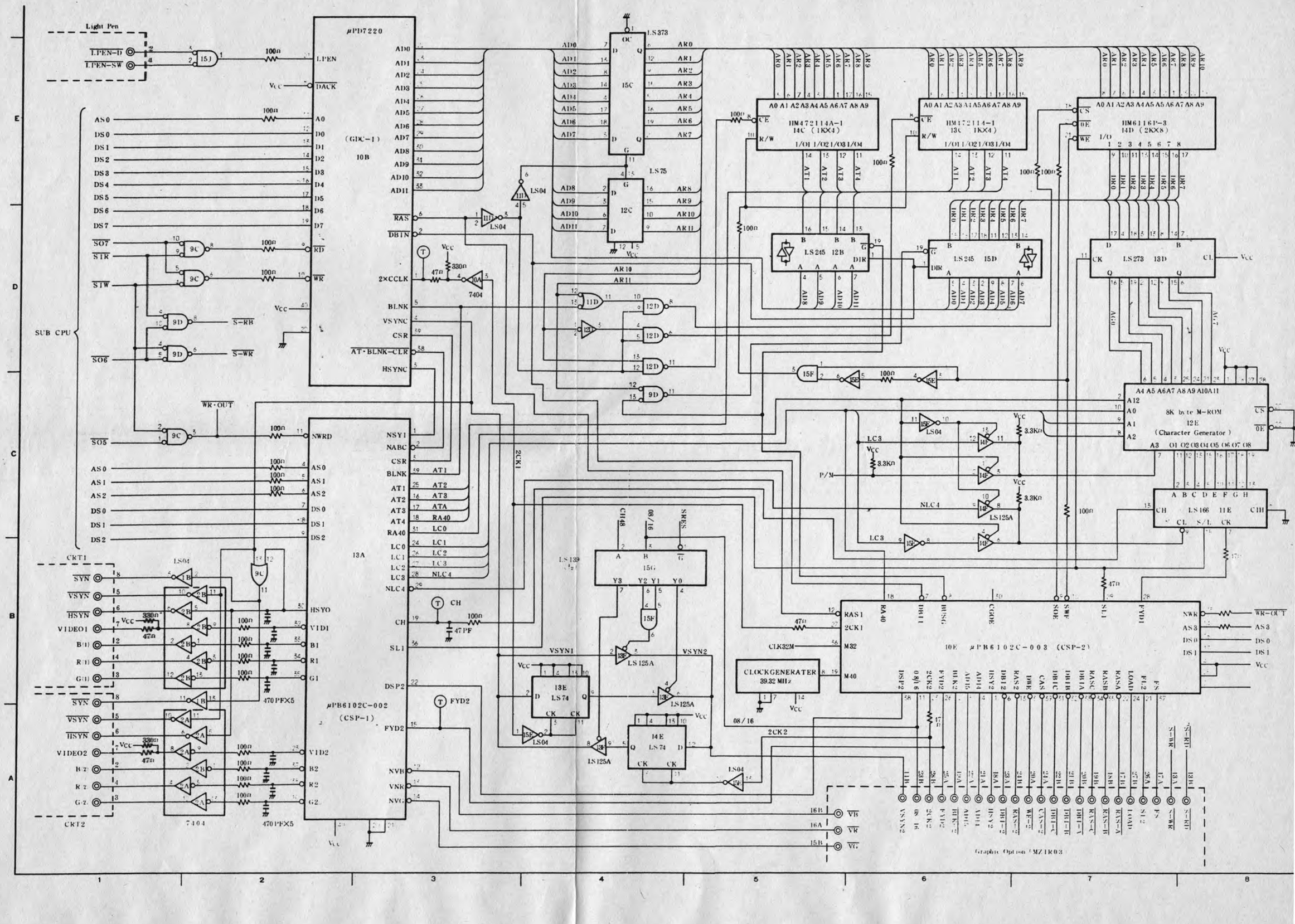


1

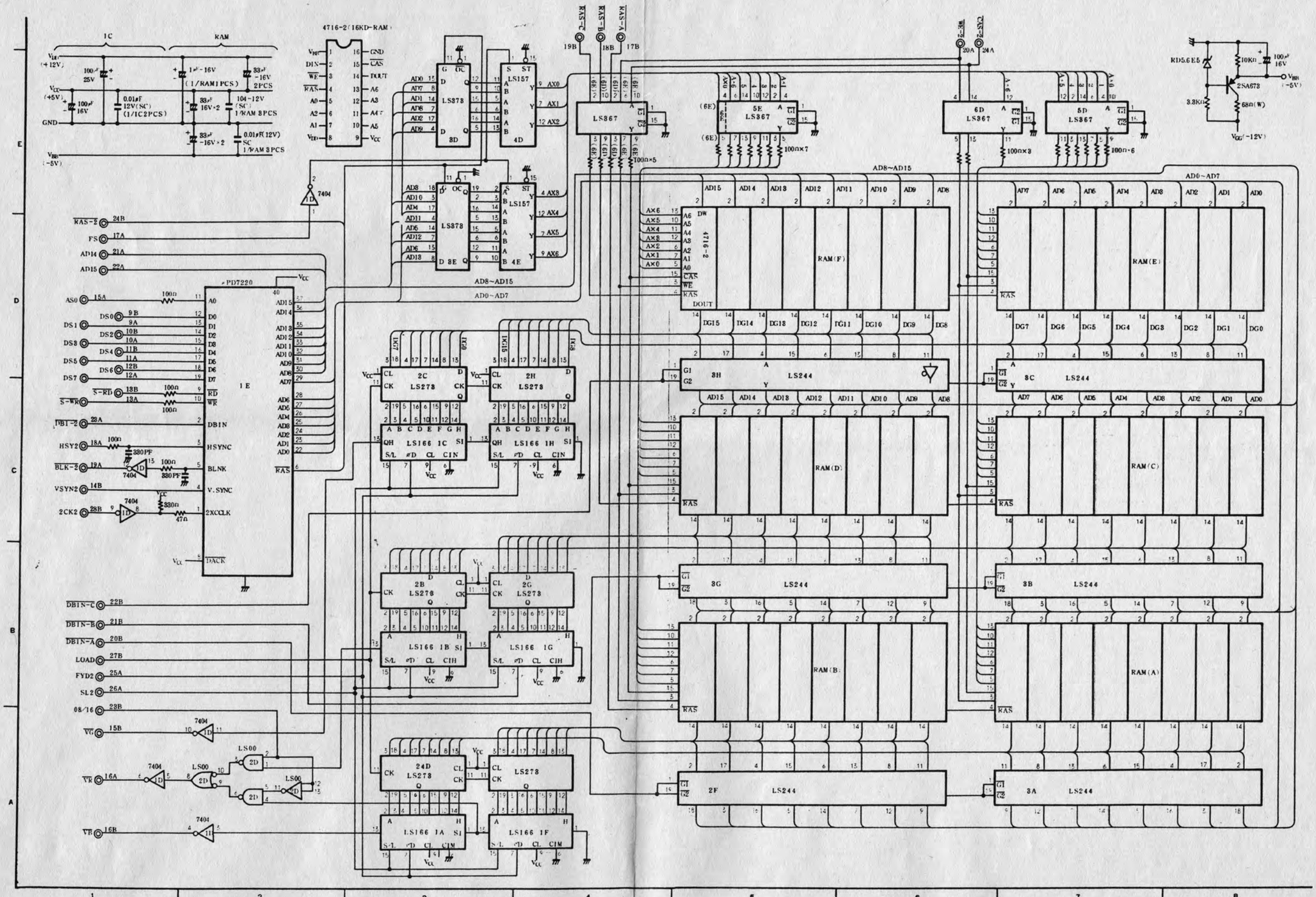
13-2. SUB CPU CIRCUIT DIAGRAM



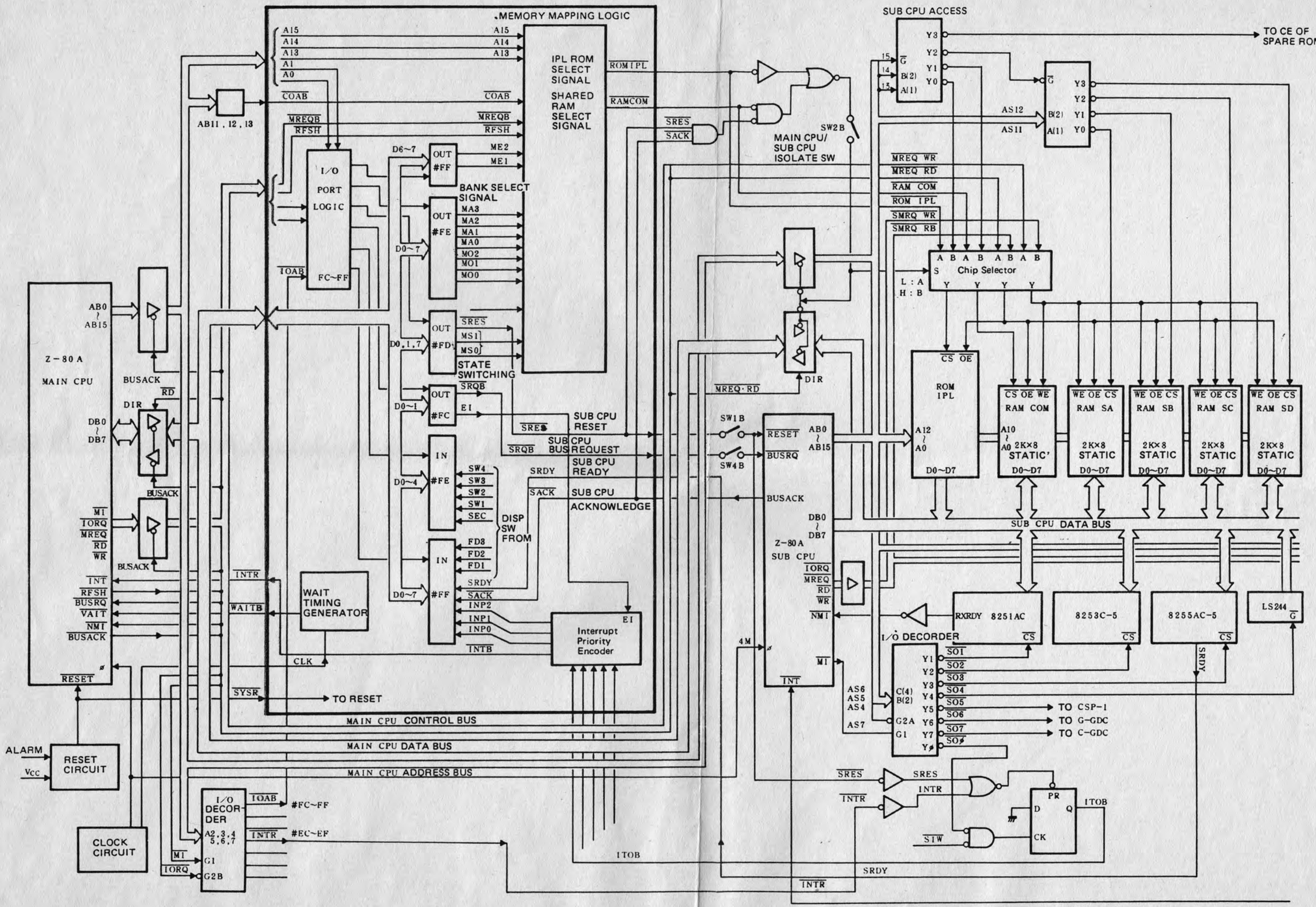
13-3. CRT INTERFACE CIRCUIT DIAGRAM



13-9. MZ-1R03 (GRAPHIC BOARD) CIRCUIT DIAGRAM

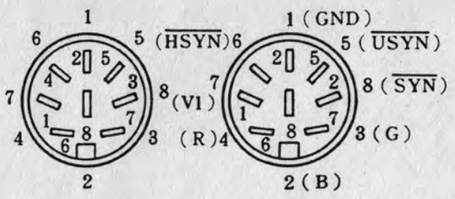


2) Memory relation between main CPU and sub-CPU.



13-15. CPU P.W.B. CONNECTOR TERMINAL TABLE

CONNECTOR



LED

1	GND
2	LED

CRT1

1	GND
2	B1
3	G1
4	R1
5	$\overline{VSYN}$
6	$\overline{HSYN}$
7	VIDEO1
8	$\overline{SYN}$

CRT2

1	GND
2	B2
3	G2
4	R2
5	$\overline{VSYN}$
6	$\overline{HSYN}$
7	VIDEO2
8	$\overline{SYN}$
9	

HALT·VOL-SP

1	GND
2	SP
3	GND
4	VOICE GND
5	VOICE
6	VOL
7	HLT

PS

2	V_{DD}	1	V_{GG}
4	V_{CC}	3	V_{CC}
6	GND	5	ALARM
8	GND	7	GND

IFC1

B		A
V_{DD}	1	V_{DD}
V_{DD}	2	V_{DD}
V_{GG}	3	V_{GG}
GND	4	GND
GND	5	GND
GND	6	GND
V_{CC}	7	V_{CC}
V_{CC}	8	V_{CC}
VOICE	9	VOICE GND
$\overline{INTFD}$	10	SYSRES
$\overline{RD}$	11	$\overline{WR}$
$\overline{IORQ}$	12	$\overline{MREQ}$
D0	13	D1
D2	14	D3
D4	15	D5
D6	16	D7
A0	17	A1
A2	18	A3
A4	19	A5
A6	20	A7
A8	21	A9
A10	22	A11
A12	23	A13
A14	24	A15

IFC2

B		A
GND	1	CLK16M
GND	2	CLK 4M
V_{CC}	3	V_{CC}
$\overline{SFDC}$	4	$\overline{DMAC}$
$\overline{IOSF}$	5	$\overline{MI}$
$\overline{MFDC}$	6	$\overline{IOMF}$
$\overline{WAIT}$	7	$\overline{BUSAK}$
$\overline{RFSH}$	8	$\overline{BUSRQ}$
$\overline{INT2}$	9	$\overline{INT1}$
$\overline{ROM4}$	10	$\overline{RF2}$
$\overline{CAS}$	11	$\overline{RASD}$
$\overline{ROM3}$	12	$\overline{RASC}$
$\overline{ROM2}$	13	$\overline{RASB}$
$\overline{ROMD}$	14	$\overline{ROM1}$
$\overline{ROMC}$	15	$\overline{INT3}$
$\overline{ROMB}$	16	MPX
$\overline{ROMA}$	17	$\overline{INT4}$
$\overline{R32}$	18	AR15
AR14	19	AR13
V_{CC}	20	V_{CC}
GND	21	GND
$\overline{SEL2}$	22	$\overline{INDEX}$
$\overline{MOTOR\ ON}$	23	$\overline{SEL3}$
$\overline{STEP}$	24	$\overline{DIRECTION}$
$\overline{WR\ GATE}$	25	$\overline{WR\ DATA}$
$\overline{TRACK\emptyset}$	26	$\overline{SIDE}$
$\overline{RD\ DATA}$	27	$\overline{WR\ PR}$
GND	28	$\overline{NMI}$
GND	29	GND
V_{CC}	30	V_{CC}

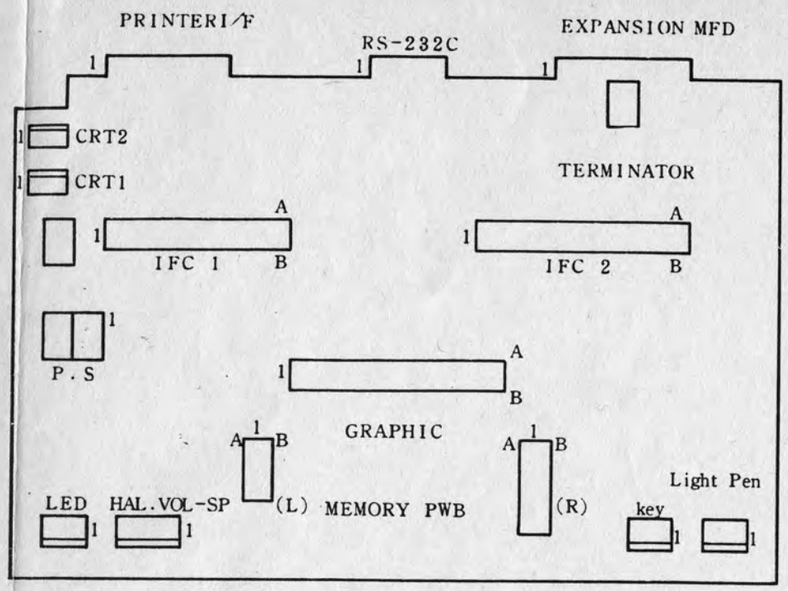
PRNTER I/F

A PARTS SIDE			B
1	$\overline{STROBE}$	2	
3	DATA1	4	
5	DATA2	6	
7	DATA3	8	
9	DATA4	10	
11	DATA5	12	
13	DATA6	14	GND
15	DATA7	16	
17	DATA8	18	
19	$\overline{ACK}$	20	
21	BUSY	22	
23	PE	24	
25	PDTR	26	
27	SRES	28	$\overline{SRES}$

RS-232C I/F

PARTS SIDE

1	SD	2	CD
3	RD	4	READY
5	CS	6	ER
7	DR	8	PO
9	GND	10	GND



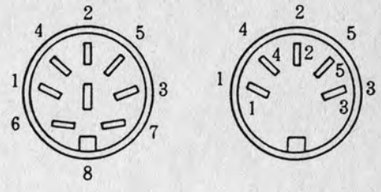
EXPANSION MFD I/F

A PARTS SIDE			B
1		2	
3	GND	4	
5		6	
7	$\overline{INDEX}$	8	
9	$\overline{SEL2}$	10	
11	$\overline{SEL3}$	12	
13		14	
15	$\overline{MOTOR\ ON}$	16	
17	$\overline{DIRECTION}$	18	TWIST PAIR
19	$\overline{STEP}$	20	
21	$\overline{WR\ DATA}$	22	GND
23	$\overline{WR\ GATE}$	24	
25	$\overline{TRACK\emptyset}$	26	
27	$\overline{WR\ PR}$	28	
29	$\overline{RD\ DATA}$	30	
31	$\overline{SIDE}$	32	
33	GND	34	

GRAPHIC

B		A
V_{DD}	1	V_{DD}
V_{DD}	2	V_{DD}
V_{DD}	3	V_{DD}
V_{GG}	4	V_{GG}
GND	5	GND
GND	6	GND
GND	7	GND
V_{CC}	8	V_{CC}
DS0	9	DS1
DS2	10	DS3
DS4	11	DS5
DS6	12	DS7
$\overline{S\text{-}RD}$	13	$\overline{S\text{-}WR}$
VSYN2	14	
$\overline{VG}$	15	AS0
$\overline{VB}$	16	$\overline{VR}$
$\overline{RAS\text{-}A}$	17	FS
$\overline{RAS\text{-}B}$	18	HSY2
$\overline{RAS\text{-}C}$	19	$\overline{BLK\text{-}2}$
$\overline{DBIN\text{-}A}$	20	$\overline{WE\text{-}2}$
$\overline{DBIN\text{-}B}$	21	AD14
$\overline{DBIN\text{-}C}$	22	AD15
08/16	23	$\overline{DBI\text{-}2}$
$\overline{RAS\text{-}2}$	24	$\overline{CAS\text{-}2}$
GND	25	FYD2
GND	26	SL2
LOAD	27	V_{CC}
2CK2	28	V_{CC}
GND	29	GND
V_{CC}	30	V_{CC}

CONNECTOR



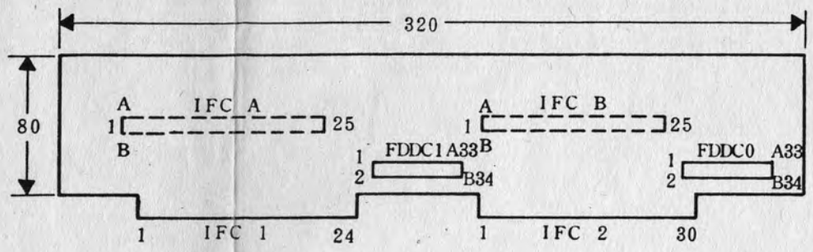
Key

1	V_{CC}
2	$\overline{DC}$
3	$\overline{STC}$
4	$\overline{ACKC}$
5	$\overline{DK}$
6	$\overline{STK}$
7	GND
8	GND

LIGHT PEN

1	V_{CC}
2	$\overline{LPEN\text{-}D}$
3	
4	$\overline{LPEN\text{-}SW}$
5	GND

13-16. MFD I/F P.W.B. CONNECTOR TERMINAL TABLE



FDDC0

B		A	
2		1	
4		3	
6		5	
8		7	$\overline{\text{INDEX}}$
10		9	$\overline{\text{SEL0}}$
12		11	$\overline{\text{SEL1}}$
14		13	
16	TWIST	15	$\overline{\text{MOTORON}}$
18	PAIR	17	$\overline{\text{DIRECTLON}}$
20	G	19	$\overline{\text{STEP}}$
22	N	21	$\overline{\text{WR DATA}}$
24	D	23	$\overline{\text{WR GATE}}$
26		25	$\overline{\text{TRACK0}}$
28		27	$\overline{\text{WR PR}}$
30		29	$\overline{\text{RD DATA}}$
32		31	$\overline{\text{SIDE}}$
34		33	

FDDC1

B		A	
2		1	
4		3	
6		5	
8		7	$\overline{\text{INDEX}}$
10		9	$\overline{\text{SEL0}}$
12		11	$\overline{\text{SEL1}}$
14		13	
16	TWIST	15	$\overline{\text{MOTORON}}$
18	PAIR	17	$\overline{\text{DIRECTLON}}$
20	G	19	$\overline{\text{STEP}}$
22	N	21	$\overline{\text{WR DATA}}$
24	D	23	$\overline{\text{WR GATE}}$
26		25	$\overline{\text{TRACK0}}$
28		27	$\overline{\text{WR PR}}$
30		29	$\overline{\text{RD DATA}}$
32		31	$\overline{\text{SIDE}}$
34		33	

IFCA

B		A
V_{DD}	1	V_{DD}
V_{DD}	2	V_{DD}
V_{GG}	3	V_{GG}
V_{GG}	4	GND
GND	5	GND
GND	6	GND
V_{CC}	7	V_{CC}
V_{CC}	8	V_{CC}
VOICE G	9	VOICE
SYSRES	10	$\overline{\text{INTFD}}$
$\overline{\text{WR}}$	11	$\overline{\text{RD}}$
$\overline{\text{MREQ}}$	12	$\overline{\text{IORQ}}$
D6	13	D7
D4	14	D5
D2	15	D3
D0	16	D1
A1	17	A0
A3	18	A2
A5	19	A4
A7	20	A6
A9	21	A8
A11	22	A10
A13	23	A12
A15	24	A14
GND	25	GND

IFCB

B		A
GND	1	CLK16M
GND	2	CLK 4M
V_{CC}	3	V_{CC}
$\overline{\text{SFDC}}$	4	$\overline{\text{MI}}$
$\overline{\text{IOSF}}$	5	BUSAK
$\overline{\text{WAIT}}$	6	$\overline{\text{BUSRQ}}$
$\overline{\text{RF SH}}$	7	GND
GND	8	$\overline{\text{INT3}}$
V_{CC}	9	$\overline{\text{RF2}}$
$\overline{\text{INT4}}$	10	$\overline{\text{CAS}}$
$\overline{\text{INT2}}$	11	MPX
$\overline{\text{INT1}}$	12	$\overline{\text{RASB}}$
$\overline{\text{RASD}}$	13	$\overline{\text{ROMD}}$
$\overline{\text{RASC}}$	14	$\overline{\text{ROMC}}$
$\overline{\text{ROM4}}$	15	$\overline{\text{ROMB}}$
$\overline{\text{ROM3}}$	16	GND
$\overline{\text{ROM2}}$	17	$\overline{\text{ROMA}}$
$\overline{\text{ROM1}}$	18	AR15
$\overline{\text{R32}}$	19	AR13
AR14	20	$\overline{\text{NMI}}$
GND	21	GND
GND	22	GND
GND	23	GND
V_{CC}	24	V_{CC}
V_{CC}	25	V_{CC}

IFC1

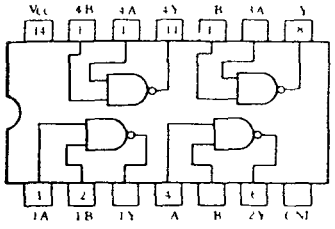
B	PARTS SIDE A	
V_{DD}	1	V_{DD}
V_{DD}	2	V_{DD}
V_{GG}	3	V_{GG}
GND	4	GND
GND	5	GND
GND	6	GND
V_{CC}	7	V_{CC}
V_{CC}	8	V_{CC}
VOICE	9	VOICE G
$\overline{\text{INTFD}}$	10	SYSRES
$\overline{\text{RD}}$	11	$\overline{\text{WR}}$
$\overline{\text{IORQ}}$	12	$\overline{\text{MREQ}}$
D0	13	D1
D2	14	D3
D4	15	D5
D6	16	D7
A0	17	A1
A2	18	A3
A4	19	A5
A6	20	A7
A8	21	A9
A10	22	A11
A12	23	A13
A14	24	A15

IFC2

B	PARTS S A	
GND	1	CLK16M
GND	2	CLK 4M
V_{CC}	3	V_{CC}
$\overline{\text{SFDC}}$	4	
$\overline{\text{IOSF}}$	5	$\overline{\text{MI}}$
MFDC	6	$\overline{\text{IOMF}}$
$\overline{\text{WAIT}}$	7	BUSAK
$\overline{\text{RFSH}}$	8	$\overline{\text{BUSRQ}}$
$\overline{\text{INT2}}$	9	$\overline{\text{INT1}}$
$\overline{\text{ROM4}}$	10	$\overline{\text{RF2}}$
$\overline{\text{CAS}}$	11	$\overline{\text{RASD}}$
$\overline{\text{ROM3}}$	12	$\overline{\text{RASC}}$
$\overline{\text{ROM2}}$	13	$\overline{\text{RASB}}$
$\overline{\text{ROMD}}$	14	$\overline{\text{ROM1}}$
$\overline{\text{ROMC}}$	15	$\overline{\text{INT3}}$
$\overline{\text{ROMB}}$	16	MPX
$\overline{\text{ROMA}}$	17	INT4
$\overline{\text{R32}}$	18	AR15
AR14	19	AR13
V_{CC}	20	V_{CC}
GND	21	GND
$\overline{\text{SEL2}}$	22	$\overline{\text{INDEX}}$
$\overline{\text{MOTORON}}$	23	$\overline{\text{SEL3}}$
$\overline{\text{STEP}}$	24	DIRECTLON
$\overline{\text{WR GATE}}$	25	$\overline{\text{WR DATA}}$
$\overline{\text{TRACK0}}$	26	$\overline{\text{SIDE}}$
$\overline{\text{RD DATA}}$	27	$\overline{\text{WR PR}}$
GND	28	$\overline{\text{NMI}}$
GND	29	GND
V_{CC}	30	V_{CC}

13-18. PIN CONFIGURATION OF IC & LSI

74 LS 00



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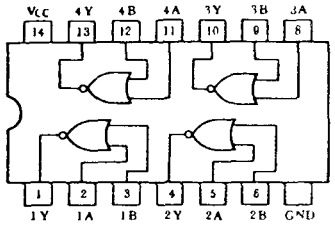

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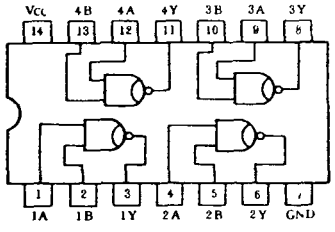

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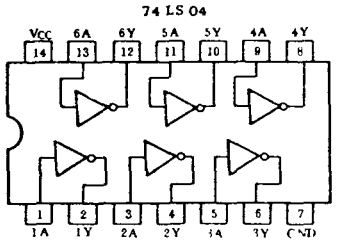

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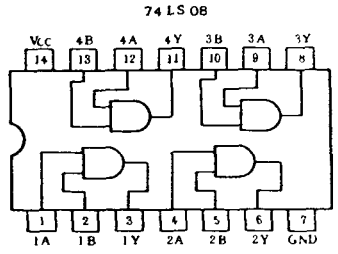

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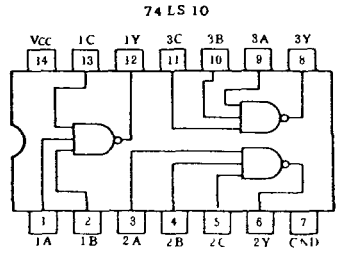

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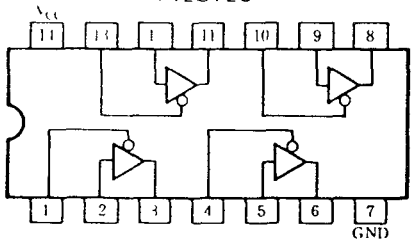

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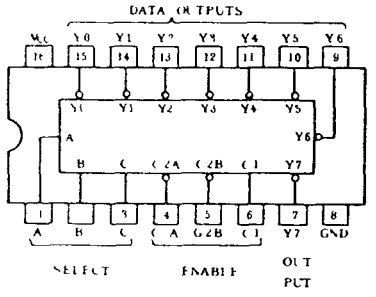

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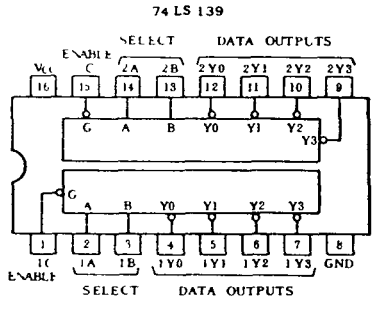

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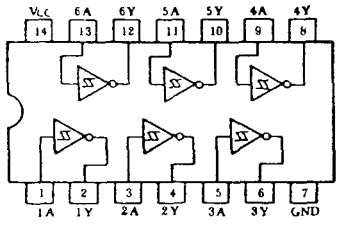

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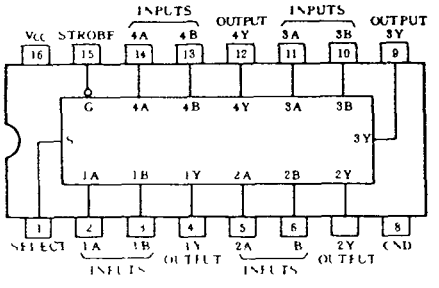

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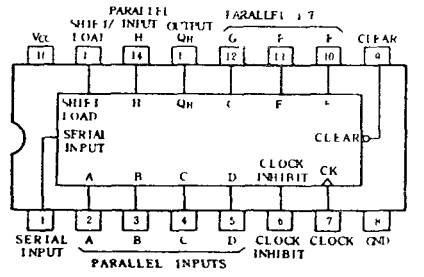

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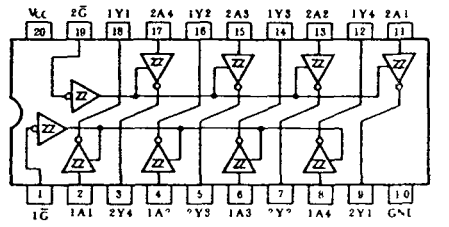

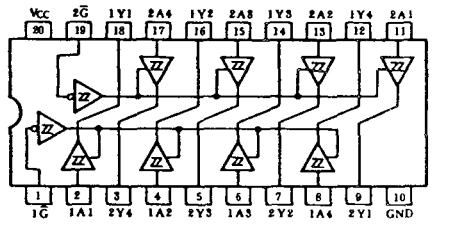

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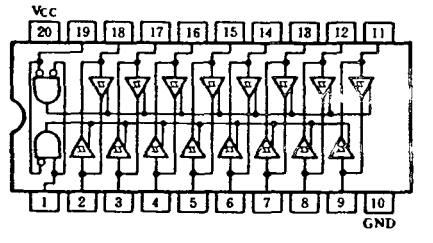

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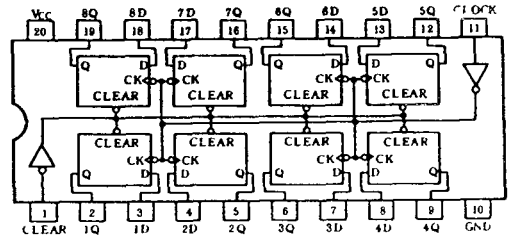

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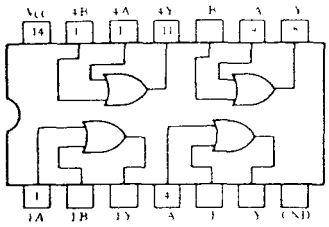

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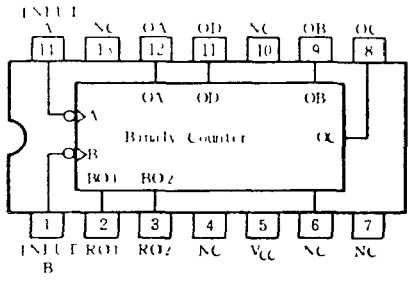

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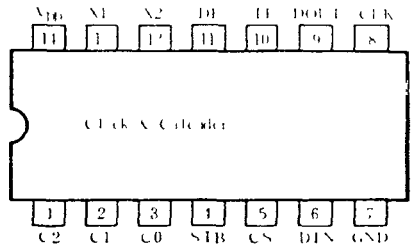

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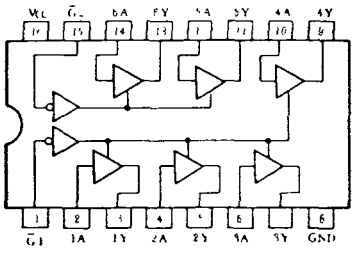

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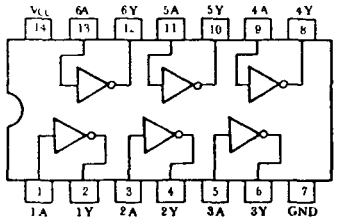

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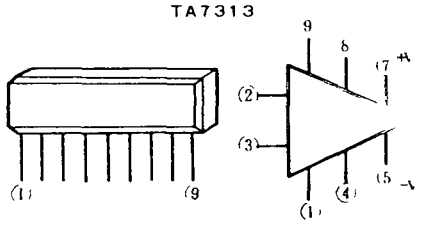

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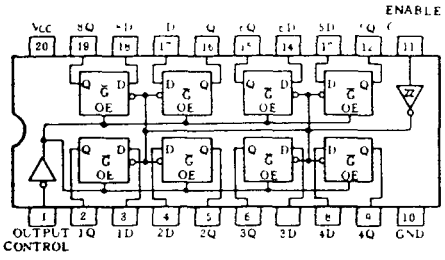

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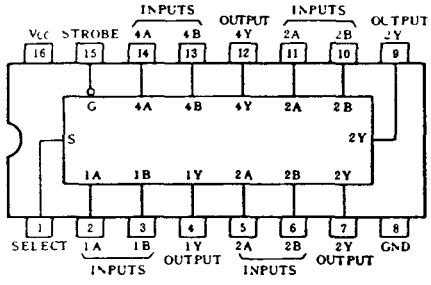

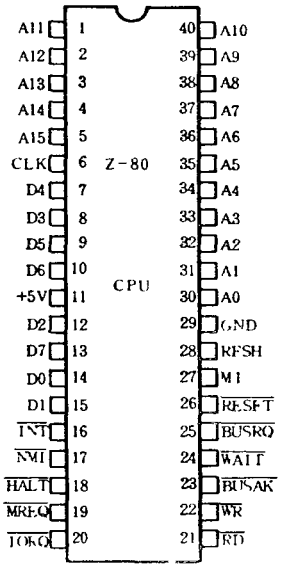

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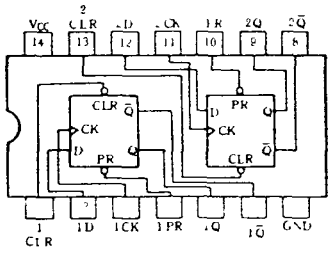

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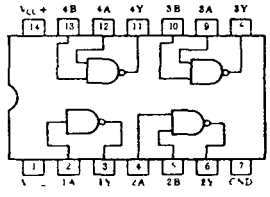

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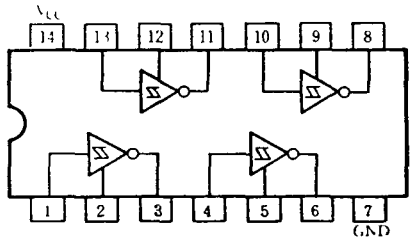

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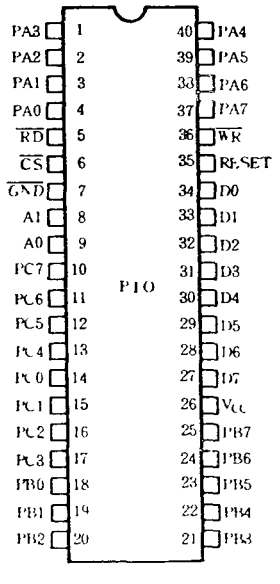

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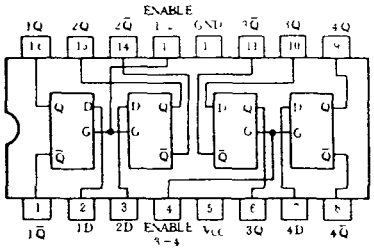

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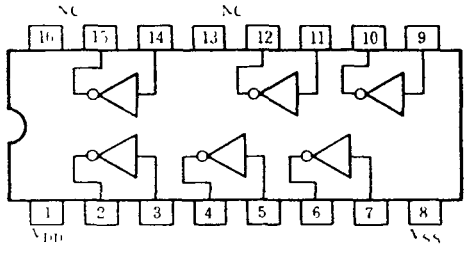

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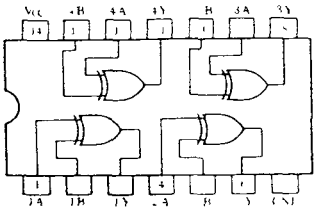

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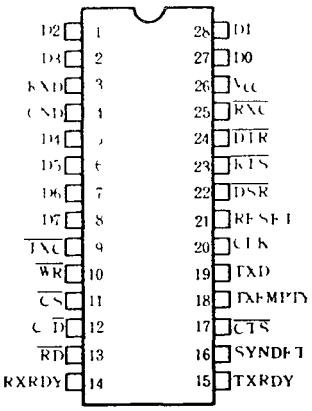

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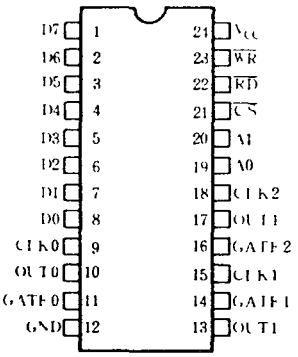
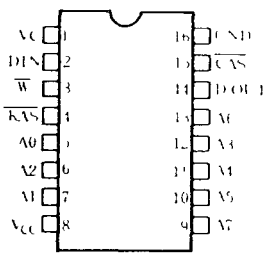


64K D-RAM



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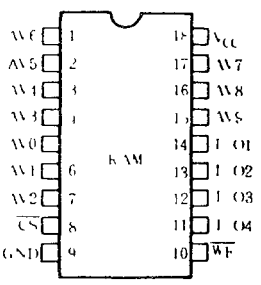

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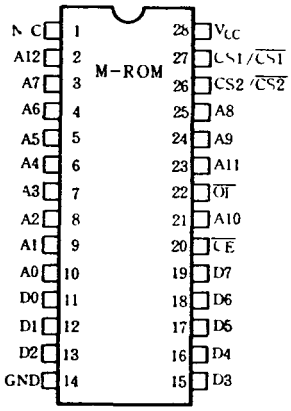

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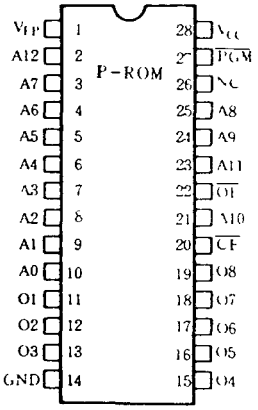

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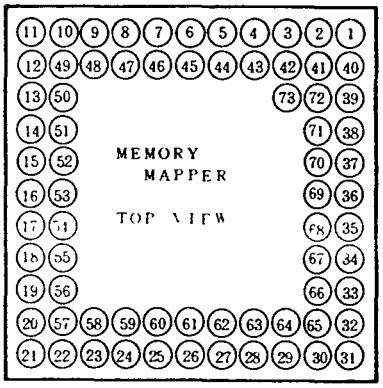

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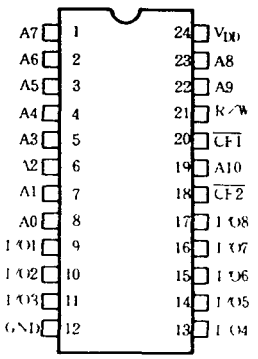
1	ST	11	A14	21	SRDY	31	SACK	41	WRB
2	D0	12	A13	22	RQ1B	32	RF1B	42	TT3B
3	D1	13	A 1	23	RQAB	33	RF2B	43	TT4B
4	D2	14	SRFS	24	RQBB	34	WATB	44	SFC
5	D3	15	SRQ	25	RQCB	35	RCMB	45	GND
6	D4	16	AR13	26	RQDB	36	TTFB	46	GND
7	D5	17	AR14	27	RSAB	37	TTOB	47	SW1
8	D6	18	AR15	28	RSBB	38	TT1B	48	SW2
9	D7	19	RST	-	CT	39	TT2L	49	A0
10	A15	20	TOA	30	RSDB	40	MRQB	50	RFSH

51	SW3	61	GND	71	GND
52	SW4	62	GND	72	TNTB
53	GND	63	RQ2B	73	NC
54	FD1	64	RQ3B		
55	GND	65	RDB		
56	FD2	66	CLK		
57	SYSR	67	RQ4B		
58	FD3	68	MPX		
59	C0AB	69	GND		
60	RQ1B	70	CASB		

2016P
M58725-15
6116P-3



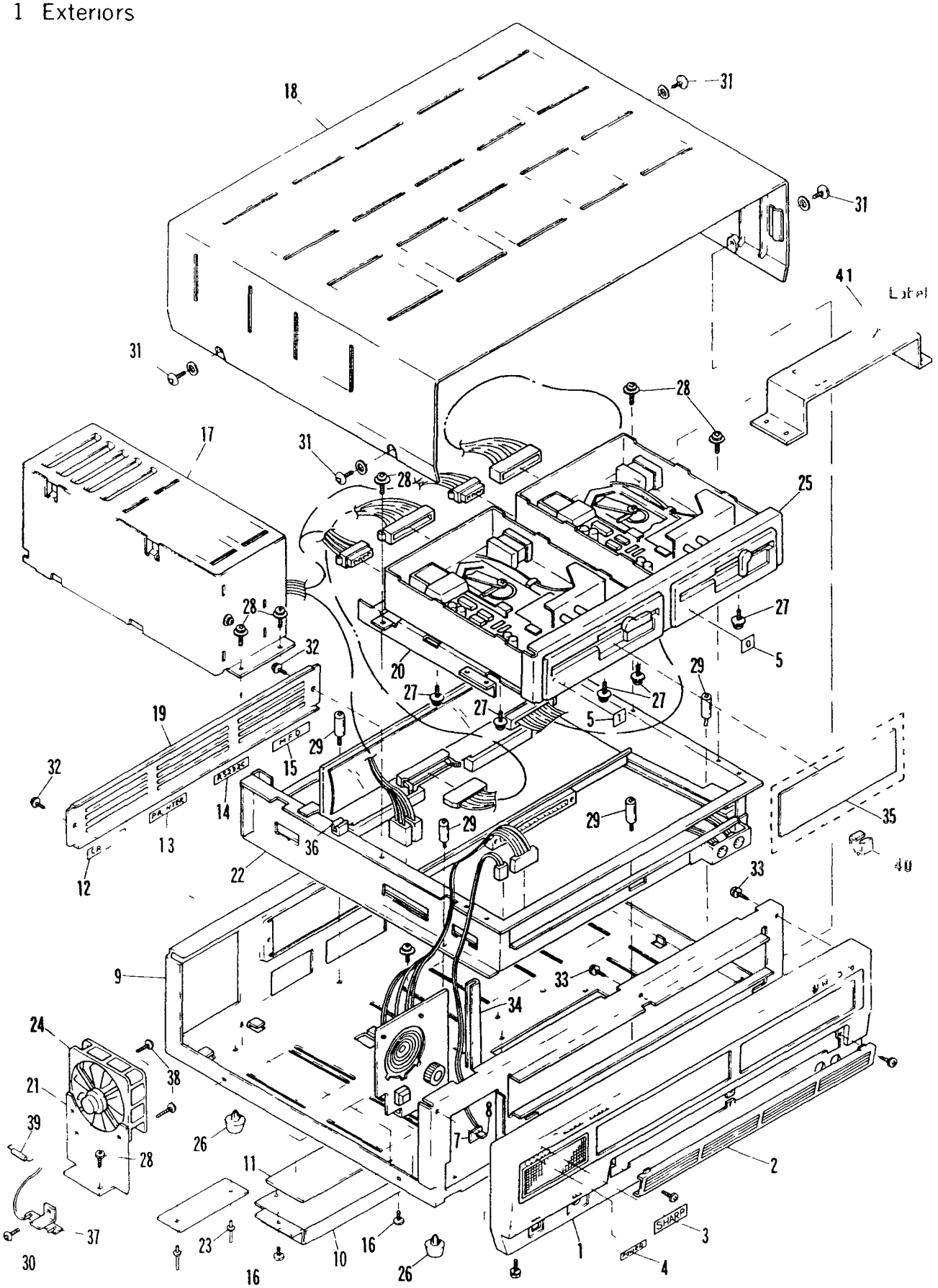
MZ-3500

PARTS GUIDE LIST

1 Exteriors

NO	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	CCABC1007ACZZ	AY		D	Front Cabinet assembly
2	GFTAF1001ACZZ	AE	N	D	Lid for Graphic slot
3	HBDGB3004GESA	AE		D	Badge "SHARP"
4	TLABZ1003ACZZ	AB	N	D	Label "POWER"
5	TLABZ1008ACZZ	AA	N	D	Drive No. label
6	QCNCW1008AC01	AC		C	Connector 2pin
7	QPWBF1005ACZZ	AA	N	C	LED PWB
8	VHPGL9PR2//-1	AC		B	Photo transistor
9	GCABA1003ACZZ	BM	N	D	Bottom cabinet
10	GFTAU1005ACZZ	AL	N	D	Lid for ROM LSI
11	PSPAG1004ACZZ	AC		C	Rubber spacer
12	TLABZ1017ACZZ	AC		C	Label for I/O port
16	XBPSF30P06K00	AA		C	Screw
17	DUNT-1018ACZZ	**	N	E	Power supply unit for 200V series
	DUNT-1035ACZZ	**		E	Power supply unit for 100V series
18	GCABB1004ACZZ	BG	N	D	Top cabinet
19	GCOVH1001ACZZ	AM	N	D	Slot cover
20	LANGT1003ACZZ	AX	N	C	Fixing angle for MFD
21	LANGT1010ACZZ	AE		C	Fixing angle for fan
22	LCHSM1008ACZZ	AY		C	Chassis
23	LX-LZ6023RCZZ	AA		C	Rivet
24	NFANP1001ACZZ	BM	N	B	Fan motor
25	RMEMR1002ACZZ	**	N	E	MFD unit
26	GLEGP0010UCZZ	AB		C	Rubber foot
27	XBPSD30P08KS0	AA		C	Screw
28	XBPSD40P06KS0	AA		C	Screw
29	LX-BZ1001ACZZ	AC		C	Screw
30	XBPSD40P06K00	AA		C	Screw
31	XBTSC40P06000	AA		C	Screw
32	XBTSF40P08000	AA		C	Screw
33	XCPSD40P12000	AA		C	Screw
34	PHOG-1001ACZZ	AC	N	C	Rubber cushion
35	GFTAF1002ACZZ	AE		D	Cover
36	LHLDW6655RCZZ	AB		C	Wire holder
37	QLUGL0006UCZZ	AB		C	Lug terminal
38	XBPSD30P30KS0	AA		C	Screw
39	VRS-PT3LB330J	AC		C	Resistor (3.0W 33Ω ±5%)
40	LHLDW6655RCZZ	AB		C	Cord holder
41	PSLDM1003ACZZ	AP		C	Shield for MFD
	TLABZ1400CCZZ	AA		C	Label

1 Exteriors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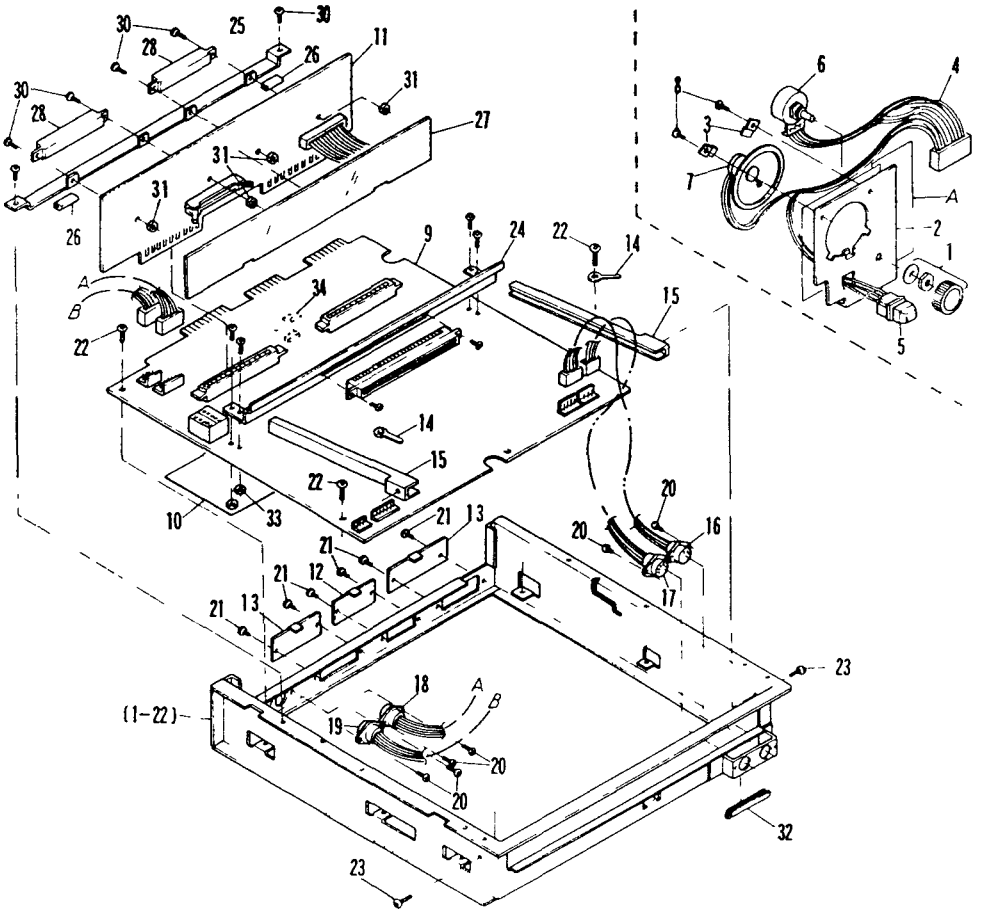
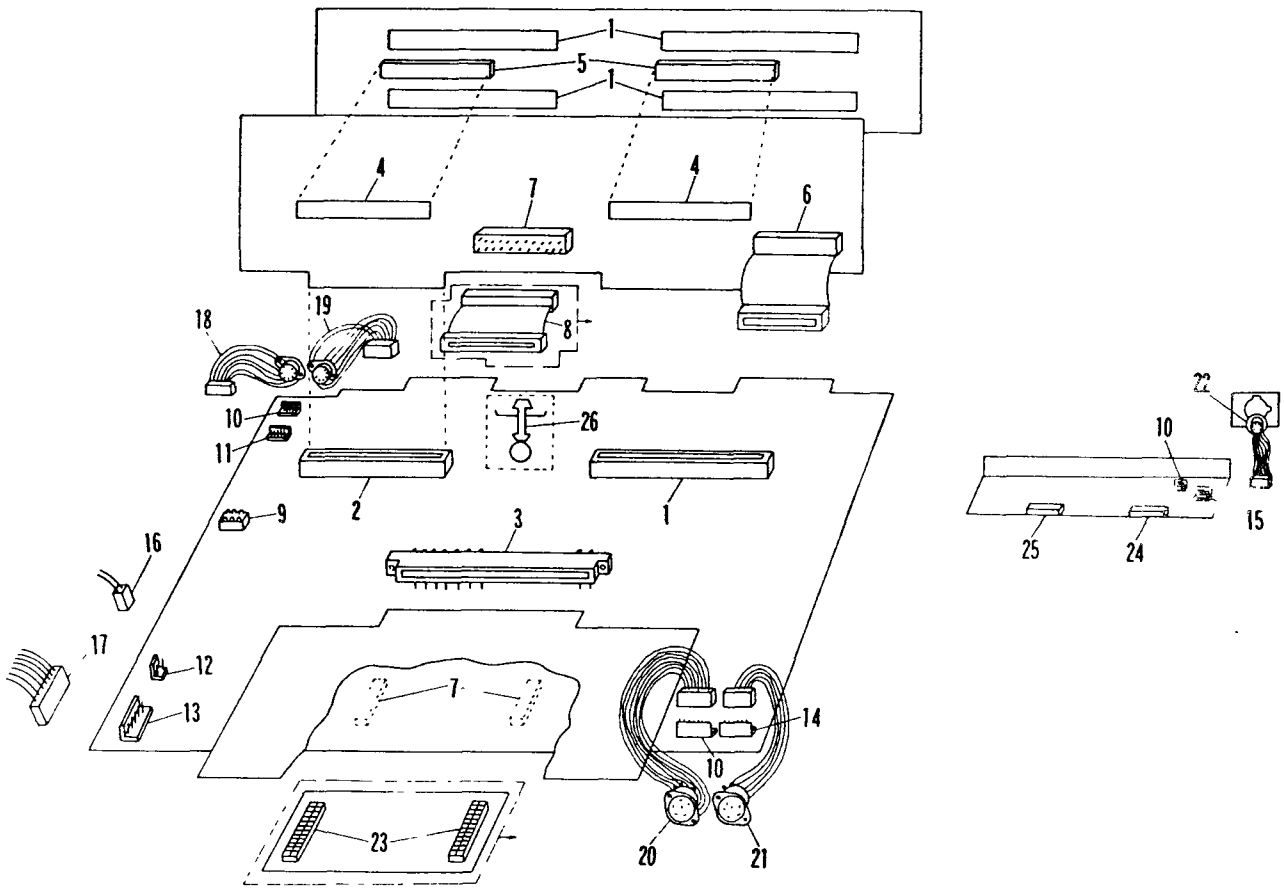
[2] PWB & Fixing angles

NO	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	JKNBM0004PAZZ	AC	N	C	Knob for VR
2	LANGS1006ACZZ	AF	N	C	Fixing angle for speaker
3	LANGK1007ACZZ	AB	N	C	Fixing angle for speaker
4	QCNCW1008AC02	AF		C	Connector
5	QSW-K1007ACZZ	AE	N	B	HALT switch
6	RVR-A5452QCZZ	AF		B	Variable resistor
7	VSP0080P-608N	AN		C	Speaker
8	XBPSD30P06K00	AA		C	Screw
9	DUNTK1082ACZZ	**		E	CPU PWB unit (Model 3541)
	DUNTK1083ACZZ	**		E	CPU PWB unit (Model 3530)
	DUNTK1064ACZZ	**		E	CPU PWB unit (Model 3540)
11	DUNTK1060ACZZ	**	N	E	MFD I/F PWB unit
12	GFTAR1003ACZZ	AD	N	D	Cover for RS232C I/O slot
13	GFTAR1004ACZZ	AC	N	D	Cover for I/O slot
15	LHLDZ1001ACZZ	AD	N	C	Guide for PWB
16	QCNW-1003ACZZ	AK	N	C	Connector for light pen
17	QCNW-1004ACZZ	AM	N	C	Connector for key board
18	QCNW-1047ACZZ	AM	N	C	Connector for CRT-1
19	QCNW-1044ACZZ	AM	N	C	Connector for CRT-2
20	XBBSC26P04000	AA		C	Screw
21	XBBSC30P06000	AA		C	Screw
22	XBPSD30P06KS0	AA		C	Screw
23	XUPSD26P06000	AA		C	Screw
24	LANGQ1004ACZZ	AH	N	C	Connector "A" angle
25	LANGQ1005ACZZ	AF	N	C	Connector "B" angle
26	PCUSG1001ACZZ	AA	N	C	Cushion for PWB
27	PZETY1001ACZZ	AE	N	C	Insulator for MFD
28	QCNCM1002ACZZ	AQ		C	Connector
29	QCNW-1007ACZZ	AX	N	C	Connector (18pin)
30	XBPSD30P10000	AA		C	Screw
	XBPSD40P08KS0	AA		C	Screw
31	XNESD30-24000	AA		C	Nut
32	PHOG-1002ACZZ	AC	N	C	Rubber cushion
33	XNESD30-24000	AA		C	Nut
34	LHLDF6648RCZZ	AB		C	Holder
35	PCUSG1001ACZZ	AA	N	C	Rubber cushion for PWB



3 Connector

NO	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	QCNCP6041QCZZ	AW		C	Connector
2	QCNCP4841QCZZ	AT		C	Connector
3	QCNCW1001ACZZ	AZ		C	Connector
4	QCNCM1004ACZZ	AQ		C	Connector
6	QCNW-1007ACZZ	AX	N	C	Connector
9	QCNCW0207HCZZ	AK		C	Connector
10	QCNCM1009ACZH	AC		C	Connector
11	QCNCM1009ACZ1	AC		C	Connector
12	QCNCM1009ACZB	AA		C	Connector
13	QCNCM1009ACZG	AC		C	Connector
14	QCNCM1009ACZE	AB		C	Connector
16	QCNCW1008AC01	AC		C	Connector
17	QCNCW1008AC02	AF		C	Connector
18	QCNW-1047ACZZ	AM	N	C	Connector for CRT-2
19	QCNW-1044ACZZ	AM	N	C	Connector for CRT-1
20	QCNW-1004ACZZ	AM	N	C	Connector for key board
21	QCNW-1003ACZZ	AK	N	C	Connector for light pen
26	LHLDF6648RCZZ	AB		C	Holder



4 Others

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	RMEMR1004AC07	BA		D	Master media
9	UBNDA1008CCZZ	AA		D	AC Cord band
10	SPAKA1003ACZZ	AZ	N	D	Packing cushion
13	SSAKH3002KCZZ	AD		D	Plastic bag

5 CPU PWB

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	LANGQ1004ACZZ	AH	N	C	Connector "A" angle
2	LHLDF6648RCZZ	AB		C	Holder
3	QCNCW0207HCZZ	AK		C	Connector
4	QCNCW1001ACZZ	AZ		C	Connector
5	QCNCM1009ACZB	AA		C	Connector
6	QCNCM1009ACZE	AB		C	Connector
7	QCNCM1009ACZG	AC		C	Connector
8	QCNCM1009ACZH	AC		C	Connector
9	QCNCM1009ACZ1	AC		C	Connector
10	QCNCP4841QCZZ	AT		C	Connector
11	QCNCP6041QCZZ	AW		C	Connector
12	QSOCZ6414ACZZ	AD		C	IC socket (14pin)
13	QSOCZ6416ACZZ	AD		C	IC socket (16pin)
14	QSOCZ6424ACZZ	AE		C	IC socket (24pin)
15	QSOCZ6428ACZZ	AE		C	IC socket (28pin)
16	QSOCZ6440ACZZ	AG		C	IC socket (40pin)
17	QSW-Z1002SCZZ	AZ		B	Dip SW
18	QSW-Z2005SCZZ	AK		B	Dip SW
19	QSW-Z9660KCZZ	AR		B	Dip SW
20	RC-KZ1018CCZZ	AE		C	Capacitor
21	RCRS-1001ACZZ	AU	N	B	X-Tal (39 32MHz)
22	RCRS-1002ACZZ	AU	N	B	X-Tal (32MHz)
23	RCRS-1003ACZZ	AU	N	B	X-Tal (2 45MHz)
24	RCRSP1003CCZZ	AT		B	X-Tal (32KHz)
25	RMPTC4333QCKB	AC		C	Block resistor (1/8W 33KΩ×4)
26	RMPTC4682QCKB	AC		C	Block resistor (1/8W 6 8KΩ×4)
27	RMPTC8333QCKB	AD		B	Block resistor (33KΩ×8 1/8W ±10%)
28	UBATN1001ACZZ	AS	N	A	Battery
29	VCCSPU1HL100D	AA		C	Capacitor (50V 10PF)
30	VCCSPU1HL330J	AA		C	Capacitor (50WV 33PF)
31	VCCSPU1HL470J	AA		C	Capacitor (50V 47PF)
32	VCEAAA1CW106Q	AB		C	Capacitor (16WV 10μF)
33	VCEAAA1CW107M	AB		C	Capacitor (16WV 100μF)
34	VCEAAA1CW336M	AB		C	Capacitor (16WV 33μF)
35	VCEAAA1EW106M	AB		C	Capacitor (25WV 10μF)
36	VCEAAA1EW107M	AC		C	Capacitor (25WV 100μF)
37	VCEAAA1EW227M	AC		C	Capacitor (25WV 220μF)
38	VCEAAA1HW105M	AB		C	Capacitor (50WV 1 0μF)
39	VCEAAA1HW335M	AB		C	Capacitor (50WV 3 3μF)
40	VCEAAA1HW475M	AB		C	Capacitor (50WV 4 7μF)
41	VCKYPA1HB681K	AA		C	Capacitor (50WV 680PF)
42	VCKYPA1HB681K	AA		C	Capacitor (50WV 680PF)
43	VCKYPU1HB221K	AB		C	Capacitor (50WV 220PF)
44	VCKYPU1HB561K	AA		C	Capacitor (50WV 560PF)
45	VCTYPA1NX104M	AB		C	Capacitor (12WV 0 10μF)
46	VCTYPA1NX104M	AB		C	Capacitor (12WV 0 10μF)
47	VCTYPU1EX103M	AB		C	Capacitor (25WV 0 010μF)
48	VHDDS1588L1-1	AD		B	Diode (1S1588L1)
49	VHiHM472114-1	AU		B	IC
50	VHiHM6116P3-1	BN		B	IC
51	VHiLH0080A/-1	AX		B	IC
52	VHiM58725P-15	AZ		B	IC
53	VHiM74LS00/-1	AE		B	IC
54	VHiM74LS02/-1	AE		B	IC
55	VHiM74LS03/-1	AE		B	IC
56	VHiM74LS04/-1	AE		B	IC
57	VHiM74LS08/-1	AE		B	IC
58	VHiM74LS10/-1	AE		B	IC
59	VHiM74LS125-1	AH		B	IC
60	VHiM74LS138-1	AK		B	IC
61	VHiM74LS139-1	AL		B	IC
62	VHiM74LS14/-1	AM		B	IC
63	VHiM74LS157-1	AK		B	IC
64	VHiM74LS166-1	AL		B	IC
65	VHiM74LS244-1	AM		B	IC
66	VHiM74LS245-1	AR		B	IC
67	VHiM74LS273-1	AP		B	IC
68	VHiM74LS32/-1	AF		B	IC

5 CPU PWB

NO	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
69	VHiM74LS367−1	AH		B	IC
70	VHiM74LS373−1	AQ		B	IC
71	VHiM74LS74/−1	AG		B	IC
72	VHiM74LS75/−1	AE		B	IC
73	VHiM74LS86/−1	AF		B	IC
74	VHiM74LS93/−1	AK		B	IC
75	VHiSN7404N/−1	AF		B	IC
76	VHiSN7406N/−1	AG		B	IC
77	VHiSN74157N−1	AM		B	IC
78	VHiSN75188N−1	AM		B	IC
79	VHiSN75189A−1	AP		B	IC
80	VHiSP6102C002	BG		B	IC
81	VHiSP6102C003	BG		B	IC
82	VHiSP6102R001	BP		B	IC
83	VHiTA7313AP−1	AL		B	IC
84	VHiTC4049P/−1	AN		B	IC
85	VHiUPD1990ACC	AT		B	IC
86	VHiUPD7220D−1	BS		B	IC
87	VHiUPD8255/−1	AY		B	IC
88	VHi2764//AC01	LM		B	LSI PROM−IPL
	VHi2764//AC02	LM		B	LSI PROM−CG (English)
	VHi2764//AC03	LM		B	LSI PROM−CG (Germany)
	VHi2764//AC04	LM		B	LSI PROM−CG (French)
89	VHi4164−150−H	AZ		B	IC
90	VHi8251AC//−1	AY		B	IC
91	VHi8253////−1	BA		B	IC
92	VHPGL3PR2//−1	AE		B	Photo transistor GL3PR2
93	VRD−ST2EY331J	AA		C	Resistor (1/4W 330Ω J)
94	VRD−ST2EY470J	AA		C	Resistor (EX 110V,220V only) (1/4W 47Ω ±5%)
95	VRD−RV2EY000J	AA		C	Resistor (1/4W ±5%)
96	VRD−ST2EY101J	AA		C	Resistor (1/4W 100Ω ±5%)
97	VRD−ST2EY102J	AA		C	Resistor (1/4W 1KΩ)
98	VRD−ST2EY103J	AA		C	Resistor (1/4W 10KΩ)
99	VRD−ST2EY104J	AA		C	Resistor (1/4W 100KΩ ±5%)
100	VRD−ST2EY222J	AA		C	Resistor (Japan only) (1/4W 2 2KΩ ±5%)
101	VRD−ST2EY331J	AA		C	Resistor (1/4W 330Ω J)
102	VRD−ST2EY332J	AA		C	Resistor (1/4W 3 3KΩ ±5%)
103	VRD−ST2EY333J	AA		C	Resistor (1/4W 33KΩ)
104	VRD−ST2EY561J	AA		C	Resistor (1/4W 560Ω J)
105	VRD−RV2EY682J	AA		C	Resistor (1/4W 6 8KΩ ±5%)
106	VRD−SU2EY152J	AA		C	Resistor (1/4W 1 5KΩ J)
107	VRD−SU2EY470J	AA		C	Resistor (47Ω)
108	VRD−SU2EY681J	AA		C	Resistor (1/4W 680Ω J)
109	VRD−SU2EY821J	AA		C	Resistor (1/4W 820Ω ±5%)
110	VRD−SU2EY822J	AA		C	Resistor (1/4W 8 2KΩ ±5%)
111	VS2SC458KC/−1	AD		B	Transistor
112	XBPSD30P06KS0	AA		C	Screw
113	XBPSD30P08000	AA		C	Screw

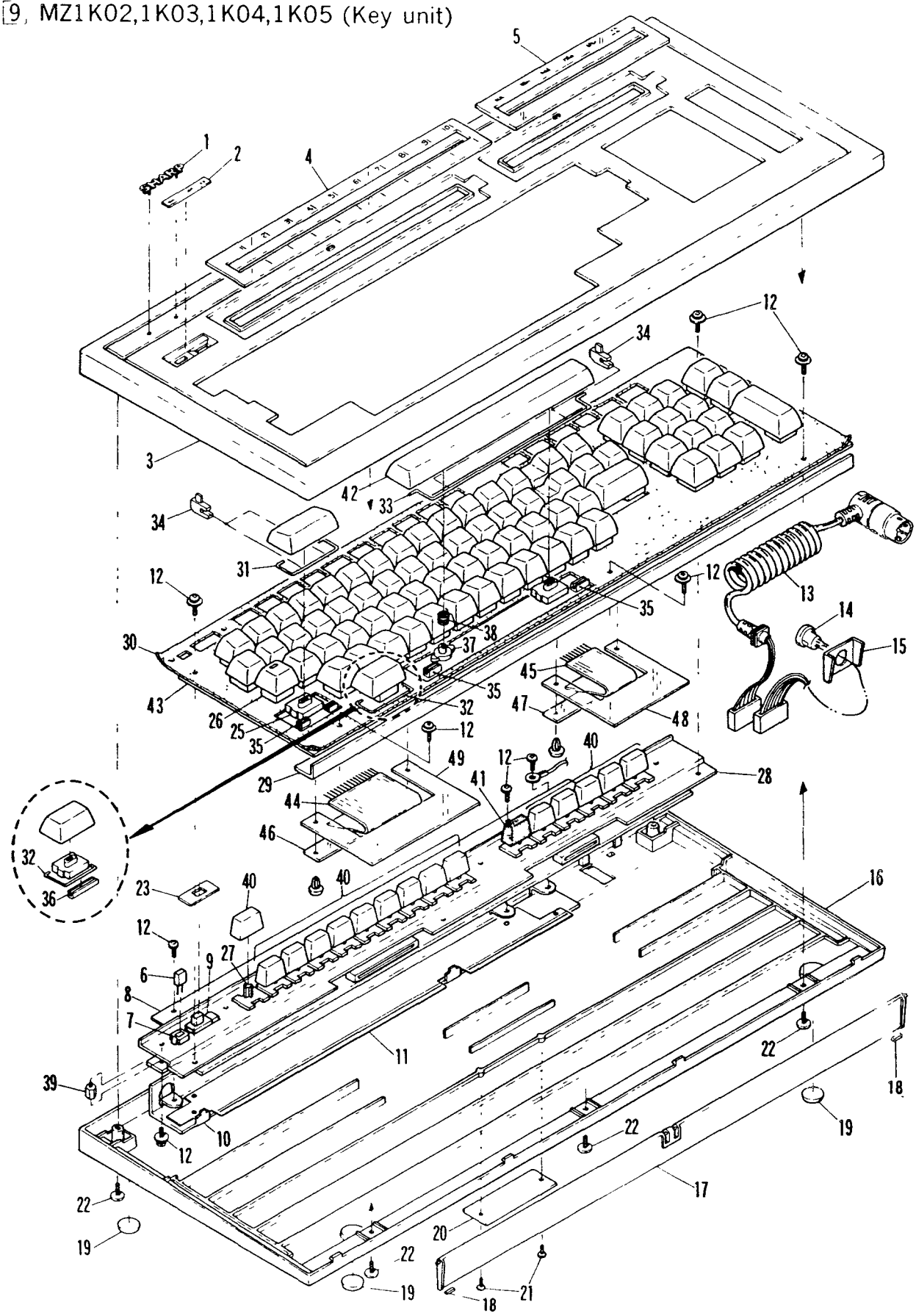
6 Power supply unit

NO	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
1	0AE3021690 4//	AS	N	B	IC (UPC78M12H)	[M001]
2	0AE3026302 5//	AD	N	B	Transistor (2SC1815−Y)	[Q001]
3	0AE3026302 5//	AF	N	B	Transistor (2SC1815−Y)	[Q002]
4	0AE3010906 6//	AE	N	B	Transistor (2SA733−Q)	[Q003]
5	0AE3010906 6//	AE	N	B	Transistor (2SA733−Q)	[Q004]
6	0AE3025878 4//	AX	N	B	Transistor (2SC2750−L)	[Q005]
7	0AE3022151 7//	AL	N	B	Transistor (2SA965−Y)	[Q006]
8	0AE3022152 0//	AH	N	B	Transistor (2SC1627−Y)	[Q007]
9	0AE3026302 5//	AD	N	B	Transistor (2SC1815−Y)	[Q008]
10	0AE3036205 2//	AD	N	B	Transistor (2SA1015−Y)	[Q009]
11	0AE3026302 5//	AD	N	B	Transistor (2SC1815−Y)	[Q010]
12	0AE3026302 5//	AD	N	B	Transistor (2SC1815−Y)	[Q011]
13	0AE3026302 5//	AD	N	B	Transistor (2SC1815−Y)	[Q012]
14	0AE3010906 6//	AE	N	B	Transistor (2SA733−Q)	[Q013]
15	0AE3010906 6//	AE	N	B	Transistor (2SA733−Q)	[Q014]
16	0AE3027984 4//	AH	N	B	Transistor (2SA1020−Y)	[Q015]
17	0AE3016737 0//	AT	N	B	Transistor (2SC2334−L)	[Q016]
18	0AE3022154 6//	AH	N	B	Transistor (2SC2655−Y)	[Q017]
19	0AE3026302 5//	AD	N	B	Transistor (2SC1815−Y)	[Q018]
20	0AE3026943 0//	AY	N	B	Transistor (S10SC4M)	[DU001]
21	0AE3026165 8//	AD	N	B	Zener diode (HZ9L−A1)	[D001]
22	0AE3012194 7//	AF	N	B	Diode (1S2348H)	[D002]
23	0AE3049983 1//	AD	N	B	Zener diode (HZ11L−B1)	[D003]
24	0AE3036208 1//	AD	N	B	Zener diode (HZ7L−C2)	[D004]

6 Power supply unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
25	0AE3012192 1//	AC	N	B	Diode (1S2076A-FEC)	[D005]
26	0AE3012192 1//	AC	N	B	Diode (1S2076A-FEC)	[D006]
27	0AE3037902 9//	AD	N	B	Zener diode (HZ7L-B2)	[D007]
28	0AE3012192 1//	AC	N	B	Diode (1S2076A-FEC)	[D008]
29	0AE3012192 1//	AC	N	B	Diode (1S2076A-FEC)	[D009]
30	0AE3020077 4//	AG	N	B	Diode (30DF-1)	[D010]
31	0AE3020077 4//	AG	N	B	Diode (30DF-1)	[D011]
32	0AE3037902 9//	AD	N	B	Zener diode (HZ7L-32)	[D012]
33	0AE3025032 6//	AG	N	B	Diode (10DF-1)	[D013]
34	0AE3012192 1//	AC	N	B	Diode (1S2076A-FEC)	[D014]
35	0AE3015987 0//	AY	N	B	Diode (S10VB10)	[RC001]
36	0AE3012186 6//	AN	N	B	Diode (1B4B1)	[RC002]
37	0AE3016526 2//	AH	N	B	Thyristor (03P05M)	[TH001]
38	0AE3051135 3//	AP	N	C	Capacitor (0.22μF 250V)	[C001]
	0AE3027239 1//	AP	N	C	Capacitor (0.1μF 125V)	[C001]
39	0AE3050972 1//	AG	N	C	Capacitor (DE1107E222M250VAC)	[C002]
40	0AE3050972 1//	AG	N	C	Capacitor (DE1107E222M250VAC)	[C003]
41	0AE3052337 0//	AP	N	C	Capacitor (KM50VRSN10000HR)	[C004]
42	0AE3014357 2//	AC	N	C	Capacitor (50F2S102K)	[C005]
43	0AE3014357 2//	AC	N	C	Capacitor (50F2S102K)	[C006]
44	0AE3012065 0//	AG	N	C	Capacitor (50F2S154K)	[C007]
45	0AE3016965 3//	AC	N	C	Capacitor (50ULB10-M)	[C008]
46	0AE3022723 6//	AD	N	C	Capacitor (10ULB220-M)	[C009]
47	0AE3012052 4//	AC	N	C	Capacitor (50F2S223K)	[C011]
48	0AE3012946 0//	AC	N	C	Capacitor (50F2S103K)	[C012]
49	0AE3012946 0//	AC	N	C	Capacitor (50F2S103K)	[C013]
50	0AE3012946 0//	AC	N	C	Capacitor (50F2S103K)	[C014]
51	0AE3028067 1//	AE	N	C	Capacitor (35ULB33-M)	[C015]
52	0AE3016557 6//	AG	N	C	Capacitor (10ULB1000-M)	[C016]
53	0AE3016557 6//	AG	N	C	Capacitor (10ULB1000-M)	[C017]
54	0AE3016965 3//	AD	N	C	Capacitor (50ULB10-M)	[C018]
55	0AE3016965 3//	AD	N	C	Capacitor (50ULB10-M)	[C019]
56	0AE3012052 4//	AC	N	C	Capacitor (50F2S223K)	[C020]
57	0AE3016440 9//	AC	N	C	Capacitor (50F2S332K)	[C021]
58	0AE3012045 6//	AC	N	C	Capacitor (50F2S472K)	[C022]
59	0AE3012946 0//	AC	N	C	Capacitor (50F2S103K)	[C023]
60	0AE3012045 6//	AC	N	C	Capacitor (50F2S472K)	[C024]
61	0AE3017000 8//	AG	N	C	Capacitor (25ULB330-M)	[C025]
62	0AE3017000 8//	AG	N	C	Capacitor (25ULB330-M)	[C026]
63	0AE3021352 5//	AG	N	C	Capacitor (35ULB220-M)	[C027]
64	0AE3019525 8//	AG	N	C	Capacitor (25ULB220-M)	[C028]
65	0AE3012052 4//	AC	N	C	Capacitor (50F2S223K)	[C029]
66	0AE3012052 4//	AC	N	C	Capacitor (50F2S223K)	[C030]
67	0AE3016440 9//	AC	N	C	Capacitor (50F2S332K)	[C031]
68	0AE3011672 9//	AK	N	C	Resistorr (TM10K(PVB)B 2KΩ)	[RV001]
69	0AE3011672 9//	AK	N	C	Resistorr (TM10K(PVB)B 2KΩ)	[RV002]
70	VRS-PT3AB102J	AC	N	C	Resistorr (RS1FB 1KΩJ)	[R001]
71	VRS-PT3DB152K	AB	N	C	Resistorr (RS2FB 1.5KΩJ)	[R002]
72	VRD-ST2EY152J	AA	N	C	Resistorr (CR25 1.5KΩJ)	[R003]
73	VRD-ST2EY333J	AA	N	C	Resistorr (CR25 33KΩJ)	[R004]
74	VRD-ST2EY333J	AA	N	C	Resistorr (CR25 33KΩJ)	[R005]
75	VRD-ST2EY152J	AA	N	C	Resistorr (CR25 1.5KΩJ)	[R006]
76	0AE3049116 9//	AE	N	C	Wire resistor	[R007]
77	VRD-ST2EY100J	AA	N	C	Resistor (CR25 10ΩJ F)	[R008]
78	VRD-ST2EY102J	AA	N	C	Resistor (CR25 1KΩJ)	[R009]
79	0AE3050804 9//	AG	N	C	Resistor (MDS 05N 5.6Ω)	[R010]
80	VRD-ST2EY4R7J	AB	N	C	Resistor (CR37 4.7ΩJ)	[R012]
81	0AE3050186 8//	AC	N	C	Resistor (RS1FB 63ΩJ)	[R013]
82	0AE3014328 4//	AC	N	C	Resistor (MR25 47ΩG)	[R014]
83	VRD-ST2EY331J	AA	N	C	Resistor (CR25 330ΩJ F)	[R015]
84	VRS-PT3AB100J	AB	N	C	Resistor (RS1FB 10ΩJ)	[R016]
85	VRD-ST2EY272J	AA	N	C	Resistor (CR25 2.7KΩJ F)	[R017]
86	VRD-ST2EY102J	AA	N	C	Resistor (CR25 1KΩJ F)	[R018]
87	VRD-ST2EY391J	AA	N	C	Resistor (CR25 390ΩJ F)	[R019]
88	VRD-ST2EY471J	AA	N	C	Resistor (CR25 470ΩJ)	[R020]
89	VRD-ST2EY331J	AA	N	C	Resistor (CR25 330ΩJ F)	[R021]
90	VRD-ST2EY182J	AA	N	C	Resistor (CR25 1.8KΩJ F)	[R022]
91	VRD-ST2EY152J	AA	N	C	Resistor (CR25 1.5KΩJ F)	[R023]
92	VRD-ST2EY222J	AA	N	C	Resistor (CR25 2.2KΩJ F)	[R024]
93	VRD-ST2EY102J	AA	N	C	Resistor (CR25 1KΩJ F)	[R025]
94	VRD-ST2EY222J	AA	N	C	Resistor (CR25 2.2KΩJ F)	[R026]
95	VRD-ST2EY681J	AA	N	C	Resistor (CR25 680ΩJ)	[R027]
96	VRD-ST2EY220J	AA	N	C	Resistor (CR25 22ΩJ)	[R028]
97	VRD-ST2EY102J	AA	N	C	Resistor (CR25 1KΩJ F)	[R029]
98	VRD-ST2EY102J	AA	N	C	Resistor (CR25 1KΩJ)	[R030]
99	VRD-ST2EY331J	AA	N	C	Resistor (CR25 330ΩJ)	[R031]
100	VRD-ST2EY331J	AA	N	C	Resistor (CR25 330ΩJ)	[R032]
101	0AE3049094 0//	AE			Wire resistor	[R033]
102	VRD-ST2EY390J	AA	N	C	Resistor (CR25 39ΩJ F)	[R034]
103	VRD-ST2EY151J	AA	N	C	Resistor (CR25 150ΩJ F)	[R035]

9, MZ1K02,1K03,1K04,1K05 (Key unit)



10 MZ1R03 (Graphic board)

NO	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	DUNTK1025ACZZ	**	N	E	PWB unit
2	SPAKA1013ACZZ	AH	N	C	Packing cushion
3	SPAKC1078ACZZ	AK	N	C	Packing case
4	XBPSD40P06000	AA	N	C	Screw
5	TSELF0003PAZZ	AA		D	Sealing label
6	LANGT1008ACZZ	AF	N	C	Angle
7	QSOCZ6416ACZZ	AD		C	IC socket
8	QSOCZ6440ACZZ	AG		C	LSI socket
9	RC-CZ1000QCZZ	AB		C	Capacitor
10	RC-SZ2001HCZZ	AF		C	Capacitor
11	VCEAAU1CW107M	AB		C	Capacitor (16V 100μF)
12	VCEAAU1CW336M	AB		C	Capacitor (16V 33μF)
13	VCEAAU1EW107M	AB		C	Capacitor (25V 100μF)
14	VCKYPA1HB331K	AA		C	Capacitor (50V 330pF)
15	VCTYPA1NX104M	AB		C	Capacitor (12V 0.1μF)
16	VHERD5 6E5/-1	AC		B	Zener diode
17	VHiM5K4116P-2	AP		B	LSI RAM
18	VHiM74LS00/-1	AE		B	IC
19	VHiM74LS157-1	AK		B	IC
20	VHiM74LS166-1	AL		B	IC
21	VHiM74LS244-1	AM		B	IC
22	VHiM74LS273-1	AP		B	LC
23	VHiM74LS367-1	AH		B	IC
24	VHiM74LS373-1	AQ		B	IC
25	VHiSN7404//-1	AE		B	IC
26	VHiUPD7220D-1	BS		B	LSI
27	VRD-ST2EY101J	AA		C	Resistor (1/2W 100Ω)
28	VRD-ST2EY103J	AA		C	Resistor (1/2W 10KΩ)
29	VRD-ST2EY331J	AA		C	Resistor (1/2W 330Ω)
30	VRD-ST2EY332J	AA		C	Resistor (1/2W 3.3KΩ)
31	VRD-SU2EY470J	AA		C	Resistor (1/2W 47Ω)
32	VRS-PT3DB680K	AB		C	Resistor (2W 68Ω)
33	VS2SA673-D1-1	AC		B	Transistor (2SA673D)
34	XBTSD30P04000	AA		C	Screw (30×4)

11 MZ1R06 (RAM board)

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	LBNDJ0009FCZZ	AC		D	Clamp band
2	SPAKA1016ACZZ	AF	N	D	Packing cushion
3	SPAKC1082ACZZ	AH	N	D	Packing case
4	TiNSJ1009ACZZ	AE	N	D	Instruction book
5	TiNSM1017ACZZ	AG	N	D	Instruction book
6	QSOCZ6416ACZZ	AD		C	IC socket
7	VCEAAA1CW476M	AB		C	Capacitor (16V 47μF)
8	VCTYPA1NX104M	AB		C	Capacitor (12V 0.1μF)
9	VHiM74LS367-1	AH		B	IC
10	VHiSN74157/-1	AH		B	IC
11	VHi4164-150-H	AZ		B	LSI DRAM
12	VRD-RV2EY101J	AA		C	Resistor
13	DUNTK1028ACZZ	**			PWB unit

■ Index

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK
[C]				
CCABC1007ACZZ	1- 1	AY		D
[D]				
DUNT-1018ACZZ	1- 17	**	N	E
DUNT-1035ACZZ	1- 17	**		E
DUNTK1025ACZZ	10- 1	**	N	E
DUNTK1028ACZZ	11- 13	**		
DUNTK1060ACZZ	2- 11	**	N	E
DUNTK1064ACZZ	2- 9	**		E
DUNTK1082ACZZ	2- 9	**		E
DUNTK1083ACZZ	2- 9	**		E
DUNTK1085ACZZ	9- 8	**		E
[G]				
GCABA1001ACZZ	9- 16	AS	N	D
GCABA1003ACZZ	1- 9	BM	N	D
GCABB1002ACZZ	9- 3	AR	N	D
GCABB1004ACZZ	1- 18	BG	N	D
GCOVH1001ACZZ	1- 19	AM	N	D
GFTAF1001ACZZ	1- 2	AE	N	D
GFTAF1002ACZZ	1- 35	AE		D
GFTAR1003ACZZ	2- 12	AD	N	D
GFTAR1004ACZZ	2- 13	AC	N	D
GFTAU1005ACZZ	1- 10	AL	N	D
GLEGG1001ACZZ	9- 18	AA	N	C
GLEGP0010UCZZ	1- 26	AB		C
GLEGP1001CCZZ	9- 19	AB		C
GSTN-1001ACZZ	9- 17	AE	N	D
[H]				
HBDGB3004GESA	1- 3	AE		D
//	9- 1	AE	N	D
[J]				
JKNBM0004PAZZ	2- 1	AC	N	C
[L]				
LANGK1007ACZZ	2- 3	AB	N	C
LANGQ1004ACZZ	2- 24	AH	N	C
//	5- 1	AH	N	C
LANGQ1005ACZZ	2- 25	AF	N	C
//	8- 1	AF	N	C
LANGS1006ACZZ	2- 2	AF	N	C
LANGT1001ACZZ	9- 10	AG		C
LANGT1002ACZZ	9- 15	AC		C
LANGT1003ACZZ	1- 20	AX	N	C
LANGT1008ACZZ	10- 6	AF	N	C
LANGT1010ACZZ	1- 21	AE		C
LBNDJ0009FCZZ	11- 1	AC		D
LCHSM1008ACZZ	1- 22	AY		C
LHLDF6648RCZZ	2- 34	AB		C
//	3- 26	AB		C
//	5- 2	AB		C
LHLDW6655RCZZ	1- 36	AB		C
//	1- 40	AB		C
LHLDZ1001ACZZ	2- 15	AD	N	C
LPLTP1001ACZZ	9- 5	AC	N	D
LPLTP1072CCZZ	9- 4	AD		D
LX-BZ1001ACZZ	1- 29	AC		C
LX-LZ6023RCZZ	1- 23	AA		C
[N]				
NFANP1001ACZZ	1- 24	BM	N	B
[P]				
PCUSG1001ACZZ	2- 26	AA	N	C
//	2- 35	AA	N	C
//	8- 2	AA	N	C
PCUSU1003ACZZ	9- 100	AA		C
PHOG-1001ACZZ	1- 34	AC	N	C
PHOG-1002ACZZ	2- 32	AC	N	C
PSLDM1001ACZZ	9- 11	AN		C
PSLDM1003ACZZ	1- 41	AP		C
PSLDP1001ACZZ	9- 23	AB		C
PSPAG1004ACZZ	1- 11	AC		C
PSPAX1001ACZZ	9- 7	AB		C
PZETY1001ACZZ	2- 27	AE	N	C
//	8- 3	AE	N	C
[Q]				
QCNCM1002ACZZ	2- 28	AQ		C
//	8- 4	AQ		C
QCNCM1004ACZZ	3- 4	AQ		C
//	8- 5	AQ		C
QCNCM1009ACZB	3- 12	AA		C
//	5- 5	AA		C
QCNCM1009ACZE	3- 14	AB		C

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK
QCNCM1009ACZE	5- 6	AB		C
QCNCM1009ACZG	3- 13	AC		C
//	5- 7	AC		C
QCNCM1009ACZH	3- 10	AC		C
//	5- 8	AC		C
//	9- 101	AC		C
QCNCM1009ACZ1	3- 11	AC		C
//	5- 9	AC		C
QCNCM1009ACZJ	9- 102	AC		C
QCNCP4841QCZZ	3- 2	AT		C
//	5- 10	AT		C
QCNCP6041QCZZ	3- 1	AW		C
//	5- 11	AW		C
QCNCW0207HCZZ	3- 9	AK		C
//	5- 3	AK		C
QCNCW1001ACZZ	3- 3	AZ		C
//	5- 4	AZ		C
QCNCW1006ACZZ	9- 103	AD		C
QCNCW1007ACZZ	9- 104	AE		C
QCNCW1008AC01	1- 6	AC		C
//	3- 16	AC		C
QCNCW1008AC02	2- 4	AF		C
//	3- 17	AF		C
QCNW-1001ACZZ	9- 13	BB		B
QCNW-1002ACZZ	9- 14	AP		C
QCNW-1003ACZZ	2- 16	AK	N	C
//	3- 21	AK	N	C
QCNW-1004ACZZ	2- 17	AM	N	C
//	3- 20	AM	N	C
QCNW-1007ACZZ	2- 29	AX	N	C
//	3- 6	AX	N	C
//	8- 6	AX	N	C
QCNW-1044ACZZ	2- 19	AM	N	C
//	3- 19	AM	N	C
QCNW-1047ACZZ	2- 18	AM	N	C
//	3- 18	AM	N	C
QLUGL0006UCZZ	1- 37	AB		C
QPIN-2005SCZZ	8- 7	AA		C
QPWBF1005ACZZ	1- 7	AA	N	C
QSOCZ6414ACZZ	5- 12	AD		C
QSOCZ6416ACZZ	5- 13	AD		C
//	10- 7	AD		C
//	11- 6	AD		C
QSOCZ6424ACZZ	5- 14	AE		C
QSOCZ6428ACZZ	5- 15	AE		C
QSOCZ6440ACZZ	5- 16	AG		C
//	8- 8	AG		C
//	9- 105	AG		C
//	10- 8	AG		C
QSW-K1002ACZZ	9- 43	BU	N	E
QSW-K1003ACZZ	9- 43	BU	N	E
QSW-K1004ACZZ	9- 43	BU	N	E
QSW-K1005ACZZ	9- 43	BU	N	E
QSW-K1007ACZZ	2- 5	AE	N	B
QSW-S1006ACZZ	9- 9	AF		B
QSW-Z1002SCZZ	5- 17	AZ		B
QSW-Z2005SCZZ	5- 18	AK		B
QSW-Z9660KCZZ	5- 19	AR		B
[R]				
RC-CZ1000QCZZ	8- 9	AB		C
//	9- 106	AB		C
//	10- 9	AB		C
RC-KZ1018CCZZ	5- 20	AE		C
RC-SZ2001HCZZ	10- 10	AF		C
RCRS-1001ACZZ	5- 21	AU	N	B
RCRS-1002ACZZ	5- 22	AU	N	B
RCRS-1003ACZZ	5- 23	AU	N	B
RCRS-1004ACZZ	9- 107	AG		B
RCRSP1003CCZZ	5- 24	AT		B
RMEMR1002ACZZ	1- 25	**	N	E
RMEMR1004AC07	4- 1	BA		D
RMPTC4331QCKB	8- 10	AB		B
RMPTC4333QCKB	5- 25	AC		C
RMPTC4682QCKB	5- 26	AC		C
RMPTC8333QCKB	5- 27	AD		B
RMPTC8333QCKJ	9- 108	AD		C
RVR-A5452QCZZ	2- 6	AF		B
RVR-MC321QCZZ	8- 11	AH		C
[S]				
SPAKA1003ACZZ	4- 10	AZ	N	D

PARTS CODE	NO	PRICE RANK	NEW MARK	PART RANK
SPAKA1004ACZZ	9- 109	AG		D
SPAKA1009ACZZ	9- 110	AB		D
SPAKA1013ACZZ	10 2	AH	N	C
SPAKA1016ACZZ	11- 2	AF	N	D
SPAKA1045ACZZ	9- 111	AP	N	D
SPAKA1127ACZZ	9 112	AD	N	D
SPAKC1033ACZZ	9 113	AP	N	D
SPAKC1035ACZZ	9- 113	AP	N	D
SPAKC1037ACZZ	9- 113	AP	N	D
SPAKC1039ACZZ	9- 113	AP	N	D
SPAKC1078ACZZ	10- 3	AK	N	C
SPAKC1082ACZZ	11- 3	AH	N	D
SPAKF1104ACZZ	9- 114	AD		D
SSAKH3002KCZZ	4- 13	AD		D
【T】				
TINSJ1009ACZZ	11- 4	AE	N	D
TINSM1017ACZZ	11 5	AG	N	D
TLABJ1769CCZZ	9- 115	AA		D
TLABZ1002ACZZ	9- 2	AA	N	D
TLABZ1003ACZZ	1- 4	AB	N	D
TLABZ1008ACZZ	1- 5	AA	N	D
TLABZ1017ACZZ	1- 12	AC		C
TLABZ1400CCZZ	1- 41	AA		C
TSELF0003PAZZ	10- 5	AA		D
TSPC-1010ACZZ	9- 20	AC	N	D
TSPC-1011ACZZ	9- 20	AC	N	D
TSPC-1012ACZZ	9- 20	AC	N	D
TSPC-1013ACZZ	9- 20	AC	N	D
【U】				
UBATN1001ACZZ	5- 28	AS	N	A
UBNDA1008CCZZ	4- 9	AA		D
【V】				
VCCCPU1HH201J	8- 12	AB		C
VCCCPU1HH680J	8- 13	AB		C
VCCSPU1HL100D	5- 29	AA		C
〃	9- 116	AA		C
VCCSPU1HL330J	5- 30	AA		C
〃	8- 14	AA		C
VCCSPU1HL470J	5- 31	AA		C
〃	8- 15	AA		C
〃	9- 117	AA		C
VCEAAA1CW106Q	5- 32	AB		C
VCEAAA1CW107M	5- 33	AB		C
〃	8- 16	AB		C
VCEAAA1CW336M	5- 34	AB		C
VCEAAA1CW476M	11- 7	AB		C
VCEAAA1EW106M	5- 35	AB		C
VCEAAA1EW107M	5- 36	AC		C
VCEAAA1EW227M	5- 37	AC		C
VCEAAA1HW105M	5- 38	AB		C
VCEAAA1HW225M	8- 17	AB		C
VCEAAA1HW335M	5- 39	AB		C
VCEAAA1HW475M	5- 40	AB		C
VCEAAU1CW107M	10- 11	AB		C
VCEAAU1CW336M	9- 118	AB		C
〃	10- 12	AB		C
VCEAAU1CW475M	9- 119	AB		C
VCEAAU1EW107M	10- 13	AB		C
VCKYPA1HB331K	10- 14	AA		C
VCKYPA1HB681K	5- 41	AA		C
〃	5- 42	AA		C
VCKYPU1HB102K	8- 18	AA		C
〃	8- 19	AA		C
VCKYPU1HB221K	5- 43	AB		C
VCKYPU1HB561K	5- 44	AA		C
VCSATU1VE104M	8- 20	AC		C
VCTYPA1NX104M	5- 45	AB		C
〃	5- 46	AB		C
〃	8- 21	AB		C
〃	8- 22	AB		C
〃	10- 15	AB		C
〃	11 8	AB		C
VCTYPU1EX103M	5- 47	AB		C
〃	8- 23	AB		C
〃	9- 120	AB		C
VHDDS1588L1-1	5- 48	AD		B
〃	8 24	AB		B
〃	9 121	AD		B
VHERD5 6E5/-1	10 16	AC		B
VHID8749HAC05	9 125	BR	N	B

PARTS CODE	NO	PRICE RANK	NEW MARK	PART RANK
VHIHM472114-1	5- 49	AU		B
VHIHM6116P3-1	5- 50	BN		B
VHILH0080A/-1	5- 51	AX		B
VHIM5K4116P-2	10- 17	AP		B
VHIM58725P-15	5- 52	AZ		B
VHIM74LS00/-1	5- 53	AE		B
〃	10- 18	AE		B
VHIM74LS02/-1	5- 54	AE		B
〃	8- 25	AE		B
VHIM74LS03/-1	5- 55	AE		B
VHIM74LS04/-1	5- 56	AE		B
VHIM74LS08/-1	5- 57	AE		B
〃	8- 26	AE		B
VHIM74LS10/-1	5- 58	AE		B
〃	8- 27	AE		B
VHIM74LS125-1	5- 59	AH		B
VHIM74LS126-1	8- 28	AH		B
VHIM74LS138-1	5- 60	AK		B
VHIM74LS139-1	5- 61	AL		B
VHIM74LS14/-1	5- 62	AM		B
VHIM74LS157-1	5- 63	AK		B
〃	8- 29	AK		B
〃	10- 19	AK		B
VHIM74LS161-1	8- 30	AH		B
VHIM74LS163-1	8- 31	AH		B
VHIM74LS166-1	5- 64	AL		B
〃	10- 20	AL		B
VHIM74LS21/-1	8- 32	AD		B
VHIM74LS221-1	8- 33	AH		B
VHIM74LS244-1	5- 65	AM		B
〃	10- 21	AM		B
VHIM74LS245-1	5- 66	AR		B
VHIM74LS27/-1	8- 34	AF		B
VHIM74LS273-1	5- 67	AP		B
〃	8- 35	AP		B
〃	10- 22	AP		B
VHIM74LS293-1	8- 36	AG		B
VHIM74LS32/-1	5- 68	AF		B
〃	8- 37	AF		B
VHIM74LS367-1	5- 69	AH		B
〃	10- 23	AH		B
〃	11- 9	AH		B
VHIM74LS373-1	5- 70	AQ		B
〃	10- 24	AQ		B
VHIM74LS74/-1	5- 71	AG		B
〃	8- 38	AG		B
VHIM74LS75/-1	5- 72	AE		B
VHIM74LS86/-1	5- 73	AF		B
VHIM74LS93/-1	5- 74	AK		B
VHIM7438///-1	8- 39	AE		B
VHINE555///-1	8- 40	AG		B
VHISN7404//-1	10- 25	AE		B
VHISN7404N/-1	5- 75	AF		B
〃	8- 41	AF		B
VHISN7406N/-1	5- 76	AG		B
VHISN7414N/-1	8- 42	AM		B
VHISN74157/-1	11- 10	AH		B
VHISN74157N-1	5- 77	AM		B
VHISN75188N-1	5- 78	AM		B
VHISN75189A-1	5- 79	AP		B
VHISP6102C002	5- 80	BG		B
VHISP6102C003	5- 81	BG		B
VHISP6102R001	5- 82	BP		B
VHITA7313AP-1	5- 83	AL		B
VHITC4049P/-1	5- 84	AN		B
〃	9- 122	AN		B
VHITC4514P/-1	9- 123	AW		B
VHITL4558//-1	8- 43	AF		B
VHIUPD1990ACC	5- 85	AT		B
VHIUPD7220D-1	5- 86	BS		B
〃	10- 26	BS		B
VHIUPD765//-1	8- 44	BR		B
VHIUPD8255/-1	5- 87	AY		B
VHI2764//AC01	5- 88	LM		B
VHI2764//AC02	5- 88	LM		B
〃	9- 124	BM	N	B
VHI2764//AC03	5- 88	LM		B
〃	9- 124	BM	N	B
VHI2764//AC04	5- 88	LM		B
〃	9- 124	BM	N	B

PARTS CODE	NO	PRICE RANK	NEW MARK	PART RANK
VHi4164-150-H	5- 89	AZ		B
//	11- 11	AZ		B
VHi8251AC//-1	5- 90	AY		B
VHi8253////-1	5- 91	BA		B
VHPGL3PR2//-1	5- 92	AE		B
VHPGL9PR2//-1	1- 8	AC		B
//	9- 6	AC		B
VRD-RV2EY000J	5- 95	AA		C
VRD-RV2EY101J	11- 12	AA		C
VRD-RV2EY682J	5- 105	AA		C
VRD-ST2EY100J	6- 77	AA	N	C
//	6- 105	AA	N	C
VRD-ST2EY101J	5- 96	AA		C
//	8- 45	AA		C
//	9- 126	AA		C
//	10- 27	AA		C
VRD-ST2EY102J	5- 97	AA		C
//	6- 78	AA	N	C
//	6- 86	AA	N	C
//	6- 93	AA	N	C
//	6- 97	AA	N	C
//	6- 98	AA	N	C
VRD-ST2EY103J	5- 98	AA		C
//	9- 127	AA		C
//	10- 28	AA		C
VRD-ST2EY104J	5- 99	AA		C
//	9- 128	AA		C
VRD-ST2EY151J	6- 103	AA	N	C
VRD-ST2EY152J	6- 72	AA	N	C
//	6- 75	AA	N	C
//	6- 91	AA	N	C
VRD-ST2EY182J	6- 90	AA	N	C
VRD-ST2EY220J	6- 96	AA	N	C
//	6- 114	AA	N	C
VRD-ST2EY222J	5- 100	AA		C
//	6- 92	AA	N	C
//	6- 94	AA	N	C
//	9- 129	AA		C
VRD-ST2EY272J	6- 85	AA	N	C
VRD-ST2EY331J	5- 93	AA		C
//	5- 101	AA		C
//	6- 83	AA	N	C
//	6- 89	AA	N	C
//	6- 99	AA	N	C
//	6- 100	AA	N	C
//	6- 106	AA	N	C
//	8- 46	AA		C
//	10- 29	AA		C
VRD-ST2EY332J	5- 102	AA		C
//	8- 47	AA		C
//	9- 130	AA		C
//	10- 30	AA		C
VRD-ST2EY333J	5- 103	AA		C
//	6- 73	AA	N	C
//	6- 74	AA	N	C
//	9- 131	AA		C
VRD-ST2EY390J	6- 102	AA	N	C
//	6- 113	AA	N	C
VRD-ST2EY391J	6- 87	AA	N	C
VRD-ST2EY392J	6- 115	AA	N	C
VRD-ST2EY4R7J	6- 80	AB	N	C
VRD-ST2EY470J	5- 94	AA		C
VRD-ST2EY471J	6- 88	AA	N	C
//	9- 132	AA		C
VRD-ST2EY472J	6- 107	AA	N	C
//	8- 48	AA		C
VRD-ST2EY561J	5- 104	AA		C
VRD-ST2EY681J	6- 95	AA	N	C
//	6- 109	AA	N	C
//	6- 110	AA	N	C
//	9- 133	AA		C
VRD-SU2EY101J	8- 49	AA		C
VRD-SU2EY152J	5- 106	AA		C
VRD-SU2EY391J	8- 50	AA		C
VRD-SU2EY470J	5- 107	AA		C
//	10- 31	AA		C
VRD-SU2EY681J	5- 108	AA		C
VRD-SU2EY821J	5- 109	AA		C
VRD-SU2EY822J	5- 110	AA		C
//	8- 51	AA		C

PARTS CODE	NO	PRICE RANK	NEW MARK	PART RANK
VRD-SU2EY824J	8- 52	AA		C
VRN-RT2EK102F	6- 111	AB	N	C
VRN-RT2EK105F	8 53	AA		C
VRN-RT2EK123F	8- 54	AB		C
VRN-RT2EK222F	6- 112	AB	N	C
VRN-RT2EK472F	8- 55	AB		C
VRN-RT2EK912F	8- 56	AC		C
VRS-PT3AB100J	6- 84	AB	N	C
//	6- 108	AB	N	C
VRS-PT3AB102J	6- 70	AC	N	C
VRS-PT3DB102J	6- 104	AB	N	C
VRS-PT3DB152K	6- 71	AB	N	C
VRS-PT3DB680K	10- 32	AB		C
VRS-PT3LB330J	1- 39	AC		C
VSP0080P-608N	2- 7	AN		C
VS2SA673-C/-1	8- 57	AE		B
VS2SA673-D1-1	10- 33	AC		B
VS2SC458KC/-1	5- 111	AD		B
[X]				
XBBSC26P04000	2- 20	AA		C
XBBSC30P06000	2- 21	AA		C
XBPSD30P06KS0	2- 22	AA		C
//	5- 112	AA		C
//	9- 12	AA		C
XBPSD30P06K00	2- 8	AA		C
//	9- 134	AA		C
XBPSD30P08KS0	1- 27	AA		C
XBPSD30P08000	5- 113	AA		C
XBPSD30P10000	2- 30	AA		C
//	8- 58	AA		C
XBPSD30P30KS0	1- 38	AA		C
XBPSD40P06KS0	1- 28	AA		C
XBPSD40P06K00	1- 30	AA		C
XBPSD40P06000	10- 4	AA	N	C
XBPSD40P08KS0	2- 30	AA		C
XBPSF30P06K00	1- 16	AA		C
XBTSC40P06000	1- 31	AA		C
XBTSD30P04000	10- 34	AA		C
XBTSF40P08000	1- 32	AA		C
XCPSD40P12000	1- 33	AA		C
XNESD30-24000	2- 31	AA		C
//	2- 33	AA		C
//	8- 59	AA		C
XUPSC26P06000	9- 21	AA		C
XUPSC30P08000	9- 22	AA		C
XUPSD26P06000	2- 23	AA		C
[0]				
0AE10447100//	6- 125	AF	N	C
0AE10447113//	6- 126	AD	N	C
0AE10480387//	6- 127	AF	N	C
0AE10500623//	6- 129	AM	N	C
0AE10504917//	6- 138	AR	N	C
0AE10504933//	6- 139	AW	N	C
0AE10507778//	6- 130	BQ	N	C
0AE10507781//	6- 131	AQ	N	C
0AE10518482//	6- 128	AV	N	C
0AE10526940//	6- 133	BM	N	C
0AE10527981//	6- 132	AX	N	C
0AE10531087//	6- 140	AQ	N	C
0AE10538909//	6- 147	AW	N	C
0AE10538912//	6- 148	AW	N	C
0AE10543486//	6- 134	AY	N	C
0AE20490445//	6- 142	AC	N	C
0AE20510574//	6- 137	AC	N	C
0AE20512336//	6- 145	AM	N	C
0AE20521194//	6- 141	AA	N	C
0AE20527978//	6- 144	AG	N	C
0AE22830579//	6- 136	AC	N	C
0AE22831688//	6- 143	AR	N	C
0AE23594924//	6- 146	AC	N	C
0AE30109066//	6- 4	AE	N	B
//	6- 5	AE	N	B
//	6- 14	AE	N	B
//	6- 15	AE	N	B
0AE30116729//	6- 68	AK	N	C
//	6- 69	AK	N	C
0AE30120456//	6- 58	AC	N	C
//	6- 60	AC	N	C
0AE30120524//	6- 47	AC	N	C
//	6- 56	AC	N	C

PARTS CODE	NO	PRICE RANK	NEW MARK	PART RANK	
0AE30120524//	6- 65	AC	N	C	
//	6- 66	AC	N	C	
0AE30120650//	6- 44	AG	N	C	
0AE30121866//	6- 36	AN	N	B	
0AE30121921//	6- 25	AC	N	B	
//	6- 26	AC	N	B	
//	6- 28	AC	N	B	
//	6- 29	AC	N	B	
//	6- 34	AC	N	B	
0AE30121947//	6- 22	AF	N	B	
0AE30129460//	6- 48	AC	N	C	
//	6- 49	AC	N	C	
//	6- 50	AC	N	C	
//	6- 59	AC	N	C	
0AE30143284//	6- 82	AC	N	C	
0AE30143572//	6- 42	AC	N	C	
//	6- 43	AC	N	C	
0AE30159870//	6- 35	AY	N	B	
0AE30164409//	6- 57	AC	N	C	
//	6- 67	AC	N	C	
0AE30165262//	6- 37	AH	N	B	
0AE30165576//	6- 52	AG	N	C	
//	6- 53	AG	N	C	
0AE30167370//	6- 17	AT	N	B	
0AE30169653//	6- 45	AC	N	C	
//	6- 54	AD	N	C	
//	6- 55	AD	N	C	
0AE30170008//	6- 61	AG	N	C	
//	6- 62	AG	N	C	
0AE30195258//	6- 64	AG	N	C	
0AE30200774//	6- 30	AG	N	B	
//	6- 31	AG	N	B	
0AE30213525//	6- 63	AG	N	C	
0AE30216904//	6- 1	AS	N	B	
0AE30221517//	6- 7	AL	N	B	
0AE30221520//	6- 8	AH	N	B	
0AE30221546//	6- 18	AH	N	B	
0AE30227236//	6- 46	AD	N	C	
0AE30250326//	6- 33	AG	N	B	
0AE30258784//	6- 6	AX	N	B	
0AE30261658//	6- 21	AD	N	B	
0AE30263025//	6- 2	AD	N	B	
//	6- 3	AF	N	B	
//	6- 9	AD	N	B	
//	6- 11	AD	N	B	
//	6- 12	AD	N	B	
//	6- 13	AD	N	B	
//	6- 19	AD	N	B	
0AE30269430//	6- 20	AY	N	B	
0AE30272391//	6- 38	AP	N	C	
0AE30279844//	6- 16	AH	N	B	
0AE30280671//	6- 51	AE	N	C	
0AE30362052//	6- 10	AD	N	B	
0AE30362081//	6- 24	AD	N	B	
0AE30379029//	6- 27	AD	N	B	
//	6- 32	AD	N	B	
0AE30490940//	6-101	AE			
0AE30491169//	6- 76	AE	N	C	
0AE30499831//	6- 23	AD	N	B	
0AE30500979//	6-116	AH	N	A	
0AE30500982//	6-117	AW	N	B	
0AE30501868//	6- 81	AC	N	C	
0AE30508049//	6- 79	AG	N	C	
0AE30508528//	6-118	BP	N	B	
0AE30508531//	6-118	BY	N	B	
0AE30508557//	6-120	AX	N	C	
0AE30508560//	6-121	AL	N	C	
//	6-123	AX	N	C	
0AE30509721//	6- 39	AG	N	C	
//	6- 40	AG	N	C	
0AE30509941//	6-116	AG	N	A	
0AE30511353//	6- 38	AP	N	C	
0AE30515469//	6-119	AR	N	B	
0AE30523370//	6- 41	AP	N	C	
0AE30564740//	6-124	AP	N	C	
0AE30566353//	6 122	AX	N	C	
00PA7KF095C//	9- 51	BX	N	C	
00PA7KF102B//	9- 51	BX	N	C	
00PA7KF103B//	9- 51	BX	N	C	
00PA7KF104B//	9 51	BX	N	C	

PARTS CODE	NO	PRICE RANK	NEW MARK	PART RANK	
00PA8KF115A//	9- 50	AT	N	C	
00PCH52203A//	9- 39	AC	N	C	
00PKCC10901-Z	9- 27	AG	N	B	
00PKFL10901-Z	9- 25	AG	N	B	
00PKFL11901-Z	9- 26	AH	N	B	
00P08KF018B//	9- 28	AN	N	C	
00P16KF005A//	9- 37	AC	N	C	
00P19KF005A//	9- 35	AC	N	C	
00P19KF007A//	9- 36	AC	N	C	
00P21KF008A//	9- 31	AD	N	C	
00P21KF009A//	9- 33	AF	N	C	
00P21KF013A//	9- 32	AD	N	C	
00P21KF014A//	9- 34	AC	N	C	
00P23KF001A//	9- 46	AC	N	C	
00P23KF011B//	9- 29	AL	N	C	
00P23KF014A//	9- 47	AC	N	C	
00P25KF006B//	9- 30	AM	N	C	
00P25KF007A//	9- 48	AC	N	C	
00P25KF008A//	9- 49	AC	N	C	
00P27KF021A//	9- 38	AC	N	B	
00P29KF006B//	9- 44	AK	N	C	
00P29KF007B//	9- 45	AH	N	C	
00P80D9E43000	9- 42	AQ	N	C	
00P85Y2K56000	9- 40	AH	N	C	
00P85Y2K60000	9- 41	AH	N	C	

SHARP

SHARP CORPORATION
Industrial Instruments Group
Reliability & Quality Control Department
Yamatokoriyama, Nara 639-11, Japan
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